LC Voltage-Controlled Oscillators

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Content

- Introduction
- Fundamentals of LC VCOs
- On-chip inductors
- Varactors and F-V tuning curve
- Optimization of LC VCOs
- Techniques of lowering phase noise
- Design examples
- Conclusion and prospect
Introduction

Discrete TV Tuner Module

Novel Architecture for CMOS TV Tuner: **DLIF**
**Double Conversions with Low IF**

DLIF Architecture of TV tuner for DVB system
Frequency Synthesizers

PFD \rightarrow \text{LPF} \rightarrow \text{PFD} \rightarrow \text{LPF} \rightarrow \text{PFD} \rightarrow \text{LPF} \rightarrow \text{PFD} \rightarrow \text{LPF}

- 12.5MHz
- 50
- 250KHz
- 92\sim 158
- 4253\sim 4387
- 1150\sim 1975MHz
- 1063.5\sim 1096.5MHz
LC Voltage-Controlled Oscillators

High Q, Low Parasitic Resistor Inductors

High Q, High Tuning Range MOS Varactors

Design issues
- Low phase noise
- Low power
- Wideband tuning range
- F-V tuning curve
- Quadrature output
- etc …

CMOS Complementary Cross-coupled $-G_m$ LC VCO

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Outline

- Introduction
- Fundamentals of LC VCOs
  - Oscillator views
  - Mathematics of LC VCOs
  - Structures of different LC-VCOs
- On-chip inductors
- Varactors and F-V tuning curve
- Optimization of LC VCOs
- Techniques of lowering phase noise
- Design examples
- Conclusion and prospect
Oscillator Views

Two-port view: feedback system

- Transfer function

\[ \frac{V_{out}(s)}{V_{in}} = \frac{H(s)}{1 + H(s)} \]

- Barkhausen criterion

\[ |H(j\omega_0)| \geq 1 \quad \& \quad \angle H(j\omega_0) = 180^\circ \]

One-port view: Negative Resistance

- Active circuit

\[ R_{active} = -R_P \]

- Inductance cancels capacitance

\[ j\omega L = -\frac{1}{j\omega C} \]
Ring Oscillator and LC Oscillator

Ring oscillator

\[ H(s) = -\frac{A_0^n}{\left(1 + \frac{j\omega}{\omega_0}\right)^n} \]

\[ \omega_{osc} = \omega_0 \cdot \tan\left(\frac{180^\circ}{N}\right) \]

\[ A_0 = \sqrt{1 + \left(\tan\left(\frac{180^\circ}{N}\right)\right)^2} \]

- Advantage: Large tuning range
- Disadvantage: High phase noise

LC-Tank oscillator

- Advantage: Low phase noise
- Disadvantage: Small tuning range

Inductors & MOS Varactor designs
Mathematics of LC VCOs

F-V characteristic function

\[ \omega_{out} = \omega_0 + K_V \cdot V_{ctrl} \]

An ideal integrator in Phase-Locked Loop

\[ \frac{\phi_{ex}}{V_{ctrl}}(s) = \frac{K_V}{s} \]

Performance parameters

- Center frequency
- Tuning range
- Voltage-controlled gain
- Tuning linearity
- Phase noise
- Oscillating amplitude
- Power dissipation
Narrowband LC VCOs

NMOS-only –$G_m$ LC VCO

Complementary MOS –$G_m$ LC VCO

[Ali Hajimiri, JSSC, May, 1999]
Wideband LC VCOs

Wideband LC VCO with Switched Capacitors

Tradeoffs
- MIM capacitor
- Switched NMOS transistor
- Quality of capacitors

[A, Kral, A.A. Abidi, CICC, 1998]
Quadrature LC VCOs

Quadrature LC VCO with Superharmonic coupling

- Superharmonic coupling at Common-mode, S1 & S2
- Very simple
- Two same LC-VCOs
- Low phase noise
- Low power dissipation

\[ \text{(S. L. J. Gierkink, JSSC, July, 2003)} \]
Outline

- Introduction
- Fundamentals of LC VCOs
  - On-chip inductors
    - Inductor's Class
    - Modeling of on-chip inductors
    - Optimization of equivalent capacitance
    - Quality Factor improvement
- Varactors and F-V tuning curve
- Optimization of LC VCOs
- Techniques of lowering phase noise
- Design examples
- Conclusion and prospect
Inductor’s Class

Three types of On-chip inductors

(a) single-ended, (b) floating configurations

Gyrator-based active inductors

Bondwire inductors

On-chip spiral inductors
Planar Spiral Inductor

- Number of tuners, n
- Metal width, w
- Spacing, s
- Outer diameter, \( d_{\text{out}} \)
  Inner diameter, \( d_{\text{in}} \)
- Fill ratio, \( \rho = \frac{(d_{\text{out}} - d_{\text{in}})}{(d_{\text{out}} + d_{\text{in}})} \)
- Number of sides, N

(a) Square Spiral
(b) Hexagonal Spiral
(c) Octagonal Spiral
(d) Circular Spiral
Multilayer Spiral Inductor

Stacked spiral inductor

Miniature 3D spiral inductor

Differential multilayer inductor

[A. Zolfaghari, B. Razavi, JSSC, April, 2001]

[C.C Tang, S.I. Liu, JSSC, April, 2002]
Modeling of On-chip Inductors

- EM Field Solver
  - High accuracy
  - Very slow
  - Complex for Spice

- Segmental circuit models
  - Simpler than EM field solver
  - Easy integration into Spice

- Compact, scalable, lumped circuit models
  - Simple, versatile and robust
  - Physical intuition

Characteristic of inductance of a typical integrated inductors with frequency
What is the equivalent capacitance

- At resonance frequency, the peak magnetic and electric energies are equal.
- Given a peak voltage \( V_0 \), electric energy is \( C_{eq} V_0^2 / 2 \)

First resonance frequency \( f_{SR} \)

\[
f_{SR} = \left( \frac{2\pi \sqrt{L_{eq} C_{eq}}}{} \right)^{-1}
\]

The proposed equivalent capacitance models

- Electric energy in interlayer metals, \( C_{M-M} \)
- Electric energy in single metal to substrate, \( C_{M-S} \)
Electric Energy in $C_{M-M}$ and $C_{M-S}$

$C_{M-M}$

$C_{M-S}$

Electric Energy

$$E_{e,C} = \sum_{m=1}^{N} E_{e,C_m} = \sum_{m=1}^{N} \frac{1}{2} C_m V_{c_m}^2$$

$$= \frac{1}{2} C_{M_{n-M_{n-1}}} w (V_1 - V_2)^2$$

Electric Energy

$$E_{e,C} = \sum_{m=1}^{N} E_{e,C_m} = \sum_{m=1}^{N} \frac{1}{2} C_m V_{c_m}^2$$

$$= \frac{1}{2} \sum_{m=1}^{N} C_{M_{n-M_{n-1}}} w \left( V_1 - \frac{m}{N} \Delta V \right)^2$$

$$\approx \frac{1}{6} C_{M_{n-M_{n-1}}} w \left( V_1^2 + V_2^2 + V_1 V_2 \right)$$
Voltage Profile

[A. Zolfaghari, B. Razavi, JSSC, April, 2001]

Stacked

Substrate

1st Turn 2nd Turn 3rd Turn

$V_0$ $C_{W-M1}$ $C_{W-M2}$ $C_{W-M3}$

$V_0/2$ $C_{W-M1}$ $C_{W-M2}$ $C_{W-M3}$

Bottom

Top

Bottom

Top

Bottom

Top

[ C.C Tang, S.I. Liu, JSSC, April, 2002]

Miniature 3D

Substrate

$V_0$ $C_{W-M1}$ $C_{W-M2}$ $C_{W-M3}$

$V_0/2$ $C_{W-M1}$ $C_{W-M2}$ $C_{W-M3}$

Bottom

Top

Bottom

Top

Bottom

Top

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Capacitance Coefficients

\[ C_{eq} = \kappa_1 C_1 + \kappa_2 C_2 \]

- Higher \( f_{SR} \)
- Small Area
- 3D or Stacked
Quality Factor Improvement

- Pattern ground shield
- Multipath metal
- Dual reverse-bias PN-junction isolation in deep Nwell
  Stop eddy current in skin channel
Outline

- Introduction
- Fundamentals of LC VCOs
- On-chip inductors
- Varactors and F-V tuning curve
  - Varactors’ class
  - Period calculation of LC VCO with step-like varactors
- Optimization of LC VCOs
- Techniques of lowering phase noise
- Design examples
- Conclusion and prospect
Varactors’ Class

- Four Types of Varactors in Silicon CMOS:
  PN Junction, Standard MOS, Inversion-MOS, Accumulation-MOS

(a) p+/n-well Junction

(b) D=S=B MOS

(c) Inversion MOS

(d) Accumulation MOS
DC Capacitance of MOS Varactors

(a) S=D=B PMOS Varactor  
(b) Inversion PMOS Varactor  
(c) Accumulation NMOS Varactor
Step-like Varactors

- Small-signal capacitance of step-like varactors

\[ C_{ss}(V) = \begin{cases} C_{\max} & V \geq V_{eff} \\ C_{\min} & V \leq V_{eff} \end{cases} \]

- Effective control voltage

\[ V_{eff} = V_G - V_{ctrl} - V_{TH} \]

\[ C_{ss}(V) = \frac{1}{2}(C_{\max} + C_{\min}) + \frac{1}{2}(C_{\max} - C_{\min}) \text{sign}(V - V_{eff}) \]
Oscillating Waveforms in LC-Tank

Oscillating waveforms at different $V_{\text{eff}}$

Two ellipses of different sizes joint with a step transition at $V_{\text{eff}}$

I-V locus of Step-like varactor

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# Oscillating Period Calculation

<table>
<thead>
<tr>
<th>Effective Control Voltage, $V_{\text{eff}}$</th>
<th>Oscillating Period of LC Tank</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{eff}} &lt; V_{\text{vdd}} - A_{\text{min}}$</td>
<td>$T = T_{\text{max}} = 2\pi \sqrt{LC_{\text{max}}}$</td>
</tr>
<tr>
<td>$V_{\text{eff}} &gt; V_{\text{vdd}} + A_{\text{max}}$</td>
<td>$T = T_{\text{min}} = 2\pi \sqrt{LC_{\text{min}}}$</td>
</tr>
<tr>
<td>$V_{\text{vdd}} - A_{\text{min}} &lt; V_{\text{eff}} &lt; V_{\text{vdd}}$</td>
<td>$T = \frac{1}{2}(T_{\text{max}} + T_{\text{min}}) + \frac{1}{\pi} \left( \arcsin \left( \frac{V_{\text{eff}}}{A_{\text{min}}} \right) T_{\text{max}} - \arcsin \left( \frac{V_{\text{eff}}}{\theta_1 A_{\text{max}}} \right) T_{\text{min}} \right)$</td>
</tr>
<tr>
<td>$V_{\text{vdd}} &lt; V_{\text{eff}} &lt; V_{\text{vdd}} + A_{\text{max}}$</td>
<td>$T = \frac{1}{2}(T_{\text{max}} + T_{\text{min}}) + \frac{1}{\pi} \left( -\arcsin \left( \frac{V_{\text{eff}}}{\theta_2 A_{\text{min}}} \right) T_{\text{max}} + \arcsin \left( \frac{V_{\text{eff}}}{A_{\text{max}}} \right) T_{\text{min}} \right)$</td>
</tr>
</tbody>
</table>

**Ellipse Similar Factor**

$\theta_1 = \sqrt{1 - \left( \frac{V_{\text{eff}}}{A_{\text{min}}} \right)^2 + \left( \frac{V_{\text{eff}}}{A_{\text{max}}} \right)^2}$

$\theta_2 = \sqrt{1 - \left( \frac{V_{\text{eff}}}{A_{\text{max}}} \right)^2 + \left( \frac{V_{\text{eff}}}{A_{\text{min}}} \right)^2}$
Simulation Verification in HSPICE

Simulation agrees well with the proposed calculation

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Comparison with Others’ Model

Hegazi’s effective capacitance model

\[ C_{\text{eff}} = \frac{1}{2}(C_{\text{max}} + C_{\text{min}}) + \frac{1}{\pi}(C_{\text{min}} - C_{\text{max}}) \left( \frac{\sin(V_{\text{eff}}/A)}{V_{\text{eff}}/A} + \frac{V_{\text{eff}}}{A} \sqrt{1 - \left(\frac{V_{\text{eff}}}{A}\right)^2} \right) \]

- Point A
  \[ F_{\text{eff},A} = \frac{2F_{\text{min}} \cdot F_{\text{max}}}{F_{\text{min}} + F_{\text{max}}} \]

- Point B
  \[ F_{\text{eff},B} = \frac{\sqrt{2}F_{\text{min}} \cdot F_{\text{max}}}{\sqrt{F_{\text{min}}^2 + F_{\text{max}}^2}} \]

\[ F_{\text{eff},B} \leq F_{\text{eff},A} \]

The reasons for difference between two methods:

a) Hegazi’s model is small-signal analysis;

b) Neglect 2nd and higher order harmonics;

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[E. Hegazi, A.A. Abidi, JSSC, June, 2003]
Validation with Others’ LC-VCOs

Frequency-Voltage Curves

[Y.B. Choi, 5th ASICON, 2003]  [H.L.Lao, 5th ASICON, 2003]
Outline

- Introduction
- Fundamentals of LC VCOs
- On-chip inductors
- Varactors and F-V tuning curve
- Optimization of LC VCOs
  - Low power design and low phase noise
  - Underlying physics of LC oscillators
  - Optimization method: Linear and Geometric Programming
- Techniques of lowering phase noise
- Design examples
- Conclusion and prospect
Low-power Design

- Energy Conservation Theorem

\[ \frac{CV_{\text{peak}}^2}{2} = \frac{LI_{\text{peak}}^2}{2} \]

- The loss in RLC tank

\[ P_{\text{loss}} = RC^2\omega_0^2V_{\text{peak}}^2 = \frac{R}{L^2\omega_0^2}V_{\text{peak}}^2 \]

- Low-power design
  - Lower serial resistance R
  - Increase the tank inductance
  - Work at high frequency

\[ \omega_0 = \frac{1}{\sqrt{LC}} \]

\[ Q_{\text{tank}} = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 CR} = \frac{1}{R \sqrt{C}} \]


[ASIC & System State-Key Laboratory, Fudan University]

[M. Tielbou, JSSC, Jul. 2001]
Low-phase-noise Design

- Phase noise (SSCR)
  \[ L(\Delta \omega) \propto \frac{KT}{2P_{\text{sig}}} \frac{\omega_0^2}{Q^2 \Delta \omega^2} \]
  \[ Q_{\text{tank}} \]
  \[ L(\Delta \omega) \propto \frac{KT}{V_{\text{peak}}^2} \frac{R^3}{L^2 \Delta \omega^2} \]

- Low-phase-noise design
  - Lower serial resistance R
  - Increase the tank inductance
  - Increase amplitude voltage

\[ Q_{\text{tank}} = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 CR} = \frac{1}{R} \sqrt{\frac{L}{C}} \]
Underlying Physics of LC Oscillators

\[ V_{\text{tank}} = \begin{cases} \frac{(4/\pi)I_{\text{bias}}}{g_{\text{tank}}} & (I - \text{limited}) \\ \frac{V_{\text{limit}}}{V_{\text{limit}}} & (V - \text{limited}) \end{cases} \]

\[ V_{\text{tank}} = \begin{cases} \sqrt{2E_{\text{tank}}\omega_0^2L} & (L - \text{limited}) \\ \frac{V_{\text{limit}}}{V_{\text{limit}}} & (V - \text{limited}) \end{cases} \]

[\text{A. Hajimiri, JSSC, May 1999}]
The equipartition theorem of thermodynamics states that:

Any system in equilibrium has a mean energy of KT/2

\[ C\langle v_n^2 \rangle / 2 = KT / 2 \]

\[ \langle v_n^2 \rangle = \frac{KT}{C} = KT \omega_0^2 L \]

\[ E_{\text{tank}} \propto I_{\text{tail}}^2 / L g_{\text{tank}}^2 \approx I_{\text{tail}}^2 / L g_L^2 \quad (L-\text{limited}) \]

\[ \frac{\langle v_n^2 \rangle}{V_{\text{tank}}^2} \propto \frac{1}{E_{\text{tank}}} \quad (L-\text{limited}) \]

\[ \frac{\langle v_n^2 \rangle}{V_{\text{tank}}^2} \propto \frac{L g_L^2 / I_{\text{tail}}^2}{L} \quad (L-\text{limited}) \]

\[ \frac{\langle v_n^2 \rangle}{V_{\text{tank}}^2} \propto \frac{L g_L^2 / I_{\text{tail}}^2}{L} \quad (L-\text{limited}) \]

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\[ \frac{\langle v_n^2 \rangle}{V_{\text{tank}}^2} \propto \frac{L g_L^2 / I_{\text{tail}}^2}{L} \quad (L-\text{limited}) \]
Design Insight

- $Lg_L^2$ increasing with $L$
  
  Startup condition
  Minimum tank amplitude
  Optimization at feasible point

- $Lg_L^2$ decreasing with $L$
  
  Optimization at the verge of inductance-limited and voltage-limited regime

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LC VCO Topology

12 initial design variables

- MOS transistors
  \[ W_n, L_n, W_p, L_p \]
- On-chip spiral inductors
  \[ d_{out}, w, s, n \]
- MOSCAP varactors
  \[ C_{v,max}, C_{v,min} \]
- Load cap and tail current
  \[ C_{load}, I_{tail} \]
LC VCO Parameters

\[ g_L = \frac{1}{R_p} + R_s / (L \omega)^2 \]

\[ g_v = \frac{(C_v \omega)}{Q_v} \]

\[ 2g_{tank} = g_{on} + g_{op} + g_v + g_L \]

\[ 2g_{active} = g_{mn} + g_{mp} \]

\[ L_{tank} = 2L \]

\[ 2C_{tank} = C_{PMOS} + C_{NMOS} + C_L + C_v + C_{load} \]

\[ C_{NMOS} = C_{gs,n} + C_{db,n} + 4C_{gd,n} \]

\[ C_{PMOS} = C_{gs,p} + C_{db,p} + 4C_{gd,p} \]
Design Constraints

(1) Power dissipation
\[ I_{\text{tail}} \leq I_{\text{max}} \]

(2) Oscillator voltage amplitude
\[ V_{\text{tank}} = \frac{I_{\text{tail}}}{g_{\text{tank,max}}} = \frac{2I_{\text{tail}}}{g_{\text{on}} + g_{\text{op}} + g_{\text{v}} + g_{L}} \approx \frac{2I_{\text{tail}}}{g_{L}} \geq V_{\text{tank,min}} \]

(3) Tuning range
\[ L_{\text{tank}} C_{\text{tank,min}} \leq \frac{1}{\omega_{\text{max}}^2} \quad L_{\text{tank}} C_{\text{tank,max}} \geq \frac{1}{\omega_{\text{min}}^2} \]
\[ \omega_{\text{max}} - \omega_{\text{min}}) / \omega = r_{t,min} \quad (\omega_{\text{max}} + \omega_{\text{min}}) / 2 = \omega \]

(4) Startup condition
\[ g_{\text{active}} \geq \alpha_{\text{min}} g_{\text{tank,max}} \]

(5) Maximum diameter of spiral inductor
\[ d \leq d_{\text{max}} \]

etc. …
Phase Noise Optimization

- In $1/f^2$ region, Phase noise (SSCR)

\[
L\{\Delta\omega\} \propto \left\{ \begin{array}{l}
\frac{L^2 g_L^2}{I_{\text{tail}}} \\
\frac{L^2 I_{\text{tail}}}{V_{\text{supply}}^2}
\end{array} \right. \quad (L - \text{limited})
\]

\[
Lg_L \approx L \left( R_s I(L\omega)^2 \right) = \frac{R_s}{L\omega^2}
\]

\[
L\{\Delta\omega\} \propto \left\{ \begin{array}{l}
\left( \frac{R_s}{L} \right)^2 \cdot \frac{1}{\omega^4 I_{\text{tail}}} \\
\frac{L^2 I_{\text{tail}}}{V_{\text{supply}}^2}
\end{array} \right. \quad (V - \text{limited})
\]

[D. Ham, and A. Hajimiri, JSSC, 2001]

Proposed optimization equation

Design strategy
- Lower $R_s/L$ of on-chip inductor, or select high $Q_L$ inductor
- At maximum current $I_{\text{max}}$
- At verge of inductance-limited and voltage-limited regime
Graphical Optimization

Lower $R_s/L$ in on-chip inductor,

Decrease or increase $I_{tail}$

Lower $R_s/L$ in on-chip inductor,

Decrease or increase $I_{tail}$
Geometric Programming

• What?

A special form of optimization problem:

\[
\begin{align*}
\text{minimize} & \quad f_0(x) \\
\text{subject to} & \quad f_i(x) \leq 1, \quad i = 1, \ldots, m \\
& \quad g_i(x) = 1, \quad i = 1, \ldots, p \\
& \quad x_i > 0, \quad i = 1, \ldots, n
\end{align*}
\]

where \( f_i \) are posynomial and \( g_i \) are monomial

• Object Function: phase noise

\[
L\{\Delta \omega\} = 10 \cdot \log \left( \frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{j_n^2/\Delta f}{2 \cdot \Delta \omega^2} \right)
\]

\[
\Gamma(\omega_0 \tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau + \theta_n)
\]

\[
\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi} \int_0^{2\pi} |\Gamma(x)|^2 \, dx = 2\Gamma_{rms}^2
\]
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- Techniques of lowering phase noise
  - Limited noise factor for white noise
  - Noise filtering techniques
  - Inductive control voltage
- Design examples
- Conclusion and prospect
Limited Noise Factor for White Noise

\[ \frac{V_n^2}{\Delta f} = 4KTR_N \]

- Phase noise

\[ L\{\Delta \omega\} = 10 \cdot \log \left( \frac{V_{n,SSB}^2}{\Delta f} \right) = 10 \cdot \log \left( \frac{F \cdot KT}{2P_{\text{sig}}Q^2} \left( \frac{\omega_0}{\Delta \omega} \right)^2 \right) \]

- Limited noise factor

\[ F = \frac{R_N}{R_P} = 1 + \frac{\gamma_n + \gamma_p}{2} = 1 + \gamma \]

[ASIC & System State-Key Laboratory, Fudan University]

[F. Herzel and M. Tiebout, TCASII, Jan. 2000]
Noise Sources of Close-in Phase Noise

- Flicker noise of tail current
  AM-FM modulation

- Flicker noise of differential pairs
  Differential pairs looks like a “Mixer”.
  Flicker noise modulates the baseband and 2\textsuperscript{nd} harmonics voltage at the tail.

- Varactor nonlinearity
  AM-FM modulation of common noise, power and substrate noise.

Leeson’s model

\[
L\{\Delta \omega\} = 10 \log \left( \frac{2FkT}{P_s} \cdot \left[ 1 + \left( \frac{\omega_0}{2Q_L \Delta \omega} \right)^2 \right] \cdot \left( 1 + \frac{\Delta \omega_{\text{vel}}}{|\Delta \omega|} \right) \right)
\]
Noise Filtering Techniques (1)

- Lower channel length modulation
- Filtering noise from tail current

Without large capacitor

With large capacitor

[ ASIC & System State-Key Laboratory, Fudan University ]

[A. Hajimiri, JSSC, May. 1999]
Noise Filtering Techniques (2)

Remove of tail current

Roles of the tail current:
- Supply DC current
- Boost high impedance at common-source node
- Avoiding Q-degradation by triode region FETs

(a) Without tail current
(b) With tail current

[S. Levantino, JSSC, Aug. 2002]
Noise Filtering Techniques (3)

LC filter at 2\textsuperscript{nd} harmonic

- L1 & C1, L2 & C2 resonates at 2\textsuperscript{nd} harmonic
- Boost the impedance at each common-source node, avoiding Q-degradation
- Improve the oscillating amplitude voltage, and voltage-limited moves into current-limited


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[E. Hegazi, JSSC, Dec. 2001]
Inductive Control Voltage (Proposed)

- L3 & C3 resonates at 2\textsuperscript{nd} harmonic
- Lower even harmonics in oscillating voltage
- The oscillating voltage is more symmetric in one period

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- Design examples
  - 1.08 GHz narrow LC VCO
  - 1.0-2.0 GHz wideband LC VCO

- Conclusion and prospect
Example I: 1.08GHz Narrowband LC VCO

- Chartered CMOS 0.35μm 2P4M RF/MS process
- 72-side inductor and A-MOS Varactor in Chartered library
- Die Size: 1120μm × 820μm

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Simulation and Measurement of F-V Curve

L=5.755nH; V_0=2.208V
F_{max}=1.164GHz; F_{min}=0.970GHz
C_{min}=3.247pf; C_{max}=4.675pf
A_{min}=0.811V; A_{max}=0.973V

L=5.760nH; V_0=2.083V
F_{max}=1.134GHz; F_{min}=0.978GHz
C_{min}=3.421pf; C_{max}=4.610pf
A_{min}=0.860V; A_{max}=1.000V
Phase Noise (Simulation)

- Simulation in Cadence SpectreRF:
  - Bias at 3.1mA
  - Phase Noise < -82.2dBc/Hz@10kHz

<table>
<thead>
<tr>
<th>Power Voltage</th>
<th>3.3V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current</td>
<td>3.1mA</td>
</tr>
<tr>
<td>Oscillating Frequency</td>
<td>945MHz-1137MHz</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>±8.9%</td>
</tr>
<tr>
<td>Phase Noise (Simulation)</td>
<td>-82.2dBc/Hz@10kHz, -108dBc/Hz@10kHz, -129.3dBc/Hz@10kHz</td>
</tr>
</tbody>
</table>
Example II: 1-2 GHz Wideband LC VCO

- LC oscillator core
- Switched-capacitor array
- Switched-current array
- Encoder
Differential On-Chip Inductor

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Diameter</td>
<td>100 ( \mu \text{m} )</td>
</tr>
<tr>
<td>Sides</td>
<td>16</td>
</tr>
<tr>
<td>Turns</td>
<td>5</td>
</tr>
<tr>
<td>Width</td>
<td>15 ( \mu \text{m} )</td>
</tr>
<tr>
<td>Spacing</td>
<td>1.5 ( \mu \text{m} )</td>
</tr>
<tr>
<td>Inductance</td>
<td>5.2 nH</td>
</tr>
<tr>
<td>Single-end Q</td>
<td>&gt;5</td>
</tr>
</tbody>
</table>

De-embedded PAD

![Simulation vs Measurement Graph]

- Single-end Q
- Single-end Inductance

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Simulation and Measurement of F-V Curve
Phase Noise (Simulation)

- Simulation in Cadence SpectreRF: Bias at 1.15mA
- Phase Noise < -80dBc/Hz@10kHz
- Die Size: 1120µm × 1200µm

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Voltage</td>
<td>3.3V</td>
</tr>
<tr>
<td>Current</td>
<td>3.5-10mA</td>
</tr>
<tr>
<td>Oscillating Frequency</td>
<td>1041MHz-1968MHz</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>±31%</td>
</tr>
<tr>
<td>Phase Noise (Simulation)</td>
<td>-79dBc/Hz@10kHz</td>
</tr>
<tr>
<td></td>
<td>-104.4dBc/Hz@10kHz</td>
</tr>
<tr>
<td></td>
<td>-125.3dBc/Hz@10kHz</td>
</tr>
</tbody>
</table>

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PFTN (Power-Frequency-Tuning-Normalized)

\[ PFTN = 10 \log \left[ \frac{kT}{P_{\text{sup}}} \left( \frac{f_{\text{tune}}}{f_{\text{off}}} \right)^2 \right] - L(f_{\text{off}}) \]

<table>
<thead>
<tr>
<th>Reference</th>
<th>Process (µm)</th>
<th>Power (mW)</th>
<th>( f_{\text{tune}} ) (MHz)</th>
<th>( F_0 ) (GHz)</th>
<th>Phase noise (dBc/Hz)</th>
<th>PFTN (dB)</th>
<th>Order</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.08GHz</td>
<td>0.35</td>
<td>10.23</td>
<td>192</td>
<td>1.08</td>
<td>-129@1MHz</td>
<td>-8.94</td>
<td>7</td>
</tr>
<tr>
<td>1.1-2GHz</td>
<td>0.35</td>
<td>33</td>
<td>927</td>
<td>1.50</td>
<td>-125@1MHz</td>
<td>-4.35</td>
<td>3</td>
</tr>
<tr>
<td>[13]</td>
<td>0.35</td>
<td>10</td>
<td>790</td>
<td>2.4</td>
<td>-115@600kHz</td>
<td>-6.41</td>
<td>5</td>
</tr>
<tr>
<td>[14]</td>
<td>0.7</td>
<td>24</td>
<td>81</td>
<td>1.8</td>
<td>-115@200kHz</td>
<td>-20.46</td>
<td>9</td>
</tr>
<tr>
<td>[15]</td>
<td>0.25</td>
<td>6</td>
<td>1</td>
<td>1.8</td>
<td>-121@600kHz</td>
<td>-56.15</td>
<td>10</td>
</tr>
<tr>
<td>[16]</td>
<td>0.35</td>
<td>12</td>
<td>364</td>
<td>1.3</td>
<td>-119@600kHz</td>
<td>-9.94</td>
<td>8</td>
</tr>
<tr>
<td>[17]</td>
<td>0.25</td>
<td>20</td>
<td>270</td>
<td>1.86</td>
<td>-143@3MHz</td>
<td>-4.73</td>
<td>4</td>
</tr>
<tr>
<td>[18]</td>
<td>0.25</td>
<td>7.25</td>
<td>1100</td>
<td>5.2</td>
<td>-132@3MHz</td>
<td>0.87</td>
<td>1</td>
</tr>
<tr>
<td>[19]</td>
<td>0.25</td>
<td>21.875</td>
<td>640</td>
<td>5.0</td>
<td>-124@1MHz</td>
<td>-7.08</td>
<td>6</td>
</tr>
<tr>
<td>[20]</td>
<td>0.13</td>
<td>2.7</td>
<td>1900</td>
<td>4.6</td>
<td>-112@1MHz</td>
<td>-0.85</td>
<td>2</td>
</tr>
</tbody>
</table>
Conclusions

- On-chip inductors
  - Equivalent capacitance
  - Differential multilayer inductor
  - Quality factor improvement techniques

- Varactors and F-V tuning curve
  - Period calculation of LC-VCO with step-like varactor

- Optimization of LC VCO
  - High Q inductor, Lower $R_s/L$ in on-chip inductor

- Techniques of lowering phase noise
  - Inductive control voltage

- Two design examples
Prospect(1): Switched MIM-Cap Varactor

C-V Curve

Switched MIM-Cap

Direct Model

Cross Model

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Prospect(2): Varactor and Vaructor

- **Variable Resonator: Varactor**
- **Variable Inductor: Vaructor**

![Varactor Diagram](image1)

![Vaructor Diagram](image2)
1.08GHz LC VCO with MIM Varactors

- Simulation in SpectreRF
  - F-V curves, 3.3mA
- Phase Noise < -89.7dBc/Hz@10kHz
- Better phase noise in LC-VCO with MIM Varactor than in one with MOS Varactor
- Simulation agrees well with the calculation
- TSMC 0.25µm 2P5M RF/MS process

TSMC CMOS 0.25µm 1P5M RF/MS Process
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