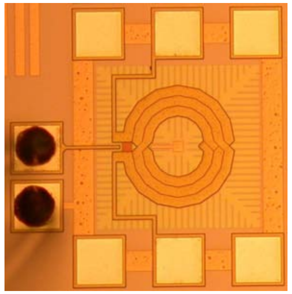
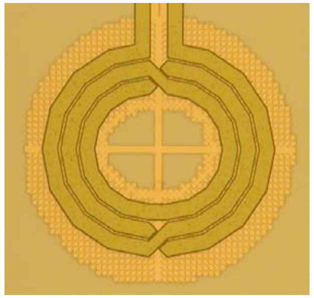
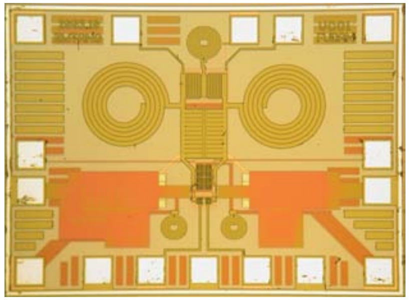
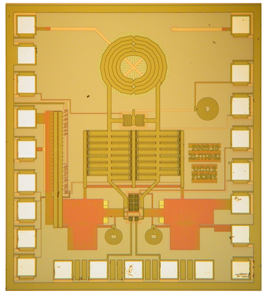
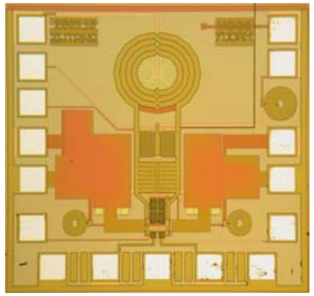






LC Voltage-Controlled Oscillators

Zhangwen Tang

Advisor : Professor Hao Min

zwtang@fudan.edu.cn, http://10.12.240.202

Jun. 4th, 2004

ASIC & System State-Key Laboratory,

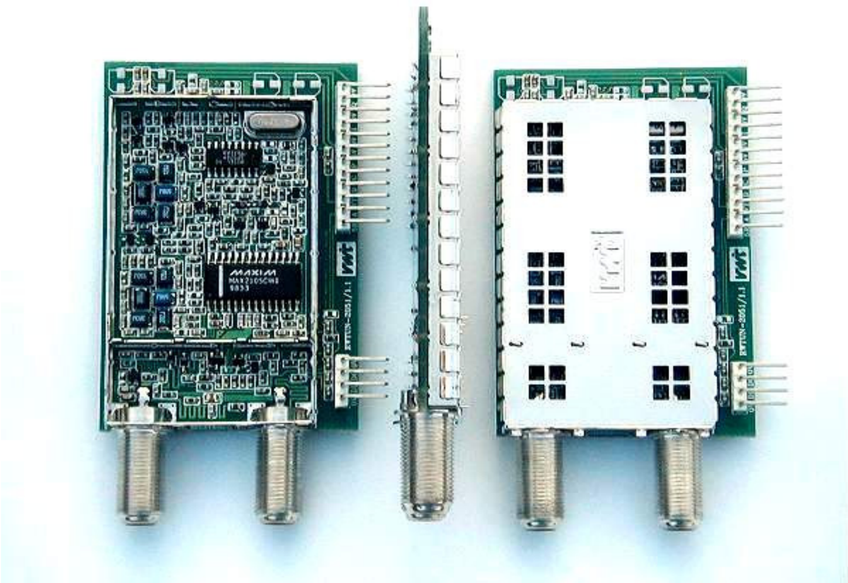
Fudan University

Content

- Introduction
- Fundamentals of LC VCOs
- On-chip inductors
- Varactors and F-V tuning curve
- Optimization of LC VCOs
- Techniques of lowering phase noise
- Design examples
- Conclusion and prospect

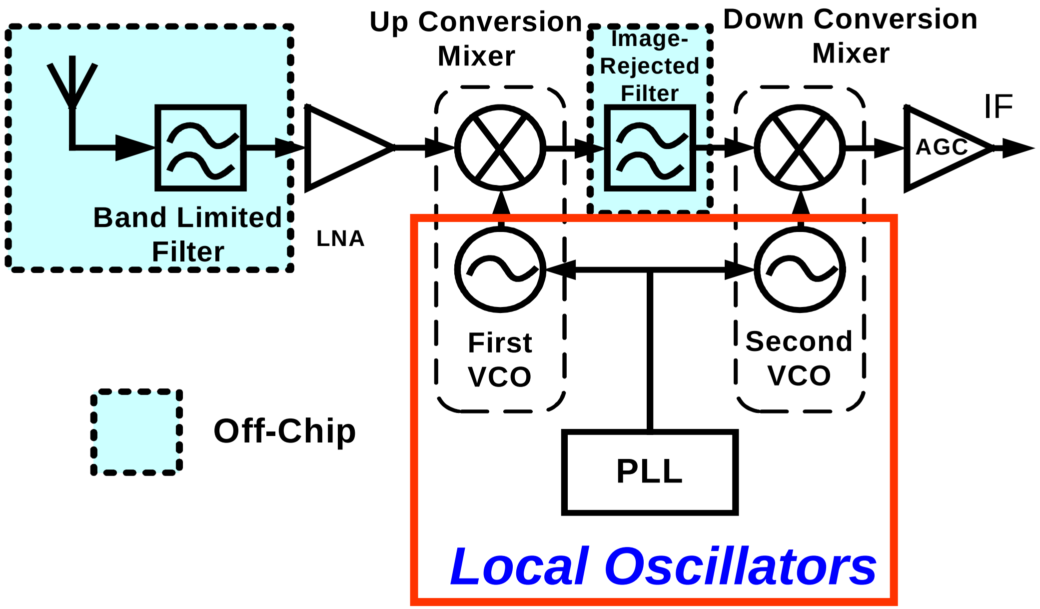
Introduction

Discrete TV Tuner Module



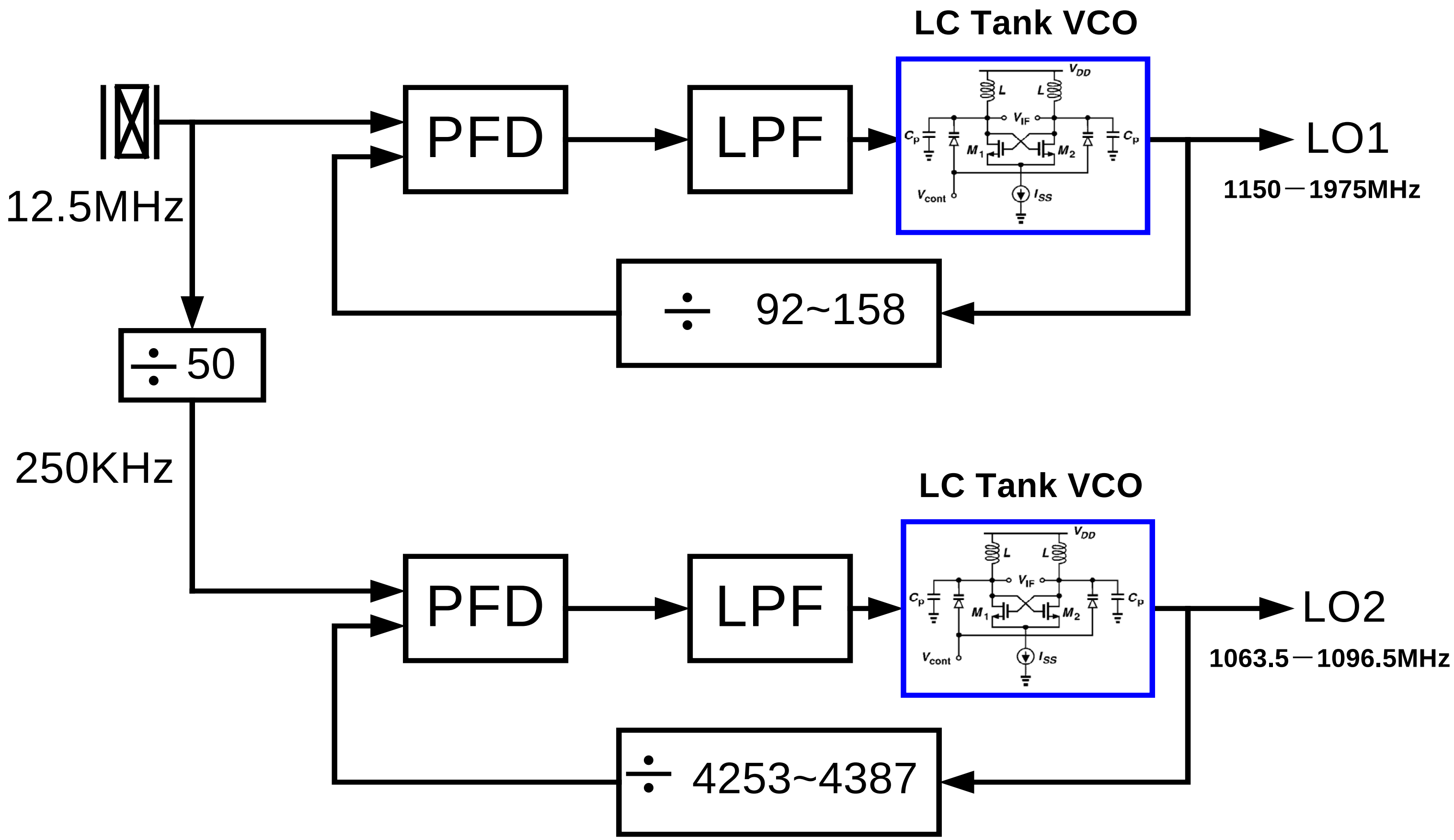
Novel Architecture for CMOS TV Tuner: *DLIF*

*D*ouble Conversions with *L*ow *IF*



DLIF Architecture of TV tuner for DVB system

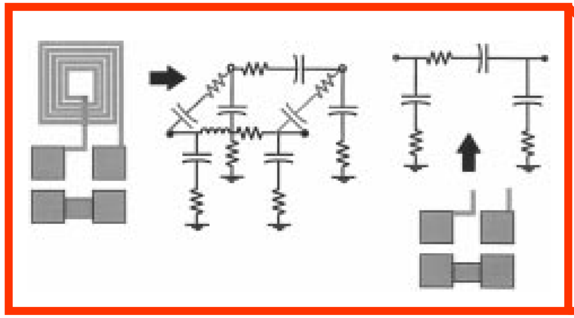
Frequency Synthesizers

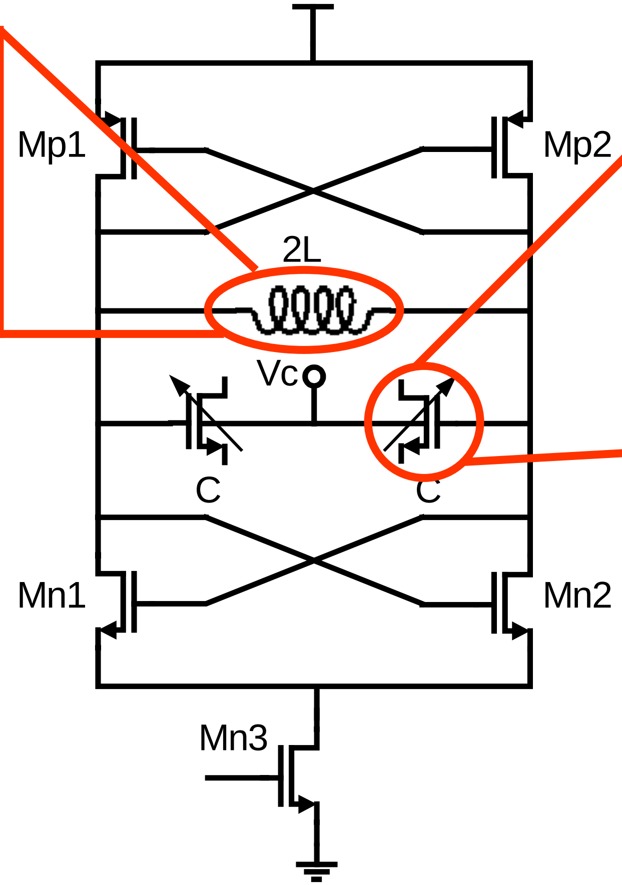


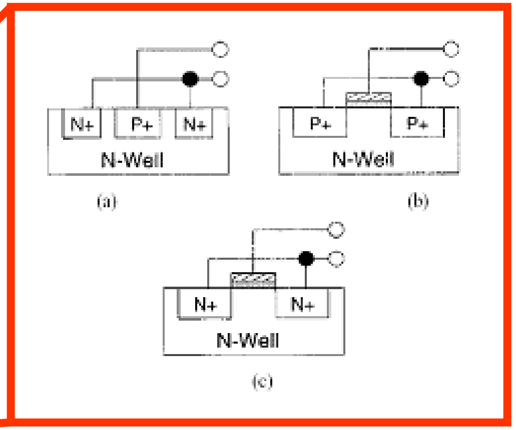
LC Voltage-Controlled Oscillators

High Q, Low Parasitic Resistor Inductors

High Q, High Tuning Range MOS Varators







Design issues

- Low phase noise
- Low power
- Wideband tuning range
- F-V tuning curve
- Quadrature output
- etc …

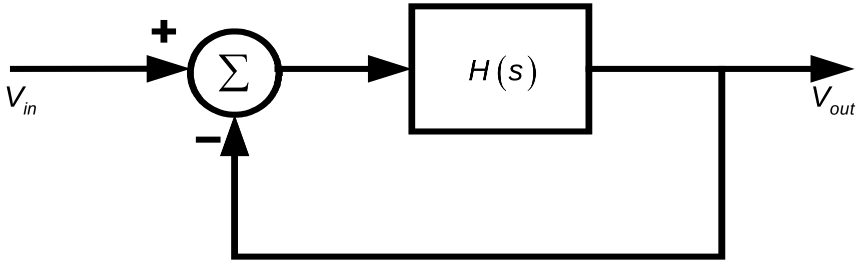
CMOS Complementary Cross-coupled $-G_m$ LC VCO

Outline

- Introduction
- Fundamentals of LC VCOs
  - Oscillator views
  - Mathematics of LC VCOs
  - Structures of different LC-VCOs
- On-chip inductors
- Varactors and F-V tuning curve
- Optimization of LC VCOs
- Techniques of lowering phase noise
- Design examples
- Conclusion and prospect

Oscillator Views

Two-port view : feedback system



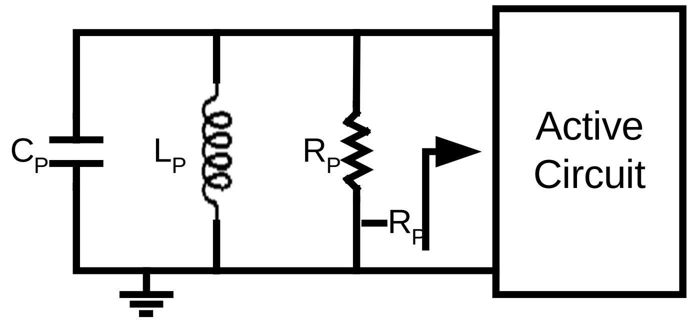
- Transfer function

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1+H(s)}$$

- Barkhausen criterion

$$|H(j\omega_0)| \geq 1 \quad \& \quad \angle H(j\omega_0) = 180^\circ$$

One-port view : Negative Resistance



- Active circuit

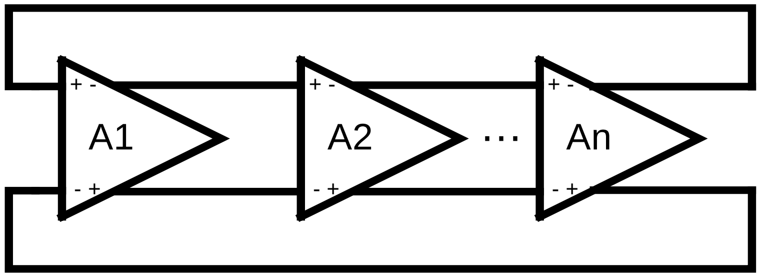
$$R_{active} = -R_P$$

- Inductance cancels capacitance

$$j\omega L = -\frac{1}{j\omega C}$$

Ring Oscillator and LC Oscillator

Ring oscillator



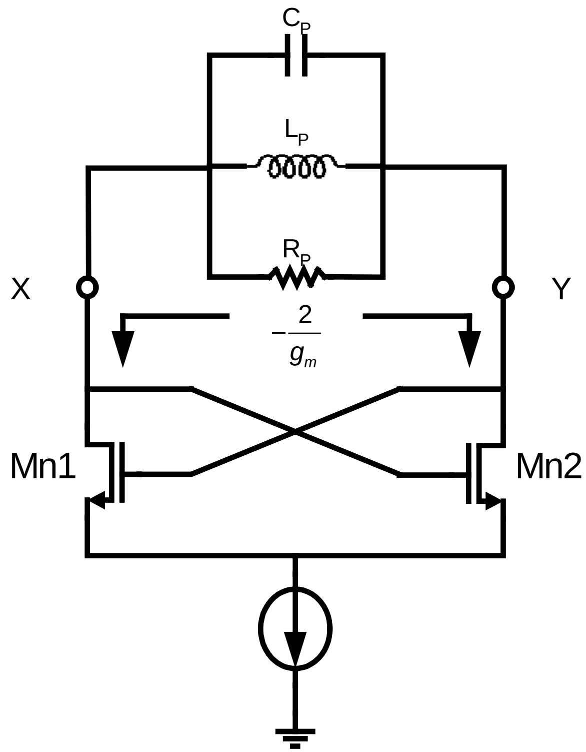
Transfer function

$$H(s) = -\frac{A_0^n}{\left(1+\frac{j\omega}{\omega_0}\right)^n}$$

$$\omega_{osc} = \omega_0 \cdot \tan\left(\frac{180^\circ}{N}\right) \qquad A_0 = \sqrt{1+\left(\tan\left(\frac{180^\circ}{N}\right)\right)^2}$$

- ***Advantage:*** Large tuning range
- ***Disadvantage:*** High phase noise

LC-Tank oscillator



- ***Advantage:*** Low phase noise
- ***Disadvantage:*** Small tuning range
  Inductors &
  MOS Varactor designs

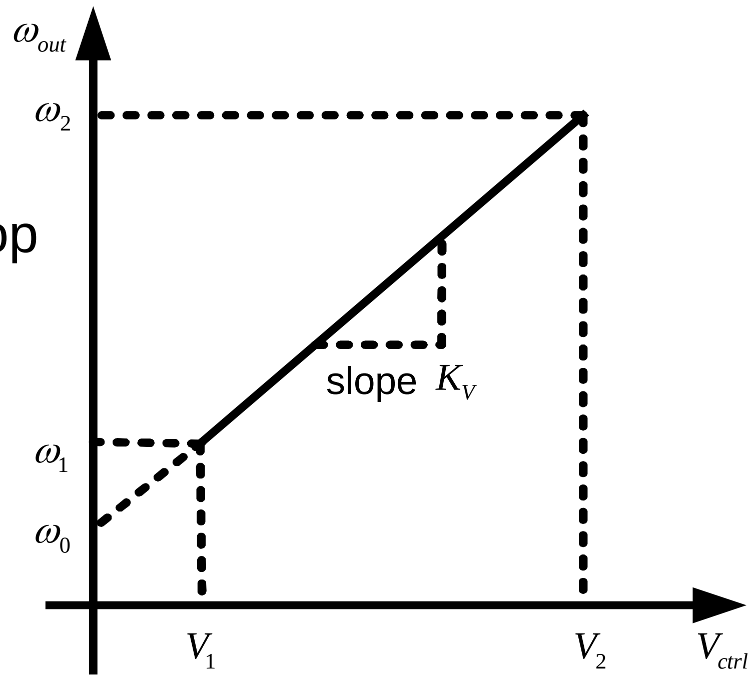
Mathematics of LC VCOs

F-V characteristic function

$$\omega_{out} = \omega_0 + K_V \cdot V_{ctrl}$$

An ideal integrator in Phase-Locked Loop

$$\frac{\phi_{ex}}{V_{ctrl}}(s) = \frac{K_V}{s}$$

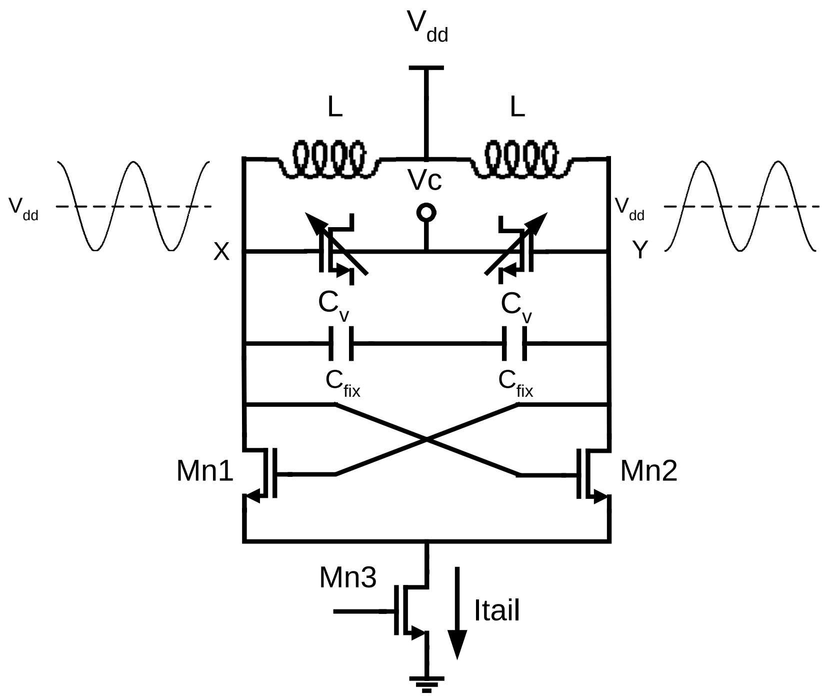


Performance parameters

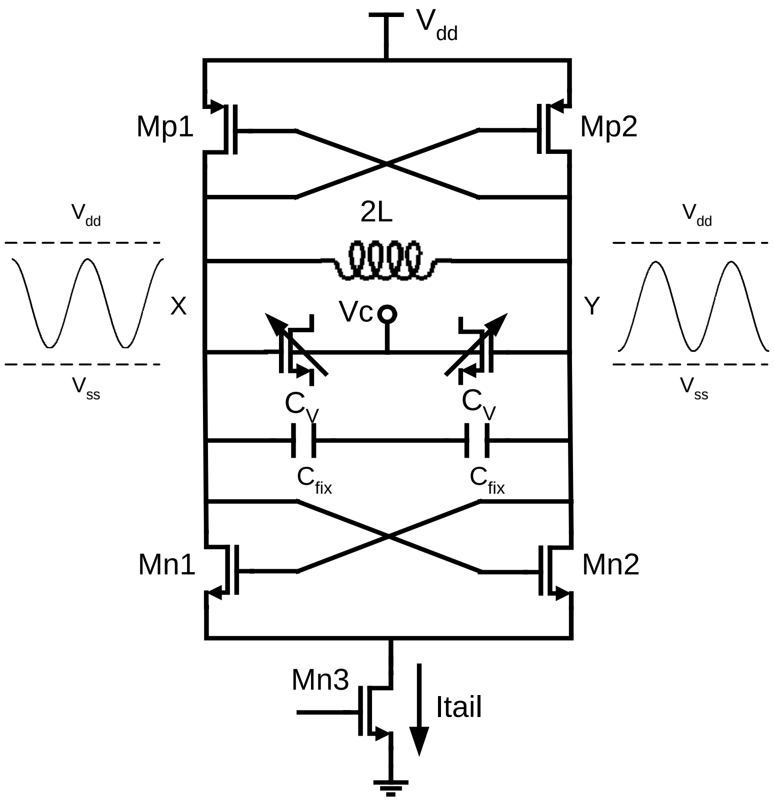
- Center frequency
- Tuning range
- Voltage-controlled gain
- Tuning linearity
- Phase noise
- Oscillating amplitude
- Power dissipation

Narrowband LC VCOs

NMOS-only $-G_m$ LC VCO



Complementary MOS $-G_m$ LC VCO



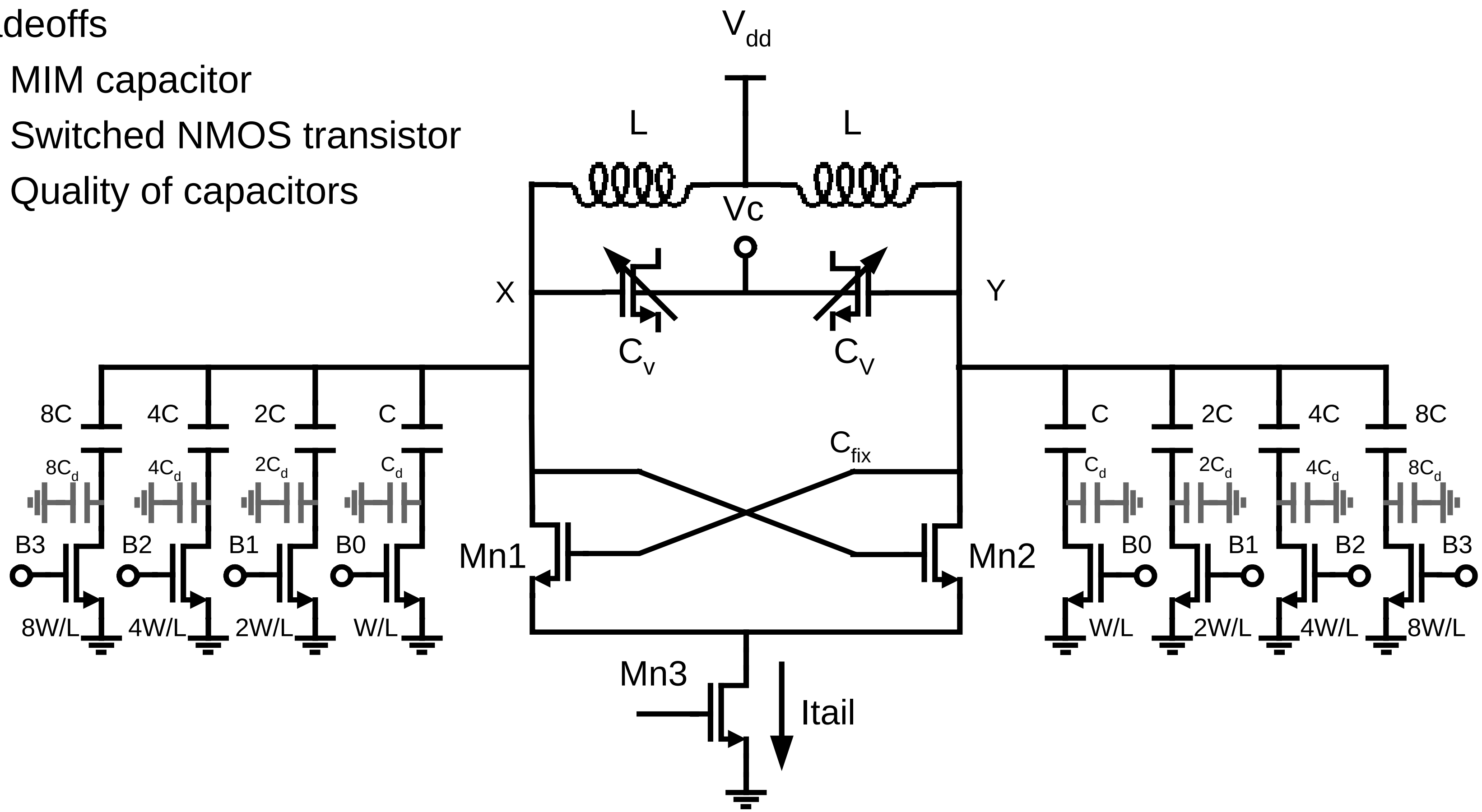
[Ali Hajimiri, JSSC, May, 1999]

Wideband LC VCOs

Wideband LC VCO with Switched Capacitors

Tradeoffs

- MIM capacitor
- Switched NMOS transistor
- Quality of capacitors

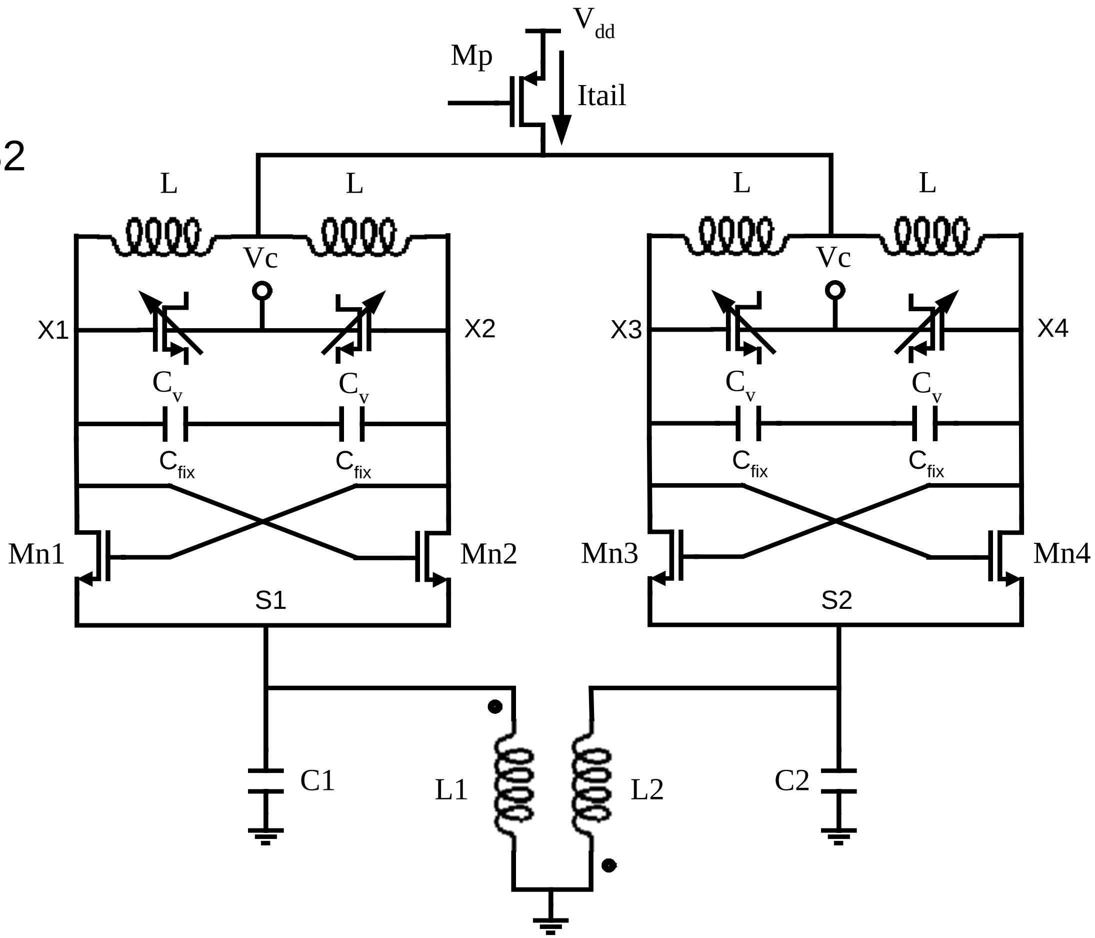


[A, Kral, A.A. Abidi, CICC, 1998]

Quadrature LC VCOs

Quadrature LC VCO with Superharmonic coupling

- Superharmonic coupling
  at Common-mode, S1 & S2
- Very simple
  two same LC-VCOs
- Low phase noise
- Low power dissipation



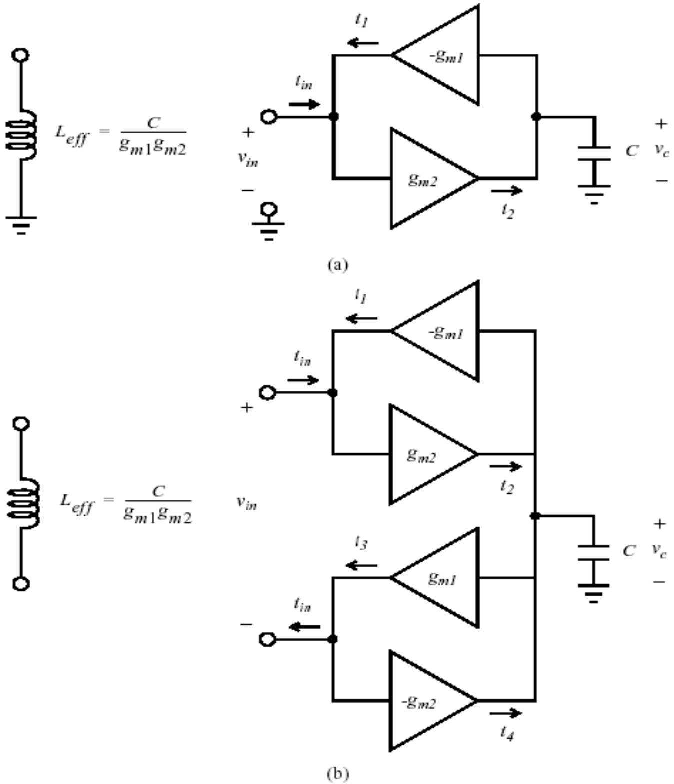
[S. L. J. Gierkink, JSSC, July, 2003]

Outline

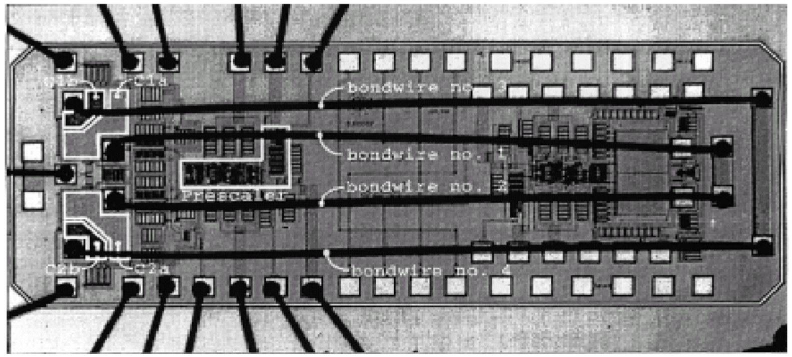
- Introduction
- Fundamentals of LC VCOs
- On-chip inductors
  - Inductor's Class
  - Modeling of on-chip inductors
  - Optimization of equivalent capacitance
  - Quality Factor improvement
- Varactors and F-V tuning curve
- Optimization of LC VCOs
- Techniques of lowering phase noise
- Design examples
- Conclusion and prospect

Inductor's Class

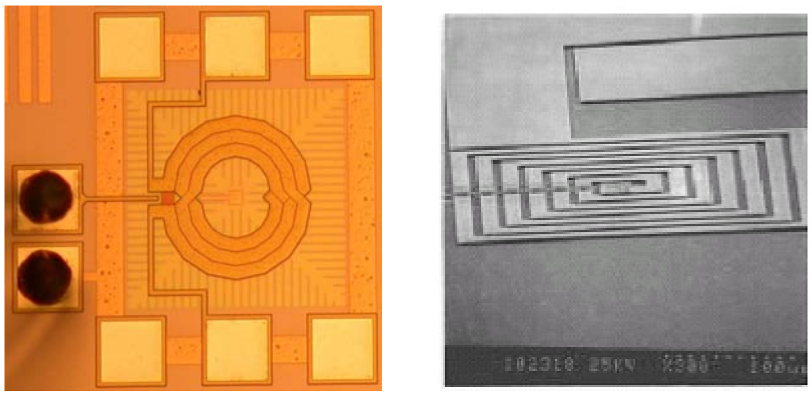
Three types of On-chip inductors



Gyrator-based active inductors
(a) single-ended，(b) floating configurations



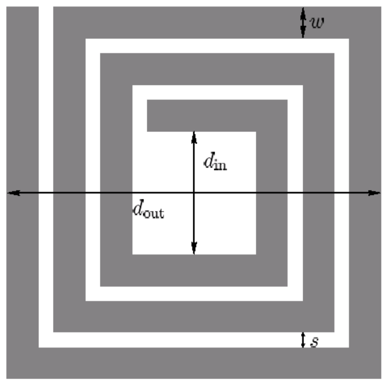
Bondwire inductors



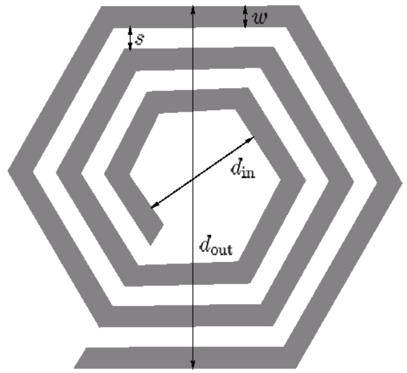
On-chip spiral inductors

Planar Spiral Inductor

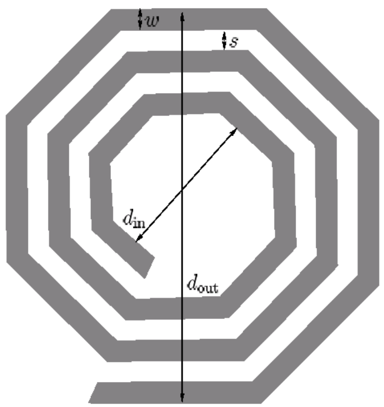
- Number of tuners, n
- Metal width, w
- Spacing, s
- Outer diameter, d_{out}
  Inner diameter, d_{in}
  Fill ratio, $\rho = (d_{out} - d_{in}) / (d_{out} + d_{in})$
- Number of sides, N



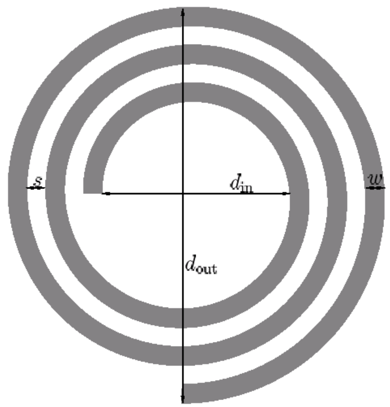
(a) Square Spiral



(b) Hexagonal Spiral



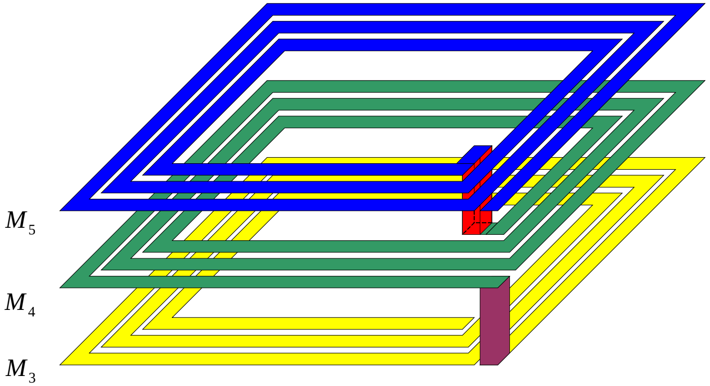
(c) Octagonal Spiral



(d) Circular Spiral

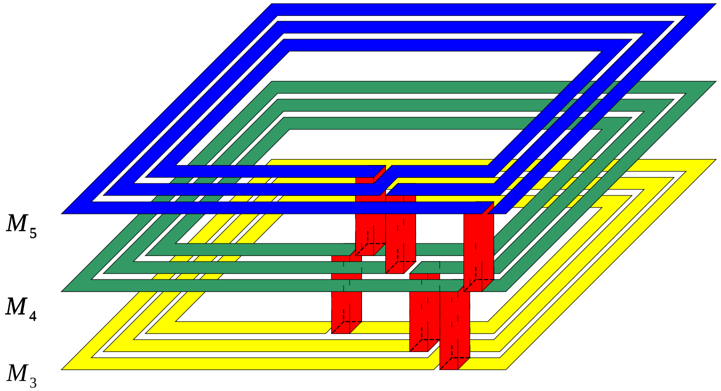
Multilayer Spiral Inductor

Stacked spiral inductor



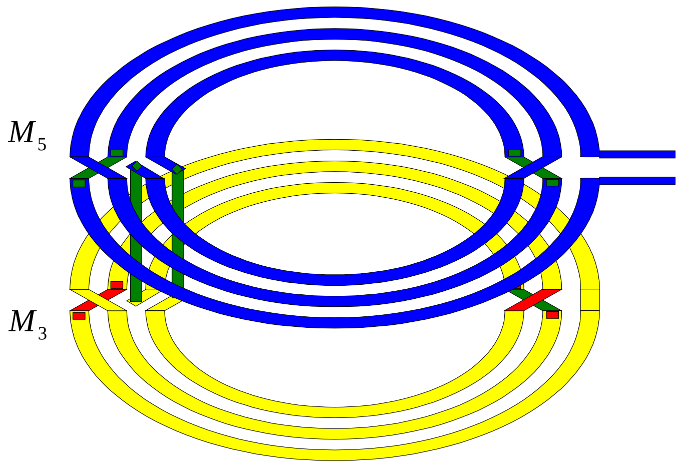
[A. Zolfaghari, B. Razavi, JSSC, April, 2001]

Miniature 3D spiral inductor



[C.C Tang, S.I. Liu, JSSC, April, 2002]

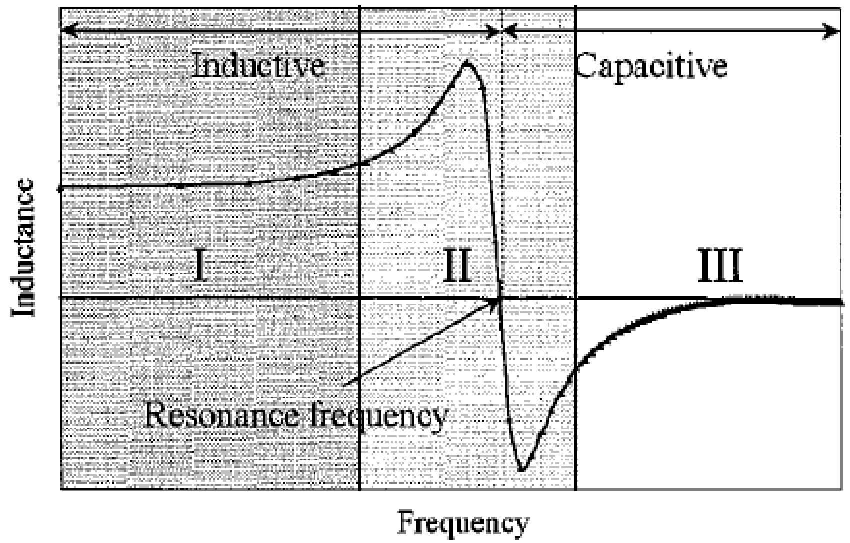
Differential multilayer inductor



Modeling of On-chip Inductors

- EM Field Solver
  - High accuracy
  - Very slow
  - Complex for Spice
- Segmental circuit models
  - Simpler than EM field solver
  - Easy integration into Spice
- Compact, scalable, lumped circuit models
  - Simple, versatile and robust
  - Physical intuition

Characteristic of inductance of a typical integrated inductors with frequency



Optimization of Equivalent Capacitance

- What is the equivalent capacitance
  - ❖ At resonance frequency, the peak magnetic and electric energies are equal.
  - ❖ Given a peak voltage V_0, electric energy is $C_{eq}V_0^2/2$

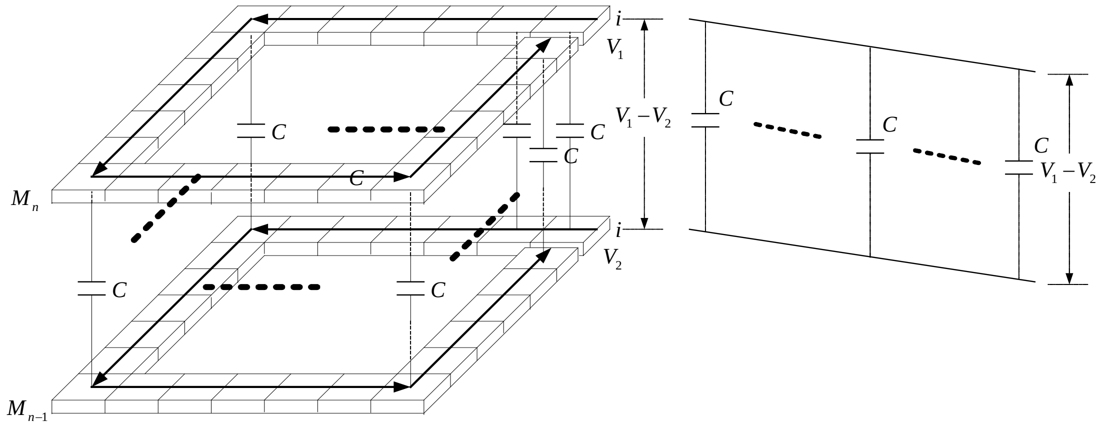
- First resonance frequency f_{SR}

$$f_{SR} = \left(2\pi\sqrt{L_{eq}C_{eq}}\right)^{-1}$$

- The proposed equivalent capacitance models
  - ❖ Electric energy in interlayer metals, $C_{M\text{-}M}$
  - ❖ Electric energy in single metal to substrate, $C_{M\text{-}S}$

Electric Energy in $C_{M\text{-}M}$ and $C_{M\text{-}S}$

$C_{M\text{-}M}$

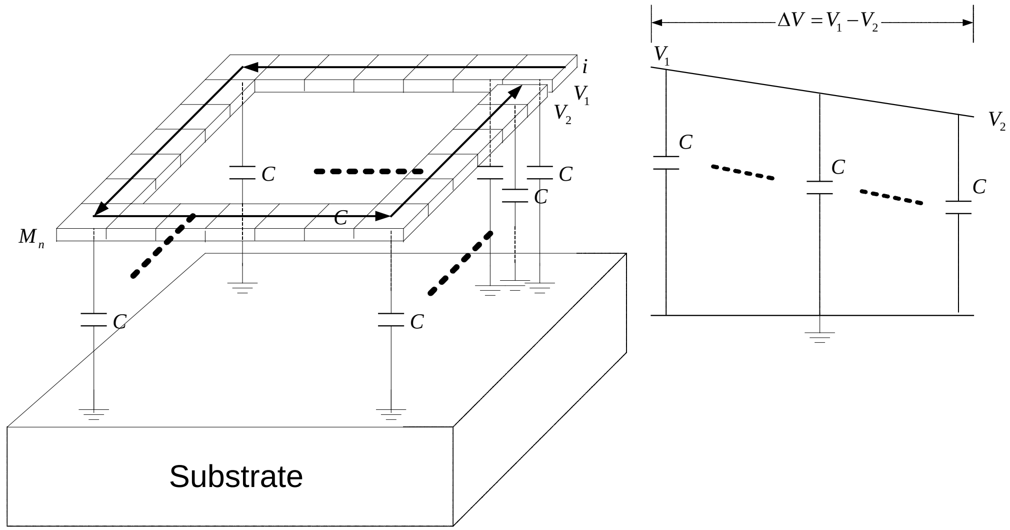


Electric Energy

$$E_{e,C}=\sum_{m=1}^{N}E_{e,C_m}=\sum_{m=1}^{N}\frac{1}{2}C_m V_{C_m}^2$$

$$=\frac{1}{2}C_{M_n-M_{n-1}}wl(V_1-V_2)^2$$

$C_{M\text{-}S}$



Electric Energy

$$E_{e,C}=\sum_{m=1}^{N}E_{e,C_m}=\sum_{m=1}^{N}\frac{1}{2}C_m V_{C_m}^2$$

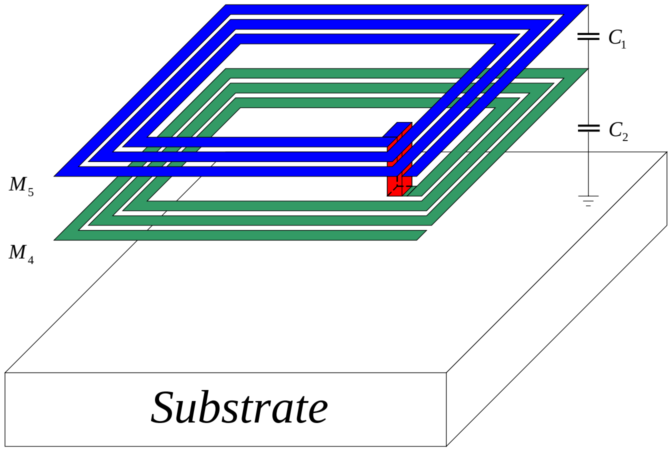
$$=\sum_{m=1}^{N}\frac{1}{2}\frac{C_{M_n-S}wl}{N}\left(V_1-\frac{m}{N}\Delta V\right)^2$$

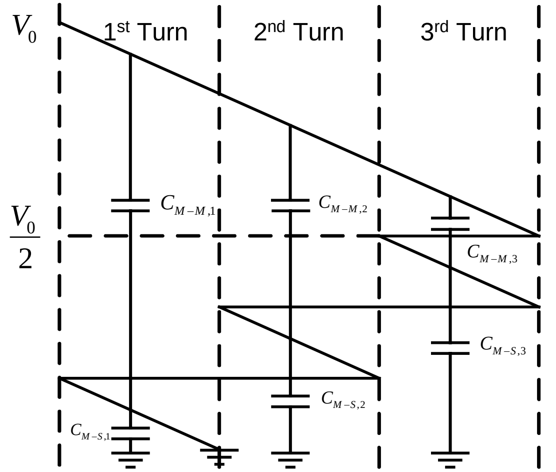
$$\overset{N\to\infty}{\approx}\frac{1}{6}C_{M_n-S}wl\left\{V_1^2+V_2^2+V_1V_2\right\}$$

Voltage Profile

[A. Zolfaghari, B. Razavi, JSSC, April, 2001]

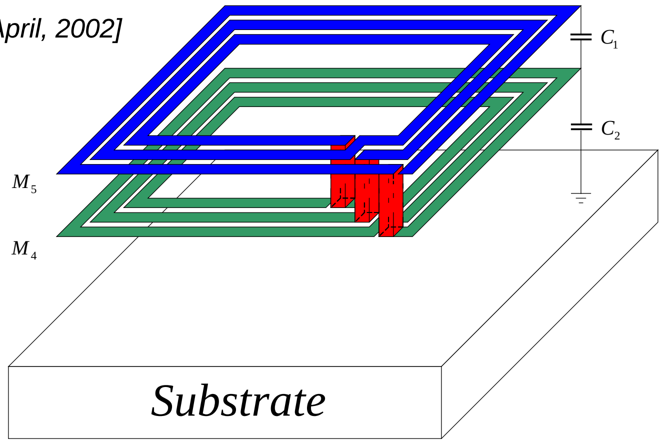
Stacked

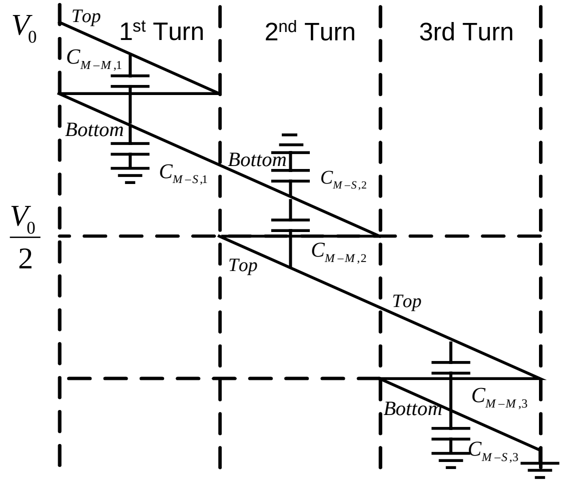




[C.C Tang, S.I. Liu, JSSC, April, 2002]

Miniature 3D



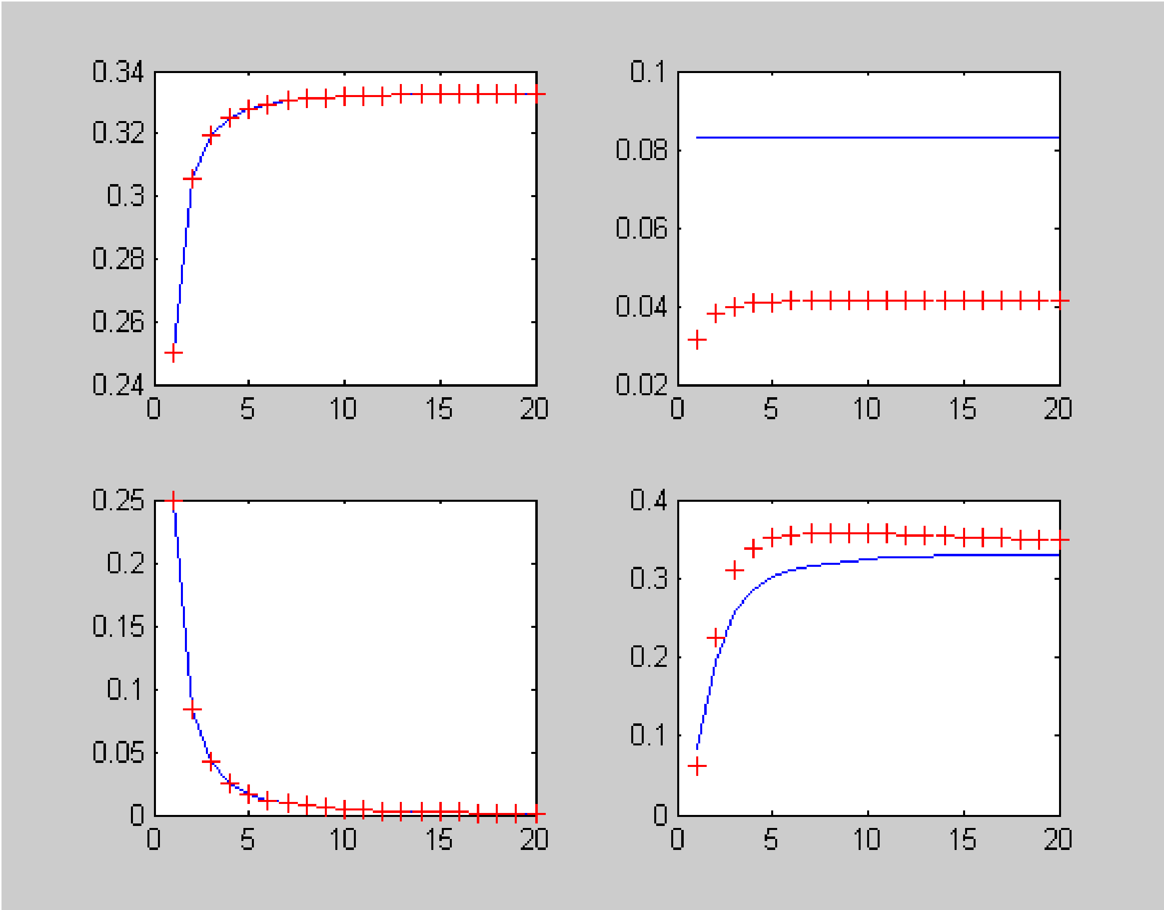


Capacitance Coefficients $C_{eq} = \kappa_1 C_1 + \kappa_2 C_2$

κ_1 κ_2

Stacked

Miniature 3D

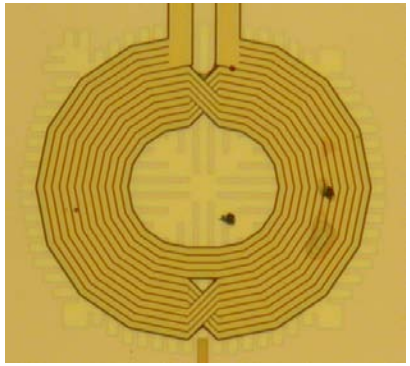


- Higher f_{SR}
- Small Area
- 3D or Stacked

Quality Factor Improvement

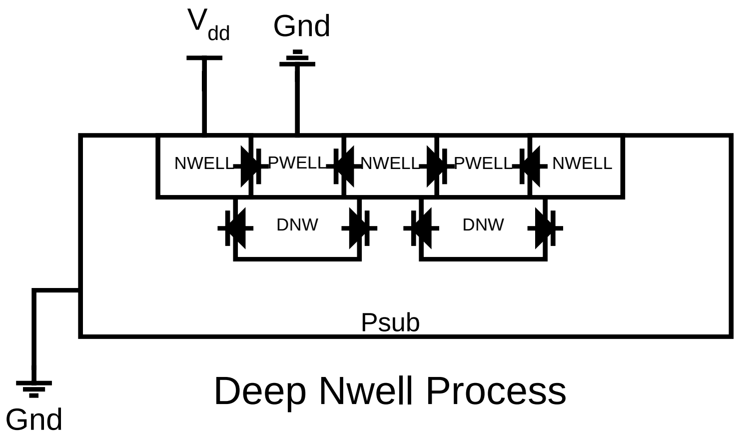
- Pattern ground shield

- Multipath metal



- Dual reverse-bias PN-junction isolation in deep Nwell

  Stop eddy current in skin channel



Deep Nwell Process

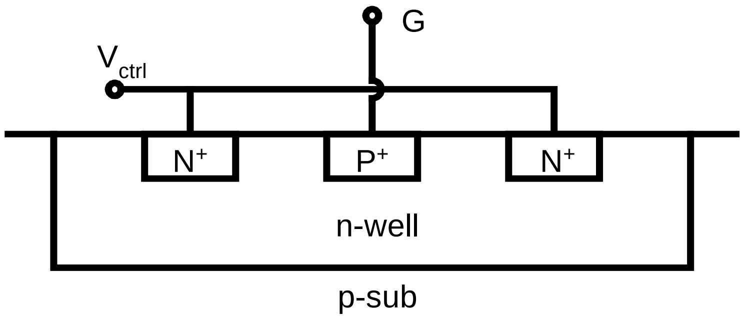
Outline

- Introduction
- Fundamentals of LC VCOs
- On-chip inductors
- Varactors and F-V tuning curve
  - Varactors' class
  - Period calculation of LC VCO with step-like varactors
- Optimization of LC VCOs
- Techniques of lowering phase noise
- Design examples
- Conclusion and prospect

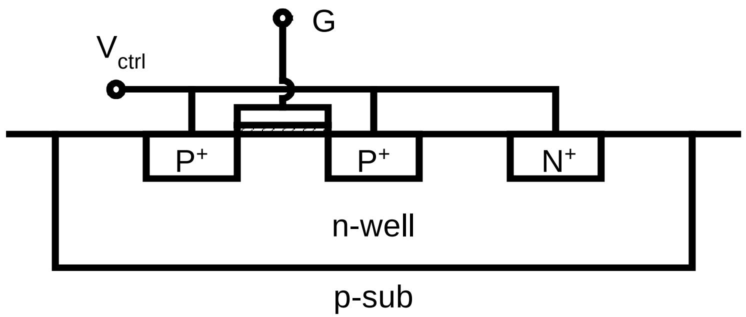
Varactors' Class

- Four Types of Varactors in Silicon CMOS:

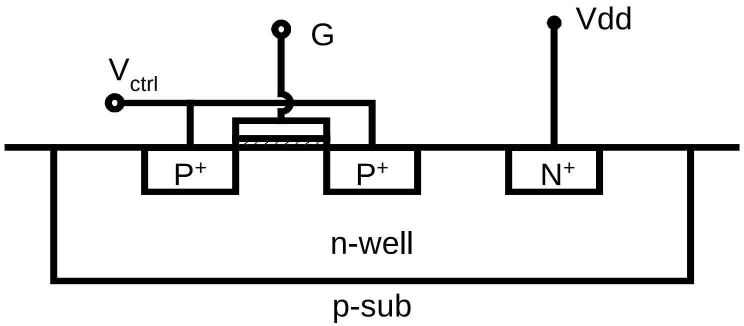
  PN Junction, Standard MOS, Inversion-MOS, Accumulation-MOS



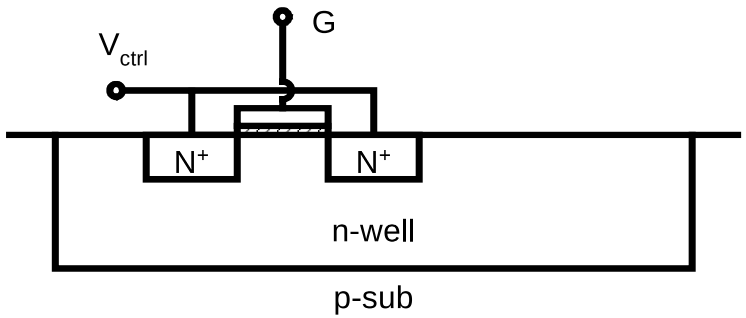
(a) p+/n-well Junction



(b) D=S=B MOS

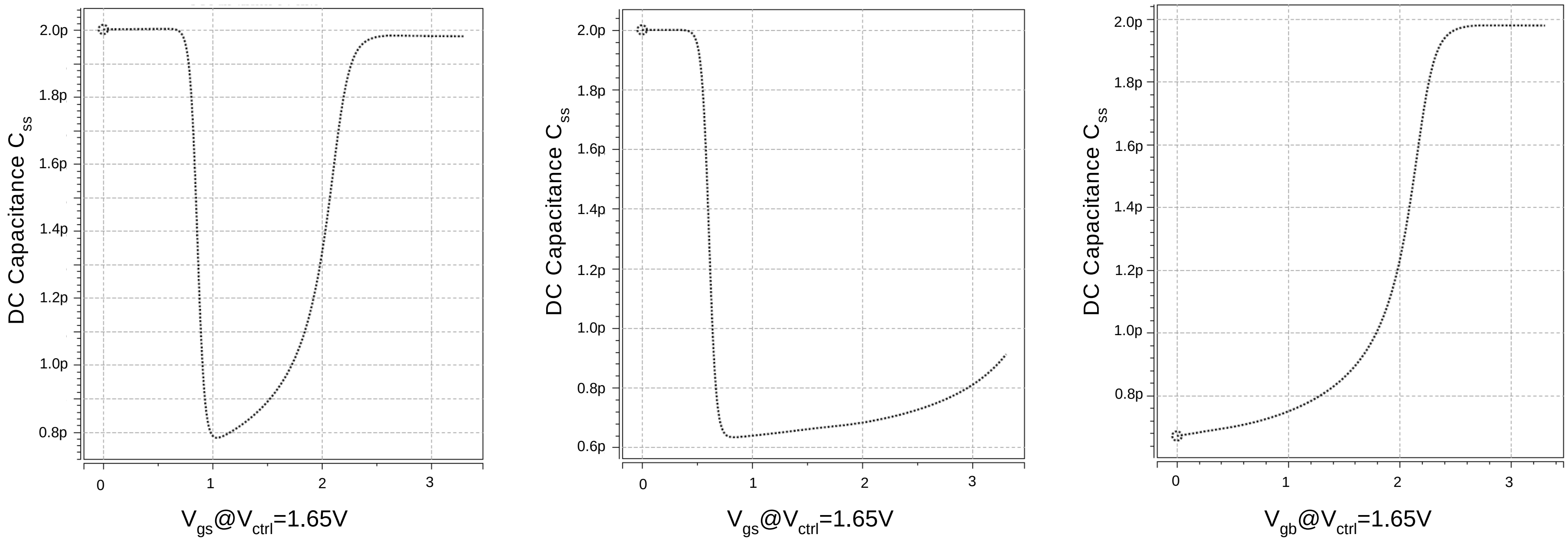


(c) Inversion MOS



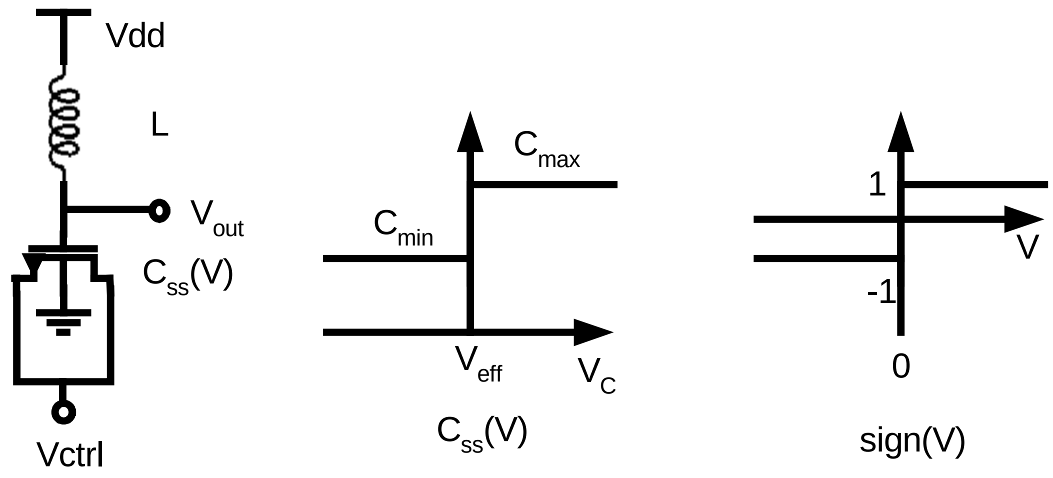
(d) Accumulation MOS

DC Capacitance of MOS Varactors



(a) S=D=B PMOS Varactor (b) Inversion PMOS Varactor (c) Accumulation NMOS Varactor

Step-like Varactors



(a) Serial LC Tank (b) Step-like Varactor (c) Unit Step Function

- Small-signal capacitance of step-like varactors

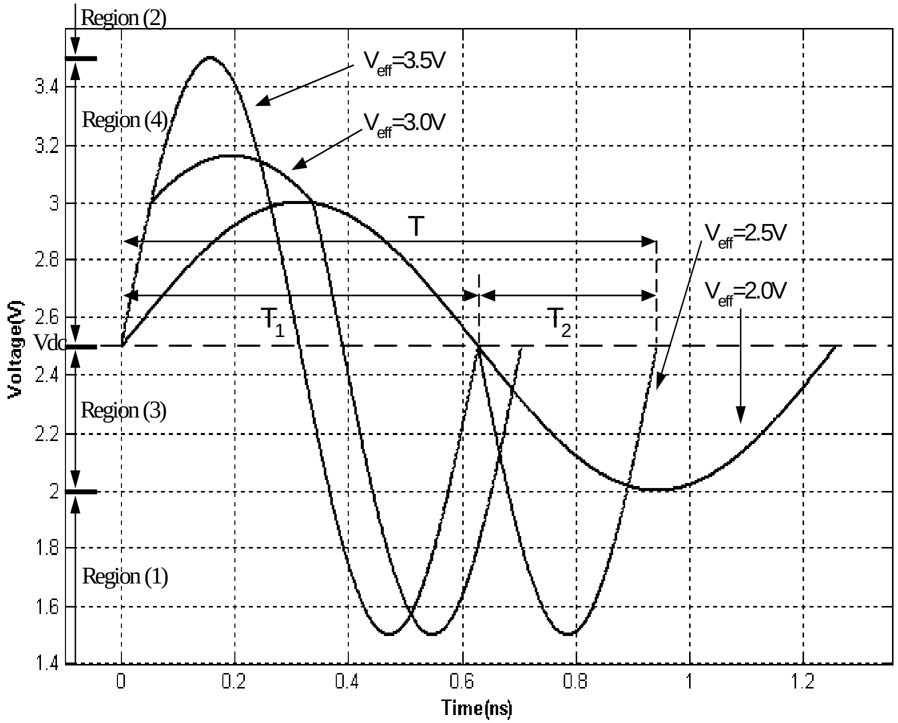
$$C_{ss}(V) = \begin{cases} C_{max} & V \geq V_{eff} \\ C_{min} & V \leq V_{eff} \end{cases}$$

- Effective control voltage $V_{eff} = V_G - V_{ctrl} - V_{TH}$

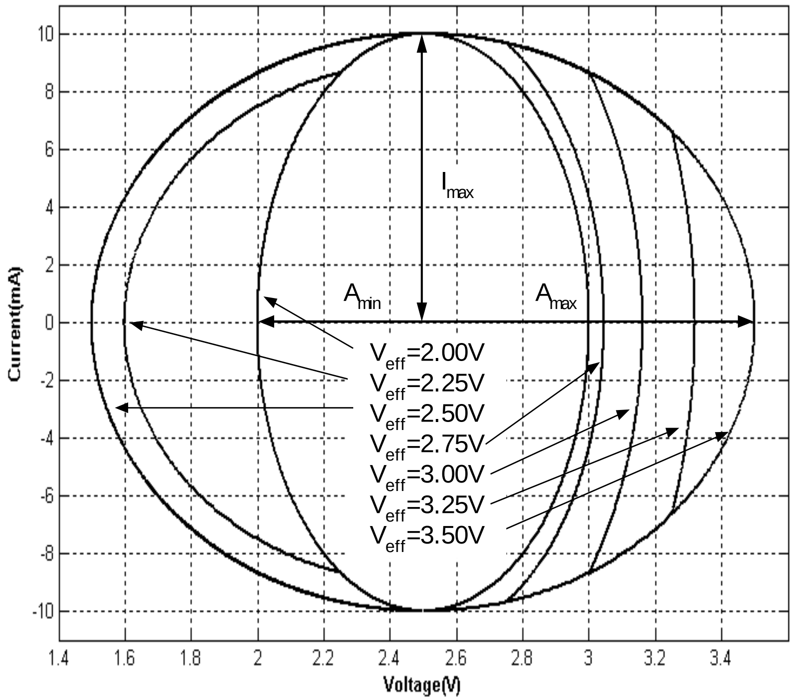
$$C_{ss}(V) = \frac{1}{2}(C_{max} + C_{min}) + \frac{1}{2}(C_{max} - C_{min})sign(V - V_{eff})$$

Oscillating Waveforms in LC-Tank

Oscillating waveforms at different V_{eff}



I-V locus of Step-like varactor

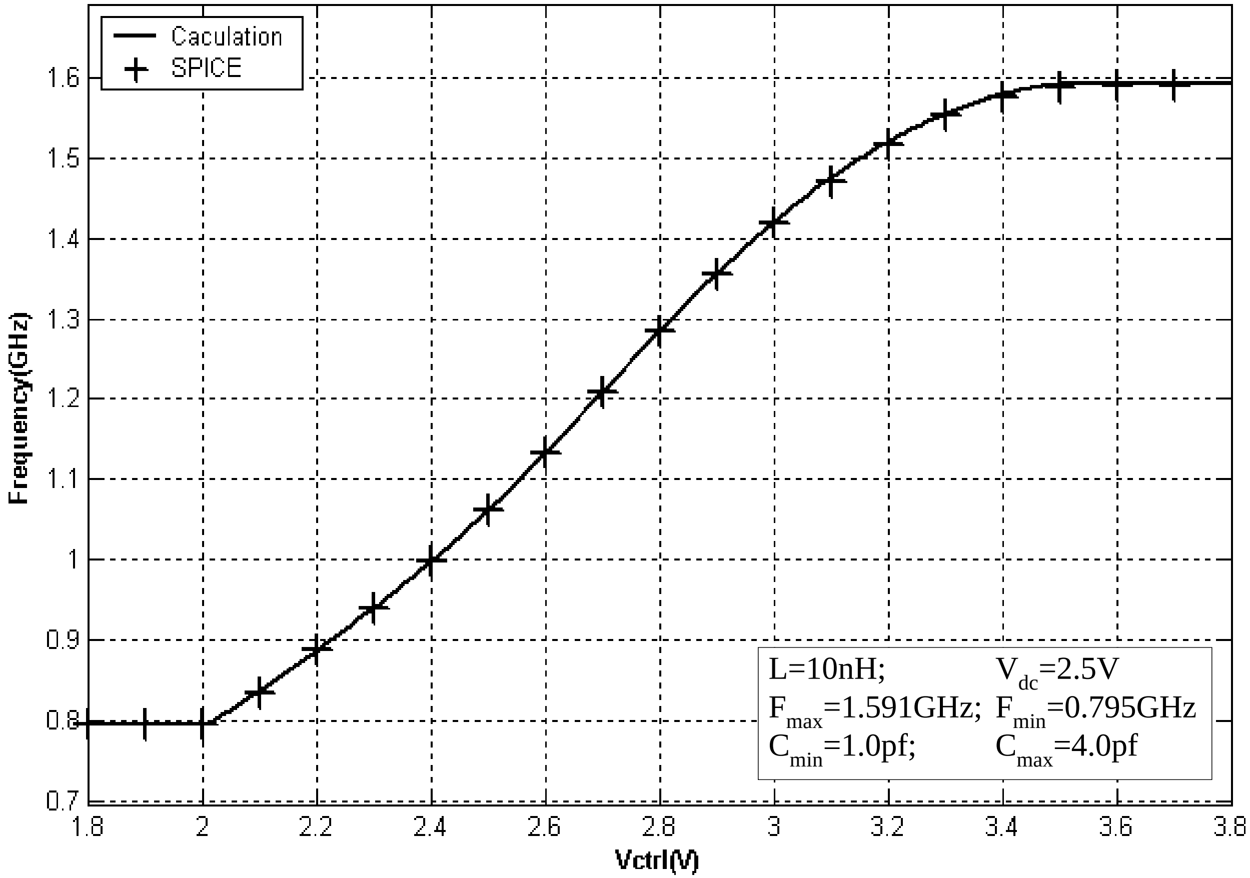


Two ellipses of different sizes joint with a step transition at V_{eff}

Oscillating Period Calculation

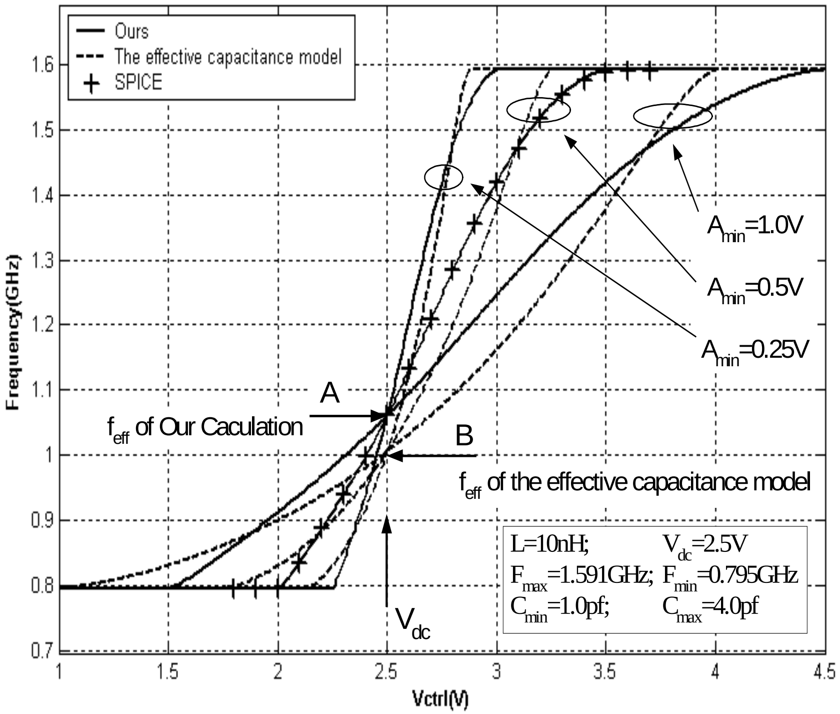
Effective Control Voltage, V_{eff}	*Oscillating Period of LC Tank*
$V_{eff}<V_{vdd}-A_{min}$	$T=T_{max}=2\pi\sqrt{LC_{max}}$
$V_{eff}>V_{vdd}+A_{max}$	$T=T_{min}=2\pi\sqrt{LC_{min}}$
$V_{vdd}-A_{min}<V_{eff}<V_{vdd}$	$T=\frac{1}{2}(T_{max}+T_{min})+\frac{1}{\pi}\left(asin\left(\frac{\lvert V_{eff}\rvert}{A_{min}}\right)T_{max}-asin\left(\frac{\lvert V_{eff}\rvert}{\theta_1 A_{max}}\right)T_{min}\right)$ Ellipse Similar Factor $\theta_1=\sqrt{1-\left(\frac{V_{eff}}{A_{min}}\right)^2+\left(\frac{V_{eff}}{A_{max}}\right)^2}$
$V_{vdd}<V_{eff}<V_{vdd}+A_{max}$	$T=\frac{1}{2}(T_{max}+T_{min})+\frac{1}{\pi}\left(-asin\left(\frac{V_{eff}}{\theta_2 A_{min}}\right)T_{max}+asin\left(\frac{V_{eff}}{A_{max}}\right)T_{min}\right)$ Ellipse Similar Factor $\theta_2=\sqrt{1-\left(\frac{V_{eff}}{A_{max}}\right)^2+\left(\frac{V_{eff}}{A_{min}}\right)^2}$

Simulation Verification in HSPICE



Simulation agrees well with the proposed calculation

Comparison with Others' Model



Hegazi's effective capacitance model

$$C_{eff} = \frac{1}{2}(C_{max} + C_{min}) + \frac{1}{\pi}(C_{min} - C_{max})\left(asin\left(\frac{V_{eff}}{A}\right) + \left(\frac{V_{eff}}{A}\right)\sqrt{1 - \left(\frac{V_{eff}}{A}\right)^2} \right)$$

- Point A $$F_{eff,A} = \frac{2F_{min} \cdot F_{max}}{F_{min} + F_{max}}$$
- Point B $$F_{eff,B} = \frac{\sqrt{2}F_{min} \cdot F_{max}}{\sqrt{F_{min}^2 + F_{max}^2}}$$

$$F_{eff,B} \le F_{eff,A}$$

The reasons for difference between two method:

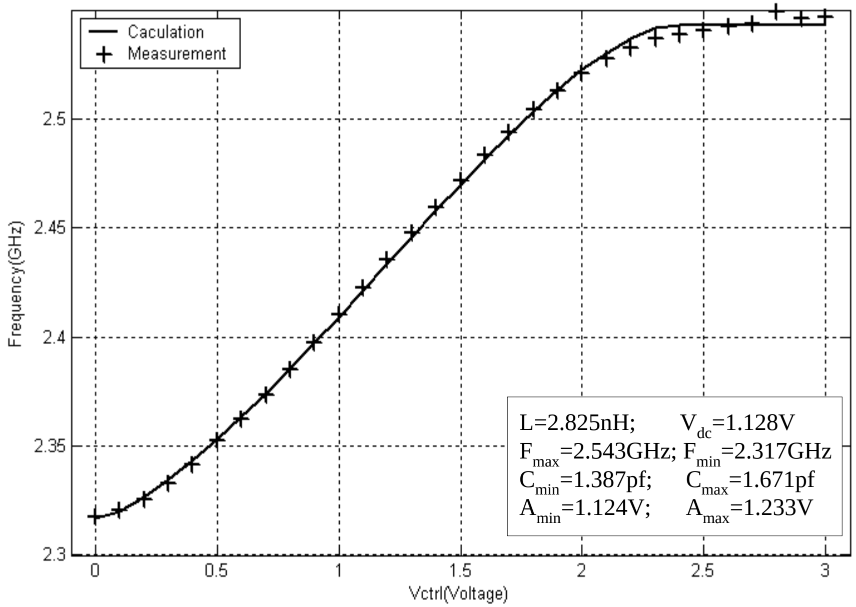
a) Hegazi's model is small-signal analysis;

b) Neglect 2rd and higher order harmonics;

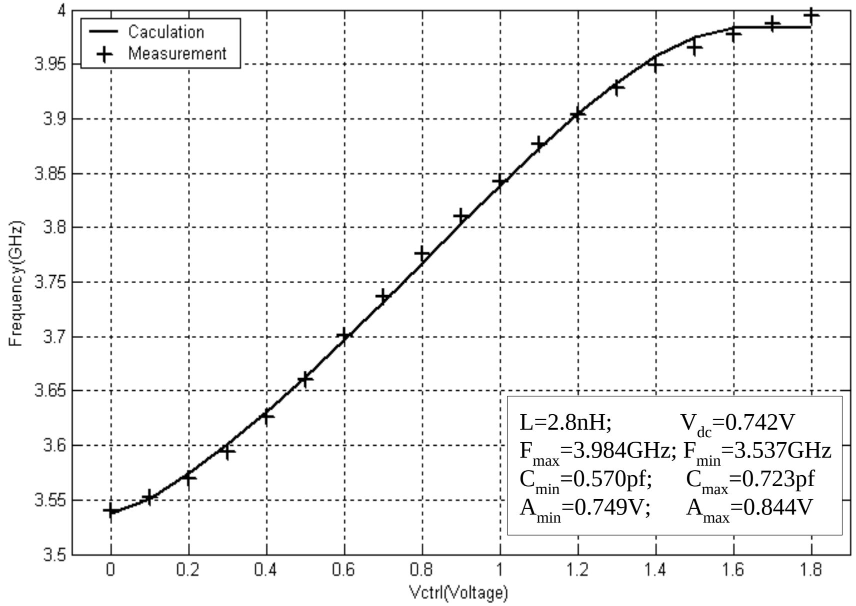
[E. Hegazi, A.A. Abidi, JSSC, June, 2003]

Validation with Others' LC-VCOs

Frequency-Voltage Curves



[Y.B. Choi, 5th ASICON, 2003]



[H.L.Lao, 5th ASICON, 2003]

Outline

- Introduction
- Fundamentals of LC VCOs
- On-chip inductors
- Varactors and F-V tuning curve
- Optimization of LC VCOs
  - Low power design and low phase noise
  - Underlying physics of LC oscillators
  - Optimization method: Linear and Geometric Programming
- Techniques of lowering phase noise
- Design examples
- Conclusion and prospect

Low-power Design

- Energy Conservation Theorem

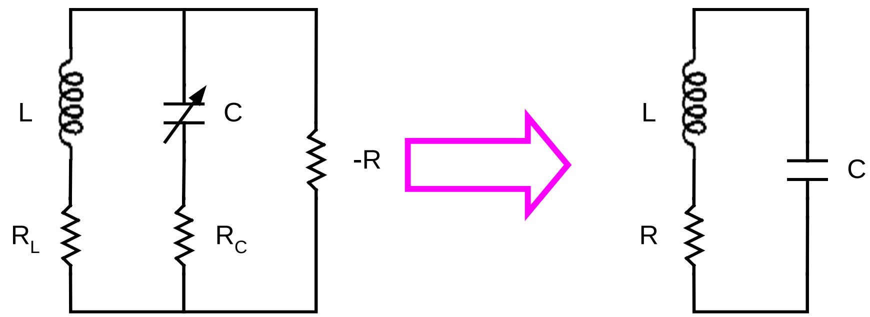
$$\frac{CV_{peak}^2}{2} = \frac{LI_{peak}^2}{2}$$

- The loss in RLC tank

$$P_{loss} = RC^2\omega_0^2 V_{peak}^2 = \frac{R}{L^2\omega_0^2} V_{peak}^2$$

- Low-power design
  - ❖ Lower serial resistance R
  - ❖ Increase the tank inductance
  - ❖ Work at high frequency

RLC Tank



$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$$Q_{tank} = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 CR} = \frac{1}{R}\sqrt{\frac{L}{C}}$$

[M. Tiebout, JSSC, Jul. 2001]

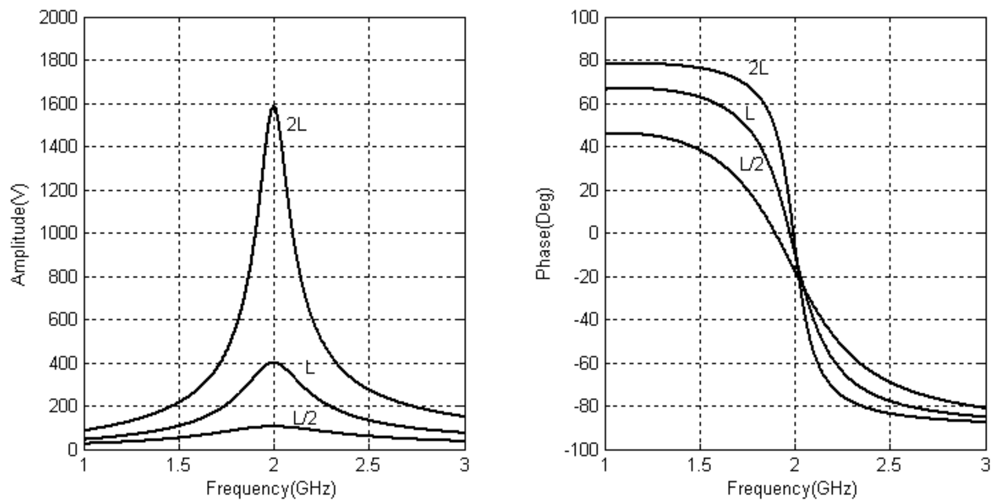
Low-phase-noise Design

- Phase noise (SSCR)

$$L(\Delta\omega) \propto \frac{KT}{2P_{sig}} \frac{\omega_0^2}{Q^2 \Delta\omega^2}$$

$$\Big\downarrow\ Q_{tank}$$

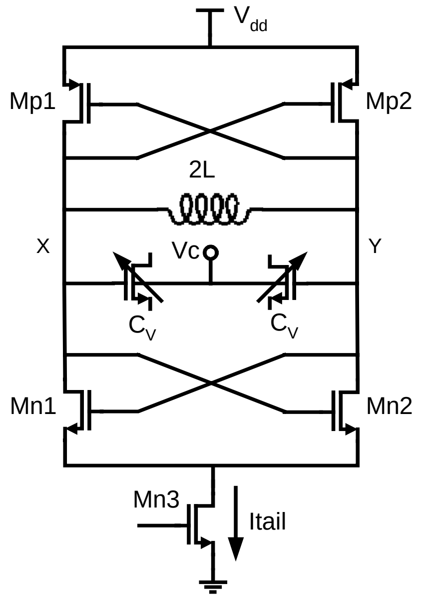
$$L(\Delta\omega) \propto \frac{KT}{V_{peak}^2} \frac{R^3}{L^2 \Delta\omega^2}$$

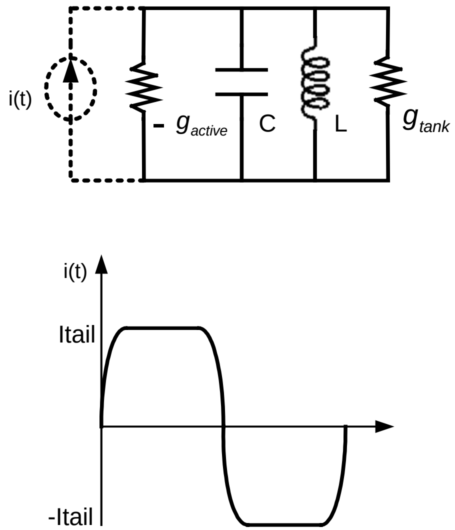


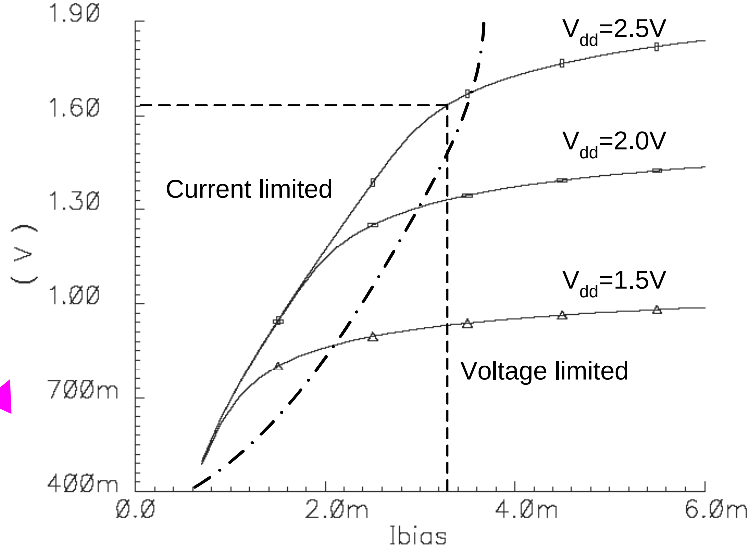
- Low-phase-noise design
  - Lower serial resistance R
  - Increase the tank inductance
  - Increase amplitude voltage

$$Q_{tank} = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 CR} = \frac{1}{R}\sqrt{\frac{L}{C}}$$

Underlying Physics of LC Oscillators

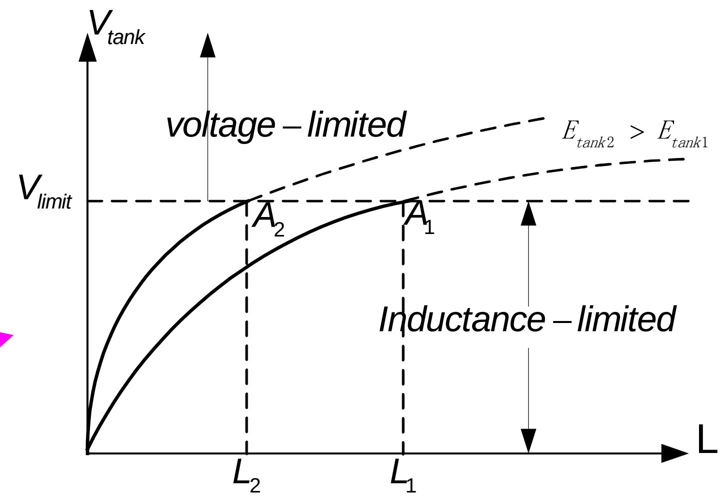






$$V_{tank} = \begin{cases} (4/\pi) I_{bias} / g_{tank} & (I-limited) \\ V_{limit} & (V-limited) \end{cases}$$

$$V_{tank} = \begin{cases} \sqrt{2E_{tank}\omega_0^2 L} & (L-limited) \\ V_{limit} & (V-limited) \end{cases}$$



[A. Hajimiri, JSSC, May 1999]

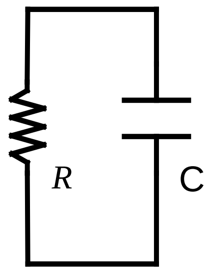
Noise-to-Carrier Rate, NCR

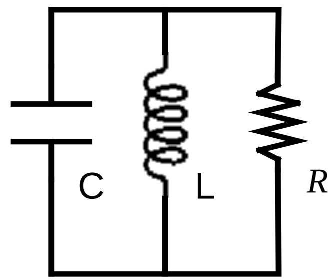
The equipartition theorem of thermodynamics states that:

Any system in equilibrium has a mean energy of KT/2

$$C\langle v_n^2\rangle /2 = KT/2$$

$$\langle v_n^2\rangle = \frac{KT}{C} = KT\omega_0^2 L$$



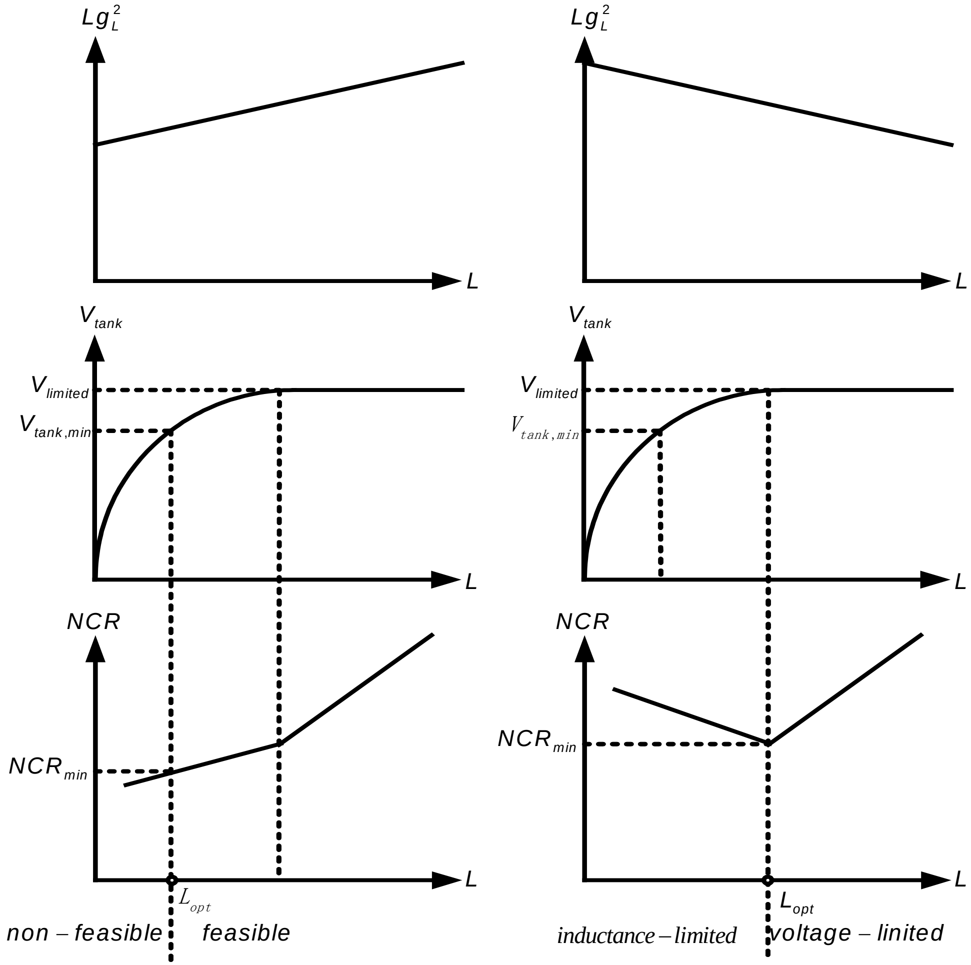


$$E_{tank} \propto I_{tail}^2 / Lg_{tank}^2 \approx I_{tail}^2 / Lg_L^2 \qquad (L-limited)$$

$$\frac{\langle v_n^2\rangle}{V_{tank}^2} \propto \begin{cases} 1/E_{tank} & (L-limited) \\ L & (V-limited) \end{cases} \rightarrow \frac{\langle v_n^2\rangle}{V_{tank}^2} \propto \begin{cases} Lg_L^2/I_{tail}^2 & (L-limited) \\ L & (V-limited) \end{cases}$$

[D. Ham and A. Hajimiri, JSSC, Jun. 2001]

Design Insight



(a) (b)

- Lg_L^2 ***increasing with L***

  Startup condition
  Minimum tank amplitude
  Optimization at feasible point

- Lg_L^2 ***descreasing with L***

  Optimization at the verge of inductance-limited and voltage-limited regime

LC VCO Topology

12 initial design variables

- MOS transistors

  $W_n \quad L_n \quad W_p \quad L_p$

- On-chip spiral inductors

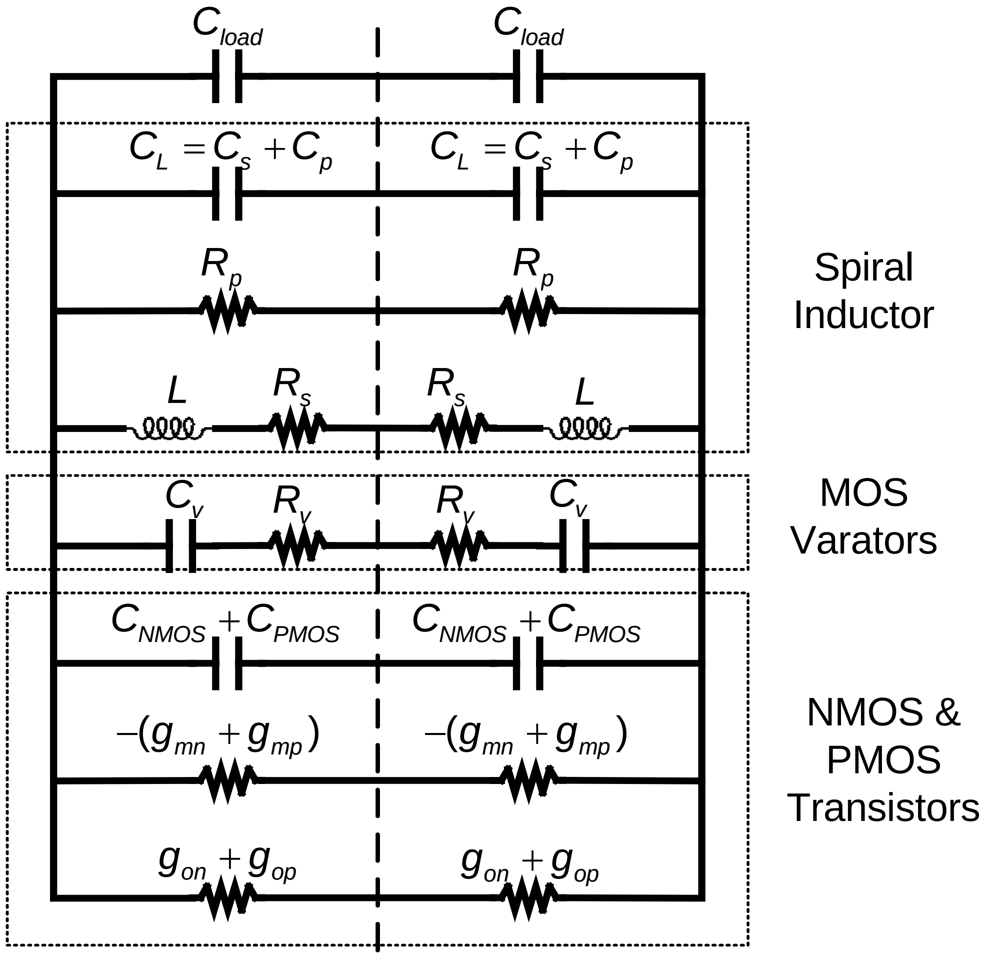
  $d_{out} \quad w \quad s \quad n$

- MOSCAP varators

  $C_{v,max} \quad C_{v,min}$

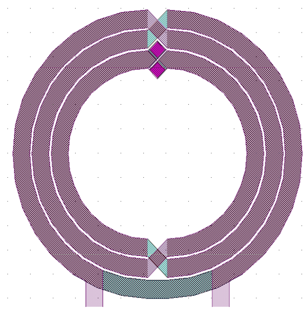
- Load cap and tail current

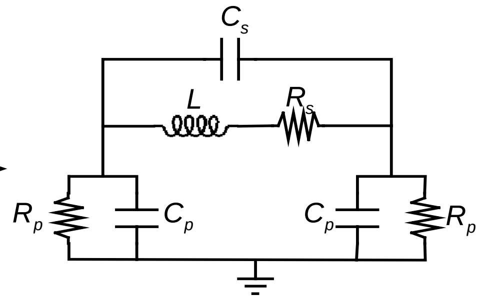
  $C_{load} \quad I_{tail}$



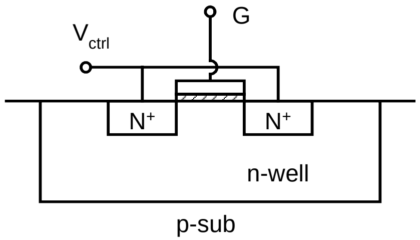
Equivalent oscillator model

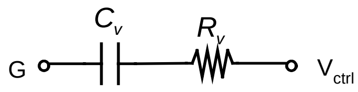
LC VCO Parameters





$$g_L = 1/R_p + R_s/(L\omega)^2$$





$$g_v = (C_v\omega)/Q_v$$

$$2g_{tank} = g_{on} + g_{op} + g_v + g_L \qquad 2g_{active} = g_{mn} + g_{mp}$$

$$L_{tamnk} = 2L \qquad 2C_{tank} = C_{PMOS} + C_{NMOS} + C_L + C_v + C_{load}$$

$$C_{NMOS} = C_{gs,n} + C_{db,n} + 4C_{gd,n} \qquad C_{PMOS} = C_{gs,p} + C_{db,p} + 4C_{gd,p}$$

Design Constraints

(1) Power dissipation

$$I_{tail} \le I_{max}$$

(2) Oscillator voltage amplitude

$$V_{tank} = \frac{I_{tail}}{g_{tank,max}} = \frac{2I_{tail}}{g_{on} + g_{op} + g_v + g_L} \approx \frac{2I_{tail}}{g_L} \ge V_{tank,min}$$

(3) Tuning range

$$L_{tamnk} C_{tank,min} \le \frac{1}{\omega_{max}^2} \quad L_{tank} C_{tank,max} \ge \frac{1}{\omega_{min}^2}$$

$$(\omega_{max} - \omega_{min})/\omega = r_{t,min} \quad (\omega_{max} + \omega_{min})/2 = \omega$$

(4) Startup condition

$$g_{active} \ge \alpha_{min} g_{tank,max}$$

(5) Maximum diameter of spiral inductor

$$d \le d_{max}$$

etc. …

Phase Noise Optimization

- In $1/f^2$ region, Phase noise (SSCR)

$$L\{\Delta\omega\} \propto \begin{cases} \dfrac{L^2 g_L^2}{I_{tail}} & (L-limited) \\ \dfrac{L^2 I_{tail}}{V_{sunpply}^2} & (V-limited) \end{cases}$$

$$Lg_L \approx L\left(R_s/(L\omega)^2\right) = \frac{R_s}{L\omega^2}$$

$$L\{\Delta\omega\} \propto \begin{cases} \left(\dfrac{R_s}{L}\right)^2 \cdot \dfrac{1}{\omega^4 I_{tail}} & (L-limited) \\ \dfrac{L^2 I_{tail}}{V_{sunpply}^2} & (V-limited) \end{cases}$$

[D. Ham, and A. Hajimiri, JSSC, 2001]

Proposed optimization equation

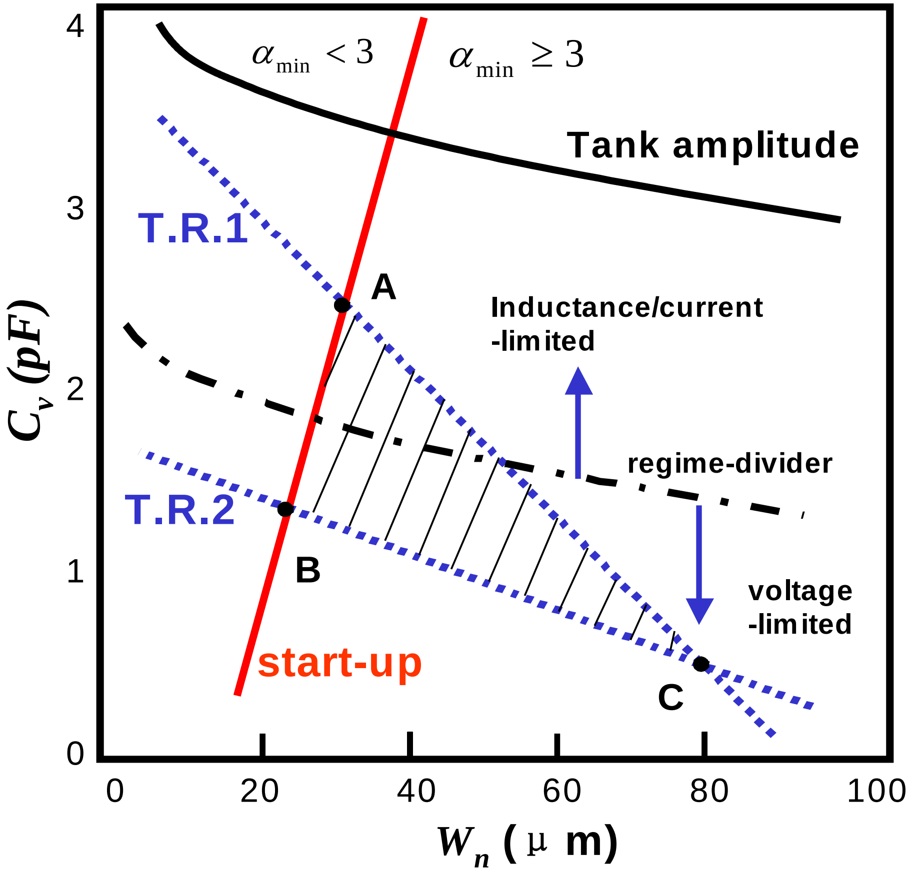
Design strategy

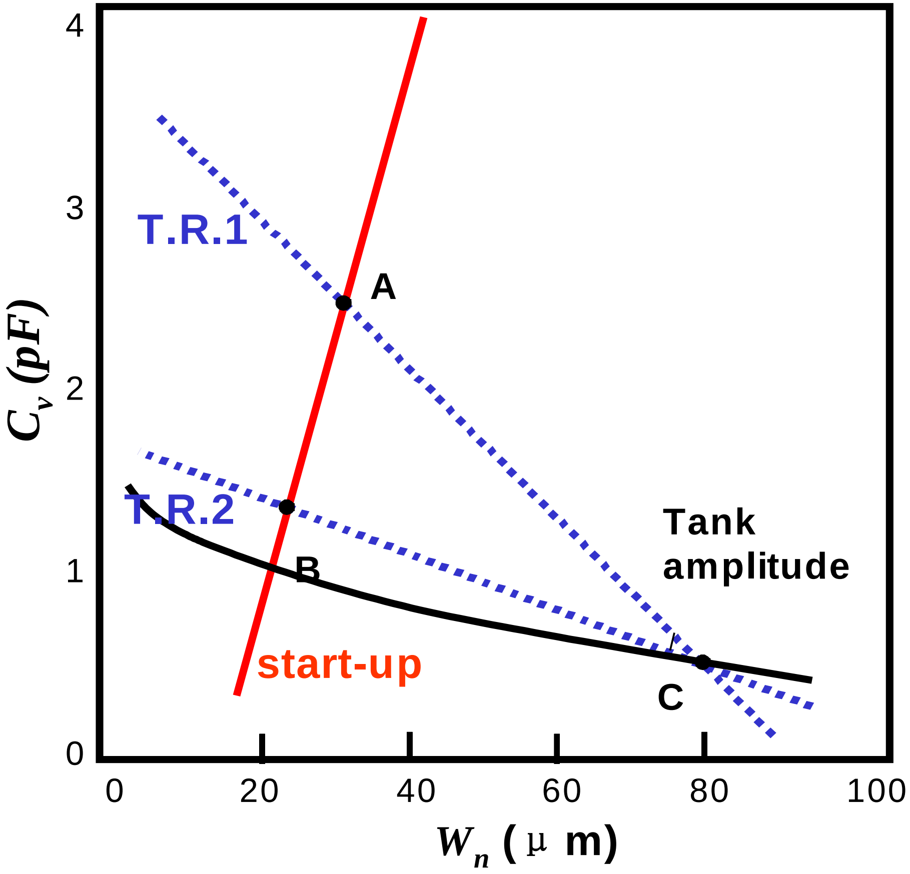
- Lower R_s/L of on-chip inductor, or select high Q_L inductor
- At maximum current I_{max}
- At verge of *inductance-limited* and *voltage-limited* regime

Graphical Optimization

Lower R_s/L in on-chip inductor,

Decrease or increase I_{tail}





Geometric Programming

- What?

a special form of optimization problem:

$$\begin{array}{ll} \text{minimize} & f_0(x) \\ \text{subject to} & f_i(x) \le 1, \quad i = 1, \dots, m \\ & g_i(x) = 1, \quad i = 1, \dots, p \\ & x_i > 0, \quad i = 1, \dots, n \end{array}$$

where f_i are posynomial and g_i are monomial

- Object Function: phase noise

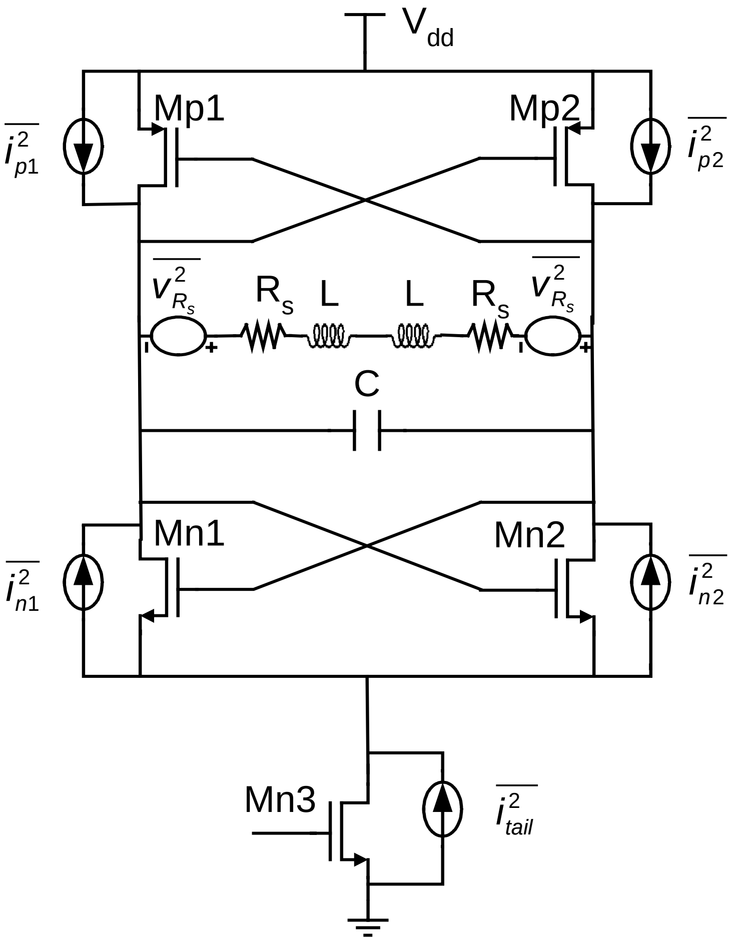
$$L\{\Delta\omega\} = 10 \cdot \log\left(\frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2 \cdot \Delta\omega^2} \right)$$

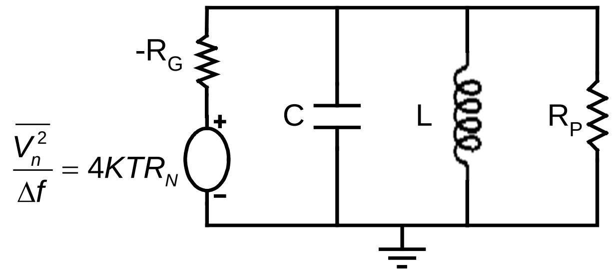
$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n cos(n\omega_0\tau + \theta_n) \qquad \sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma(x)|^2 dx = 2\Gamma_{rms}^2$$

Outline

- Introduction
- Fundamentals of LC VCOs
- On-chip inductors
- Varactors and F-V tuning curve
- Optimization of LC VCOs
- Techniques of lowering phase noise
  - Limited noise factor for white noise
  - Noise filtering techniques
  - Inductive control voltage
- Design examples
- Conclusion and prospect

Limited Noise Factor for White Noise





- Phase noise

$$L\{\Delta\omega\} = 10\cdot\log\left(\frac{\overline{v_{n,SSB}^2}/\Delta f \,\Big/ R_P}{P_{sig}}\right) = 10\cdot\log\left(F\frac{KT}{2P_{sig}Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right)$$

- Limited noise factor

$$F = \frac{R_N}{R_P} = \left(1 + \frac{\gamma_n + \gamma_p}{2}\right) = 1 + \gamma$$

[F. Herzel and M .Tiebout, TCASII, Jan. 2000]

Noise Sources of Close-in Phase Noise

- Flicker noise of tail current

  AM-FM modulation

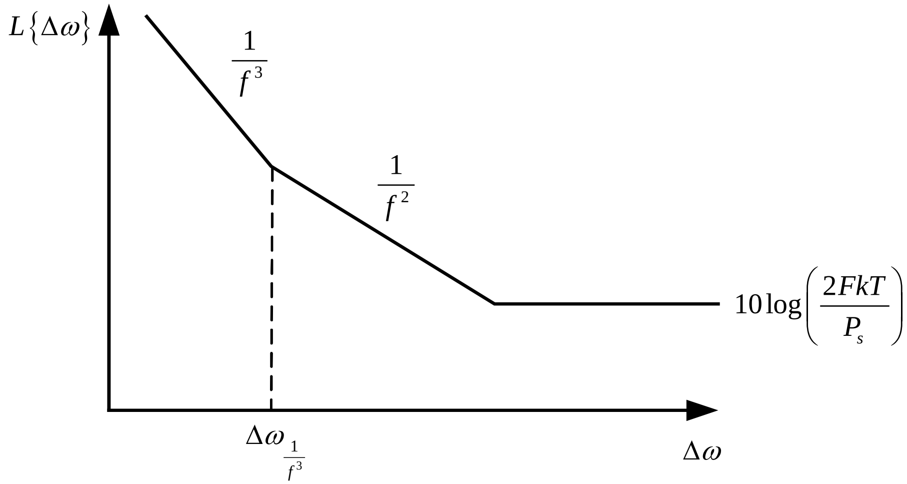
- Flicker noise of differential pairs

  Differential pairs looks like a “Mixer”.

  Flicker noise modulates the baseband and 2nd harmonics voltage at the tail.

- Varactor nonlinearity

  AM-FM modulation of common noise, power and substrate noise.

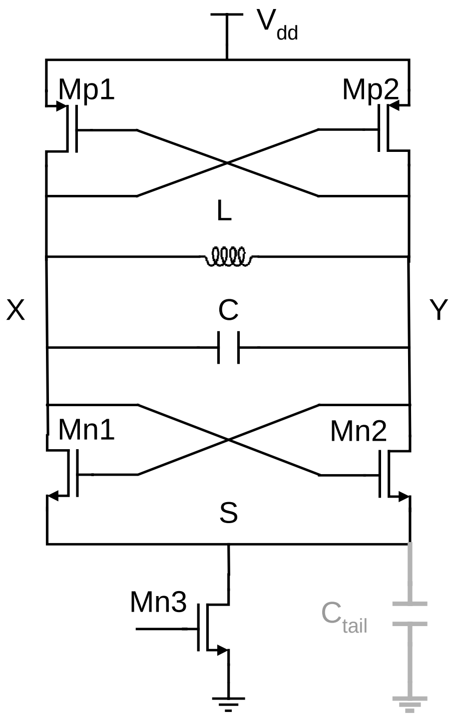


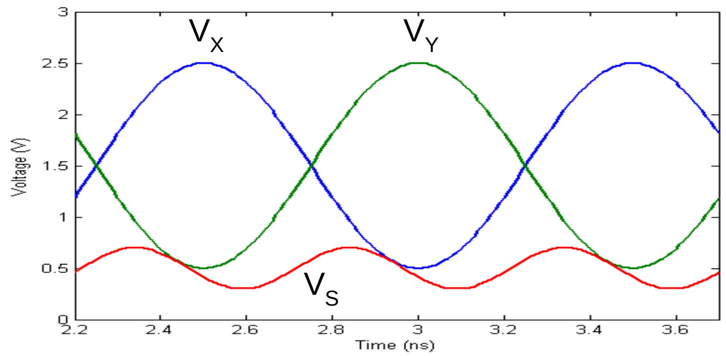
Leeson’s model

$$L\{\Delta\omega\} = 10\cdot\log\left\{\frac{2FkT}{P_s}\cdot\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\}$$

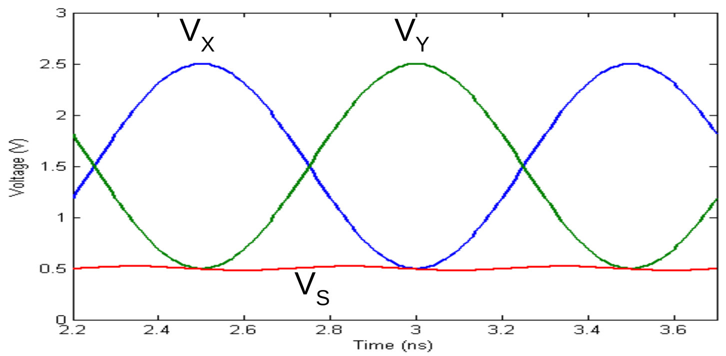
Noise Filtering Techniques (1)

Large capacitor filter at common node





Without large capacitor



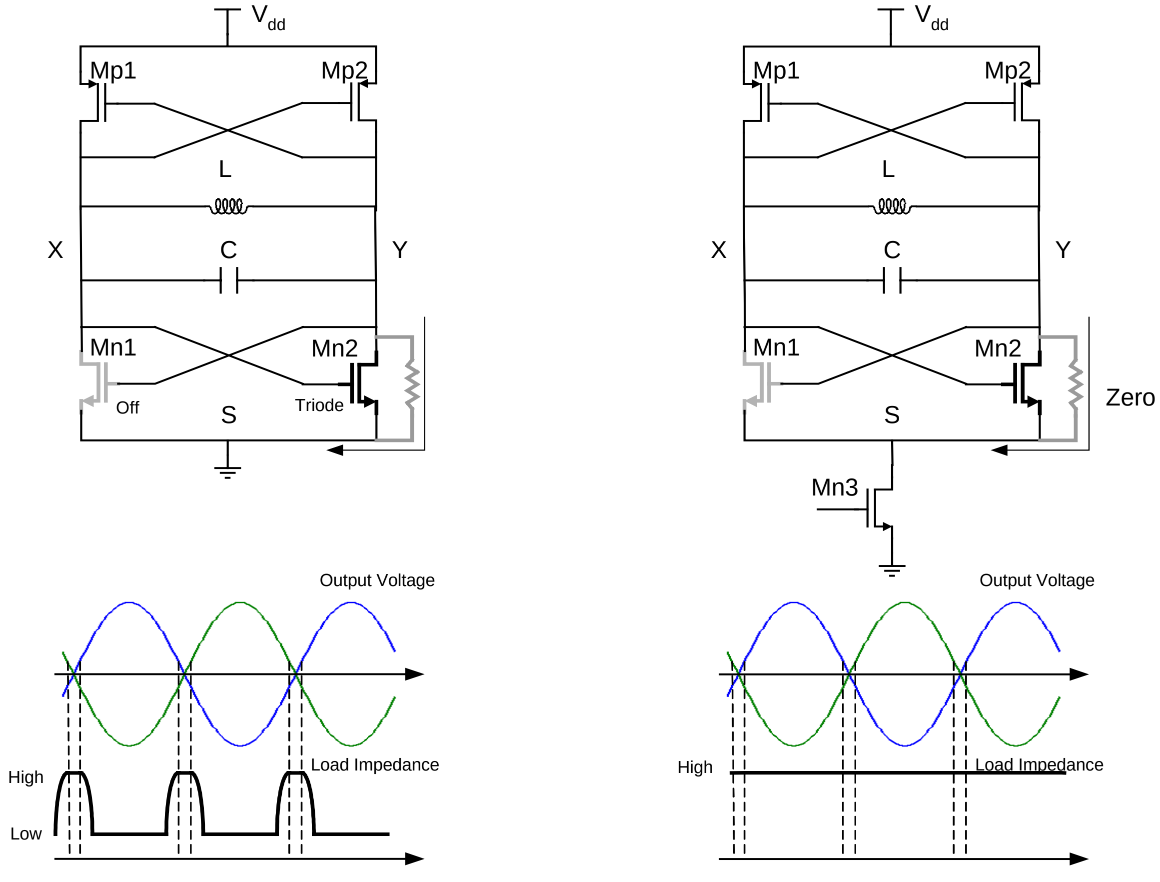
With large capacitor

- Lower channel length modulation
- Filtering noise from tail current

[A. Hajimiri, JSSC, May. 1999]

Noise Filtering Techniques (2)

Remove of tail current



(a) Without tail current

(b) With tail current

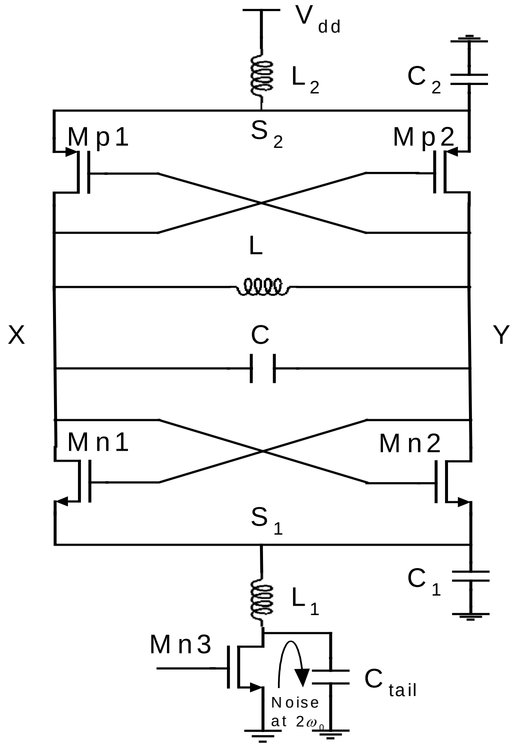
Roles of the tail current:

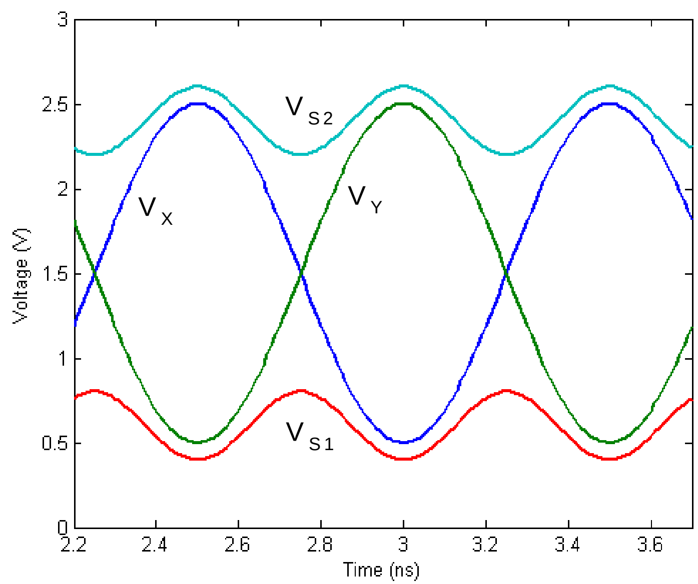
- Supply DC current
- Boost high impedance at common-source node
- Avoiding Q-degradation by triode region FETs

[S. Levantino, JSSC, Aug. 2002]

Noise Filtering Techniques (3)

LC filter at 2nd harmonic

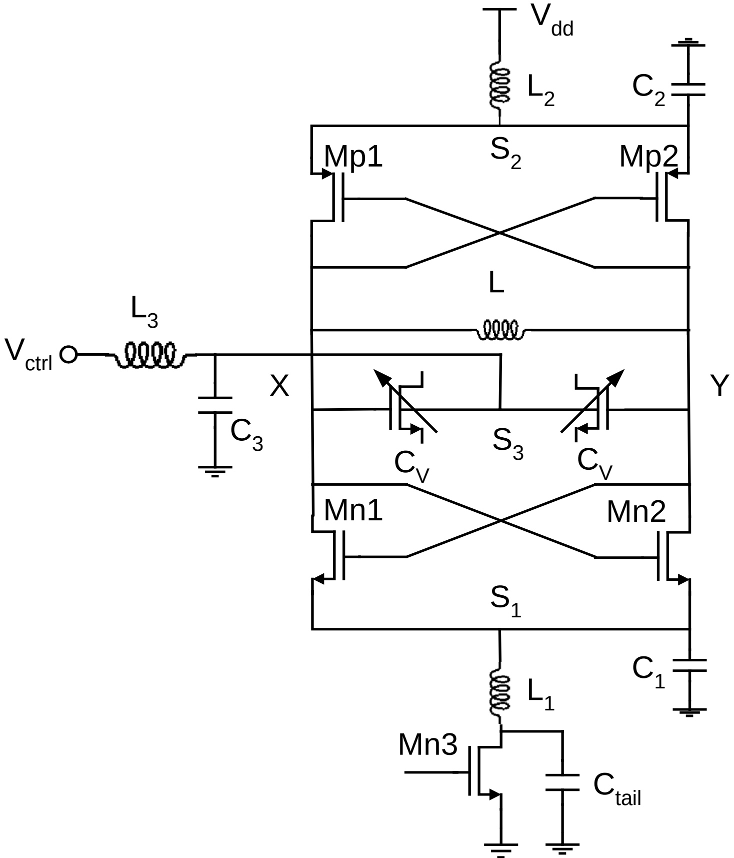


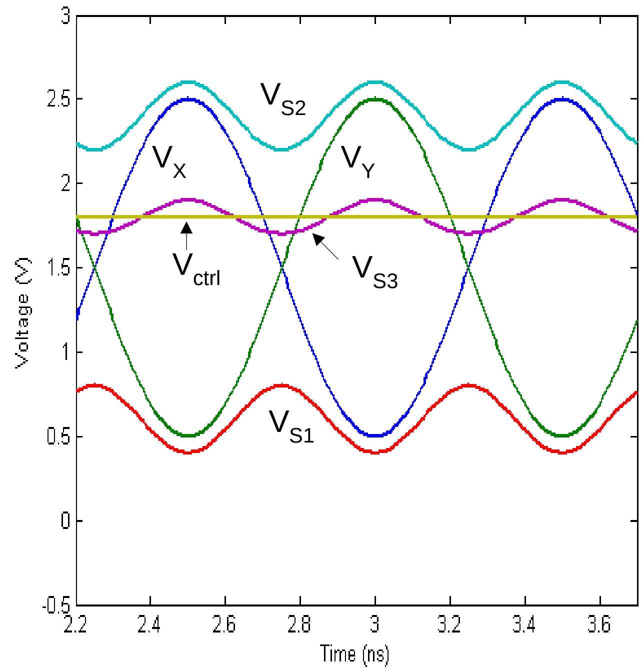


- L1 & C1, L2 & C2 resonates at 2nd harnonic
- Boost the impedance at each common-source node, avoiding Q-degradation
- Improve the oscillating amplitude voltage, and voltage-limited moves into current-limited

[E. Hegazi, JSSC, Dec. 2001]

Inductive Control Voltage (Proposed)



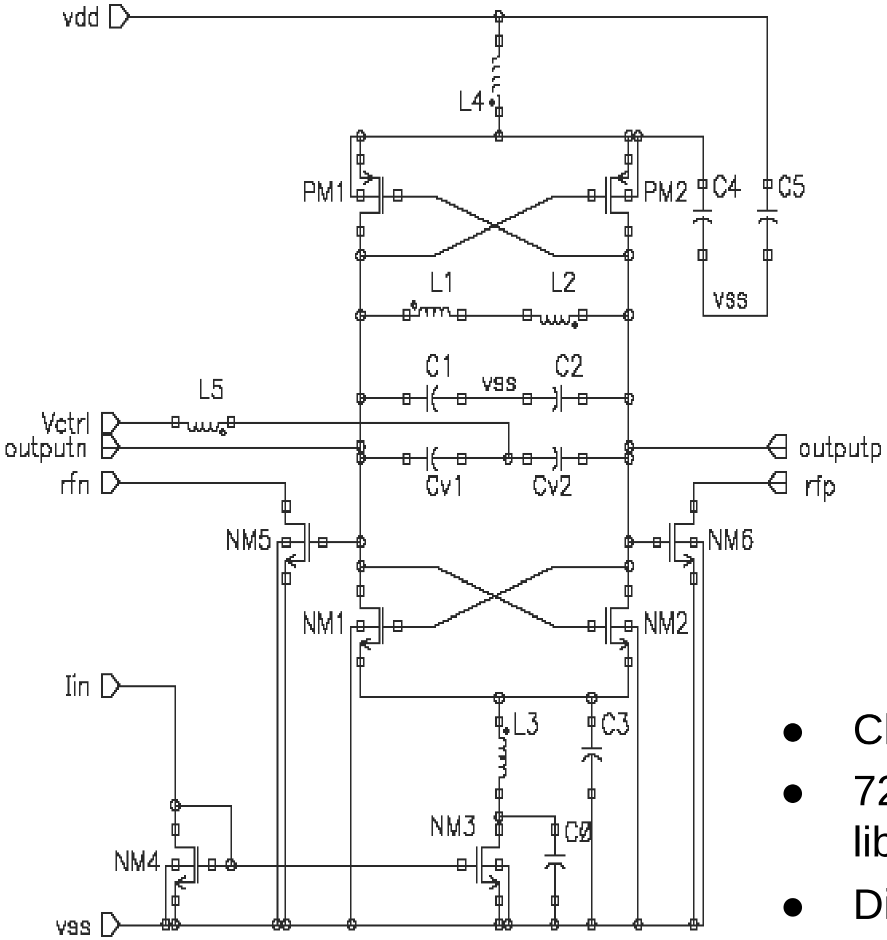


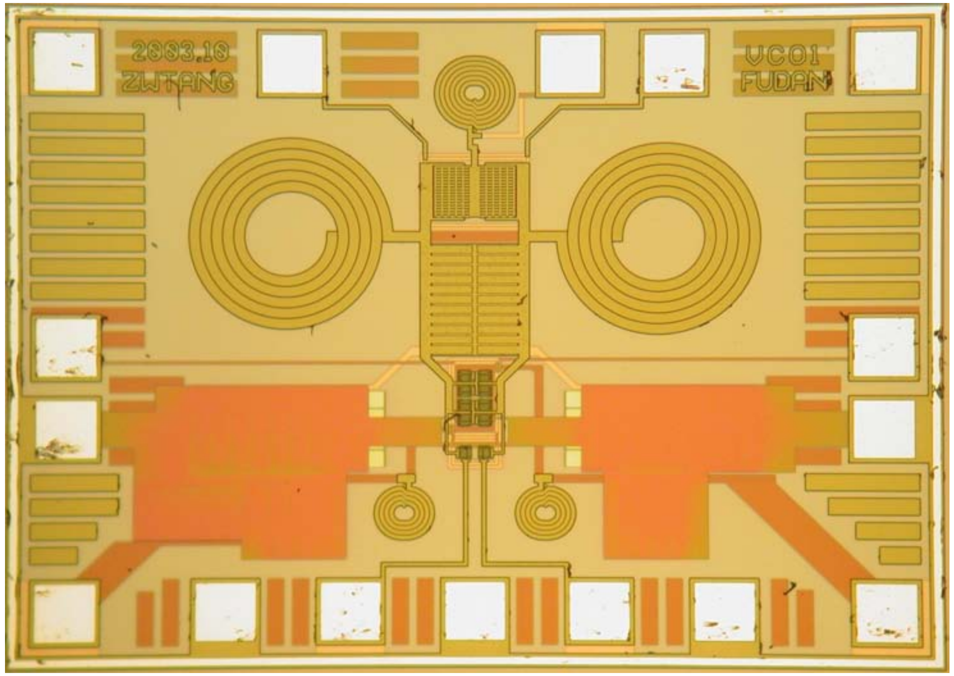
- L3 & C3 resonates at 2nd harnonic
- Lower even harmonics in oscillating voltage
- The oscillating voltage is more symmetric in one period

Outline

- Introduction
- Fundamentals of LC VCOs
- On-chip inductors
- Varactors and F-V tuning curve
- Optimization of LC VCOs
- Techniques of lowering phase noise
- Design examples
  - 1.08 GHz narrow LC VCO
  - 1.0-2.0 GHz wideband LC VCO
- Conclusion and prospect

Example I : 1.08GHz Narrowband LC VCO

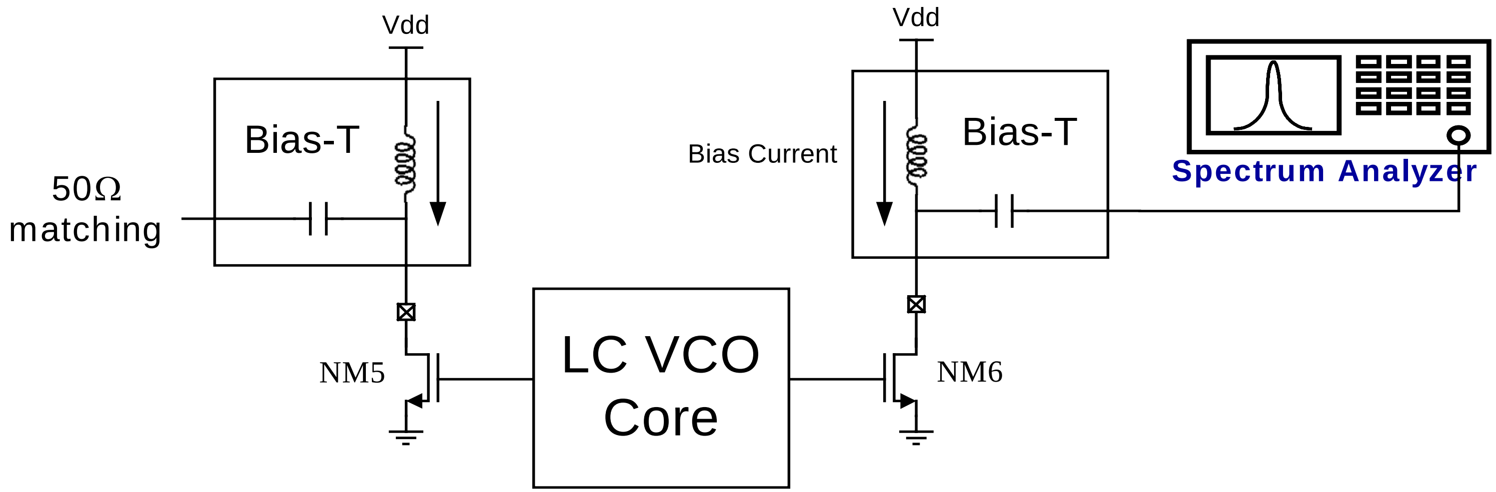


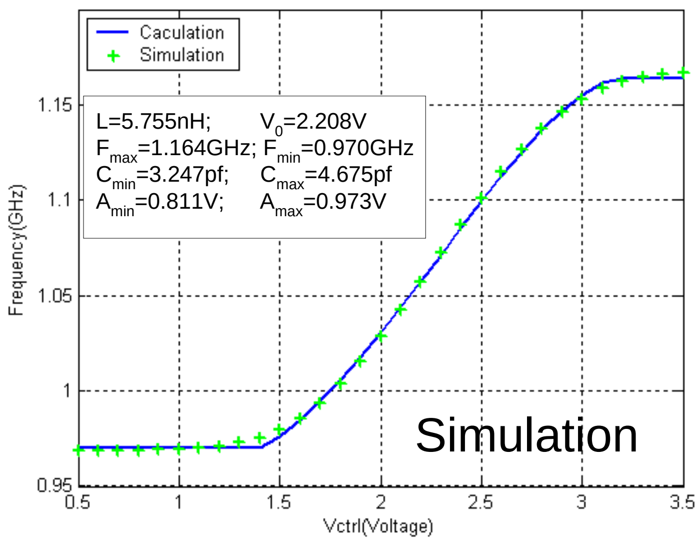


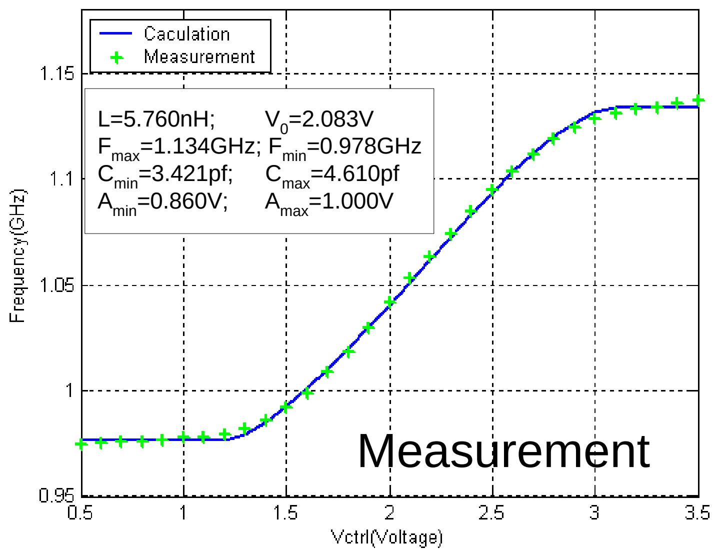
- Chartered CMOS 0.35μm 2P4M RF/MS process
- 72-side inductor and A-MOS Varactor in Chartered library
- Die Size: 1120μm×820μm

Simulation and Measurement of F-V Curve

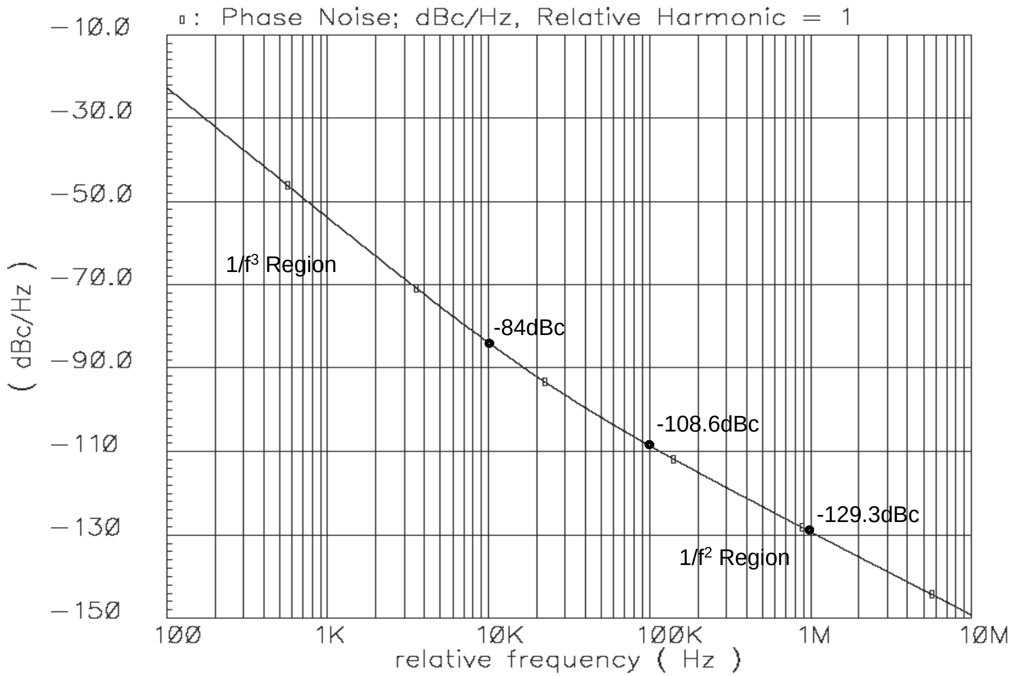
Test

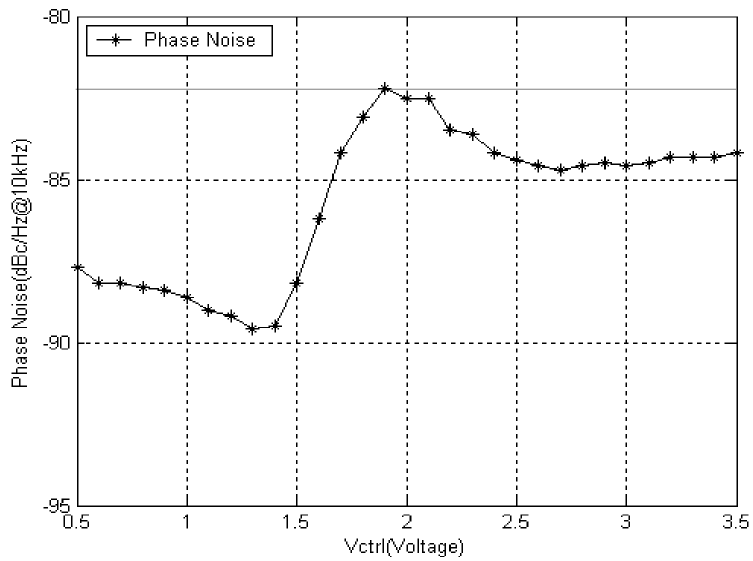






Phase Noise (Simulation)



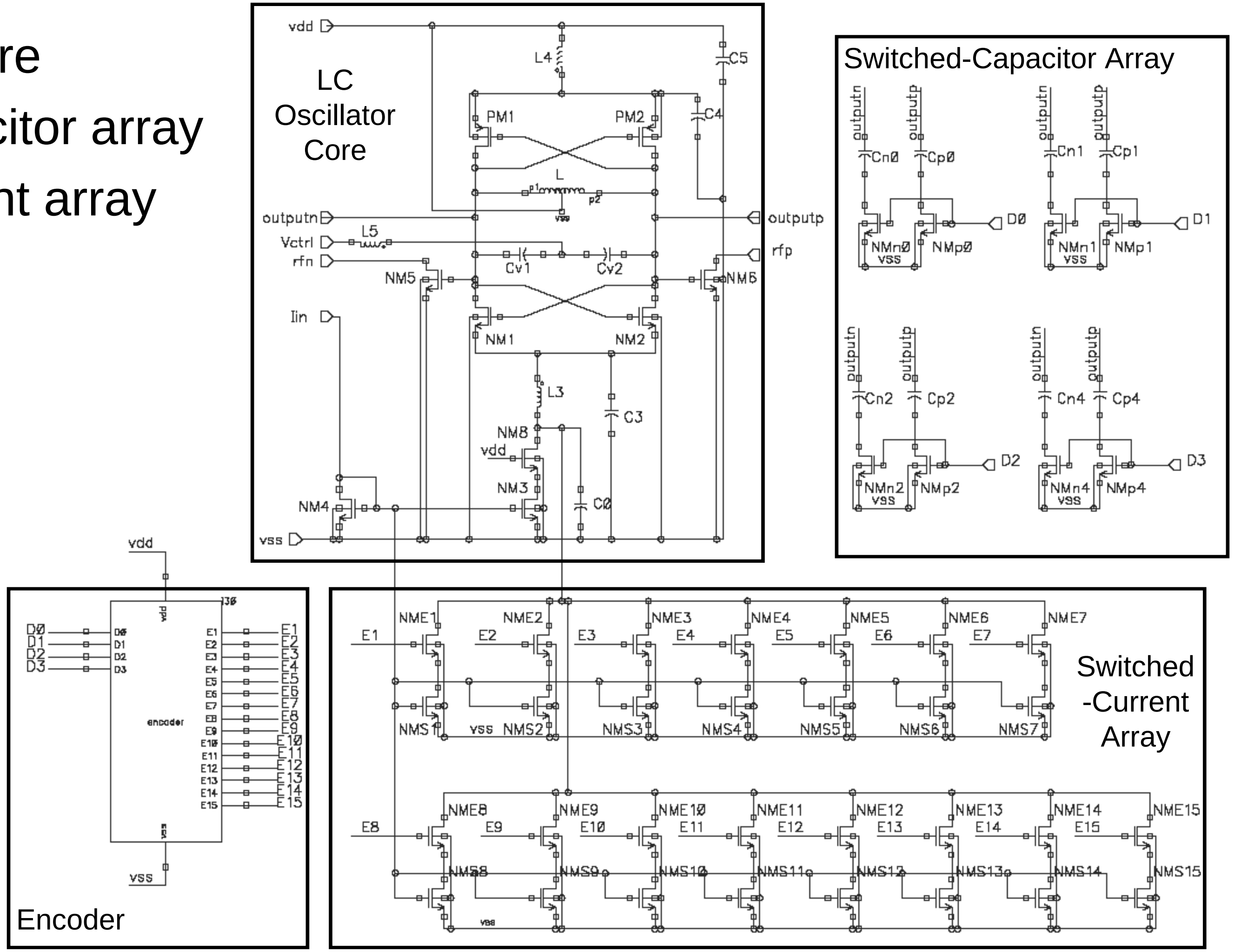


- Simulation in Cadence SpectreRF : Bias at 3.1mA
- Phase Noise < -82.2dBc/Hz@10kHz

Power Voltage	**3.3V**
Current	**3.1mA**
Oscillating Frequency	**945MHz-1137MHz**
Tuning Range	**±8.9%**
Phase Noise (Simulation)	**-82.2dBc/Hz@10kHz** **-108dBc/Hz@10kHz** **-129.3dBc/Hz@10kHz**

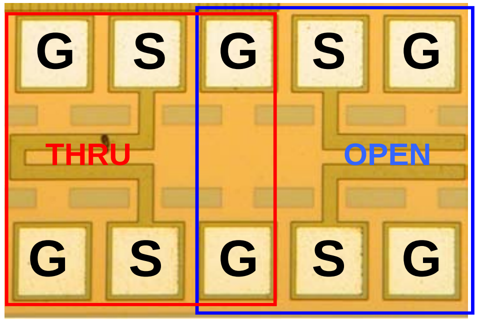
Example II : 1-2 GHz Wideband LC VCO

- LC oscillator core
- Switched-capacitor array
- Switched-current array
- Encoder

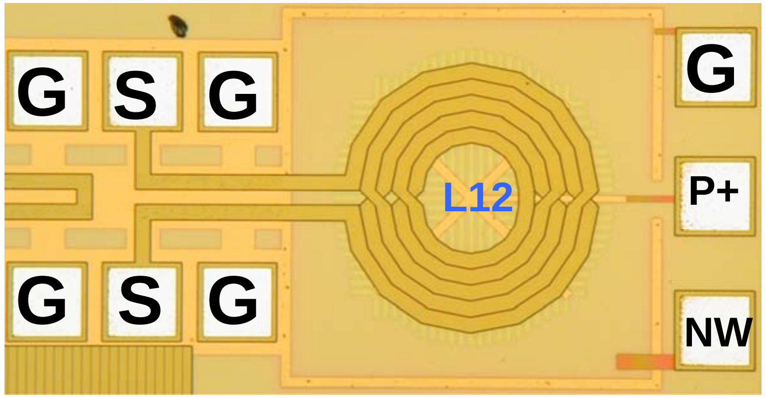


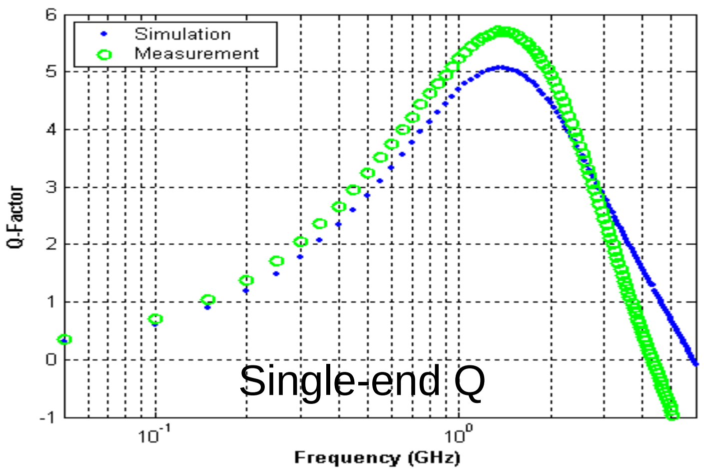
Differential On-Chip Inductor

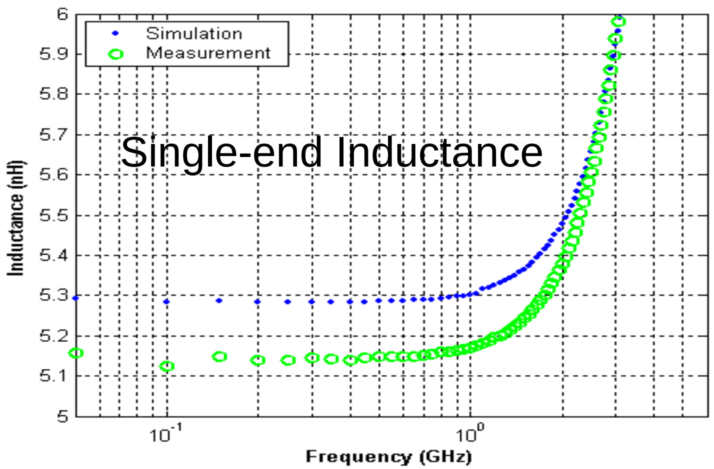
Core Diameter	**100μm**
Sides	**16**
Turns	**5**
Width	**15 μm**
Spacing	**1.5 μm**
Inductance	**5.2nH**
Single-end Q	**>5**



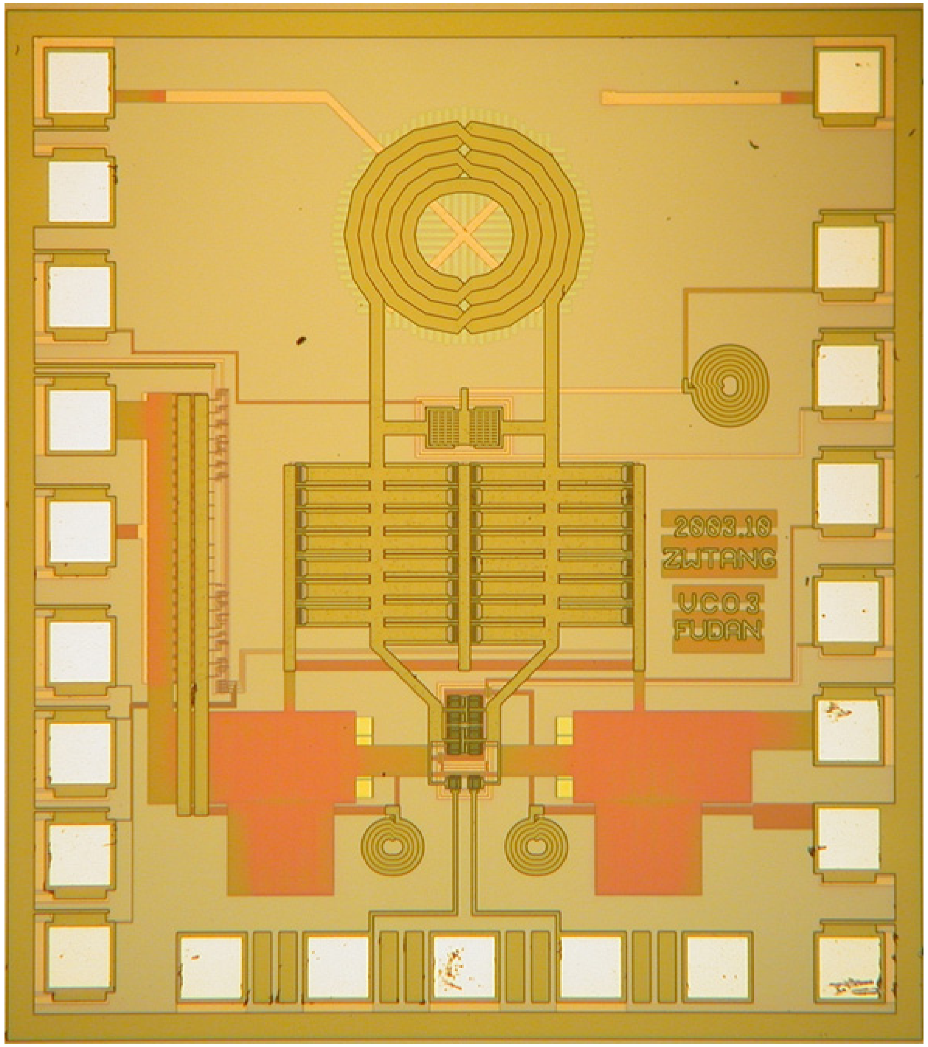
De-embeded PAD



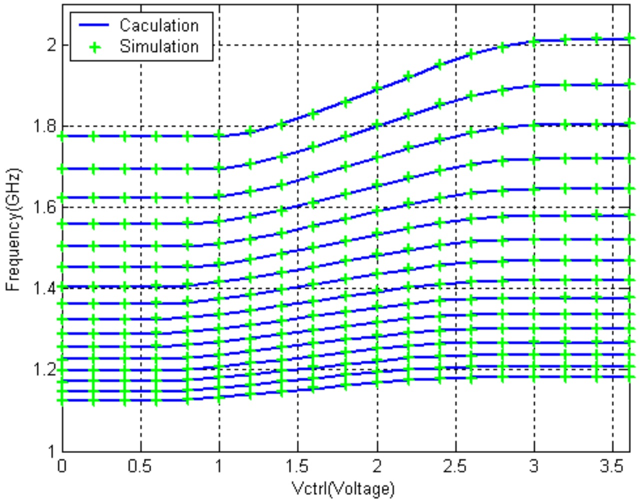




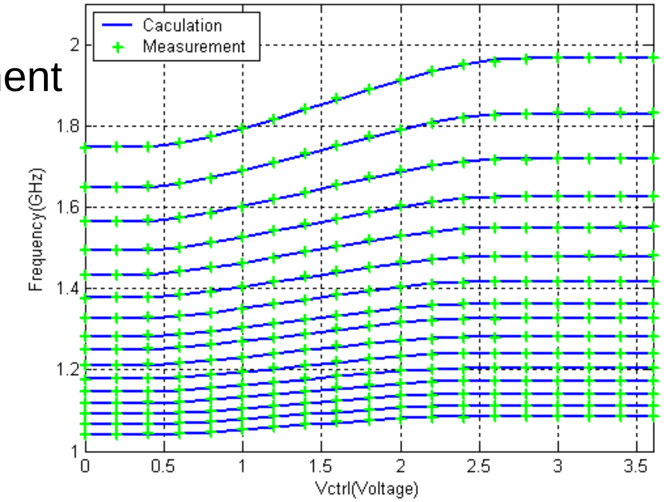
Simulation and Measurement of F-V Curve



Simulation

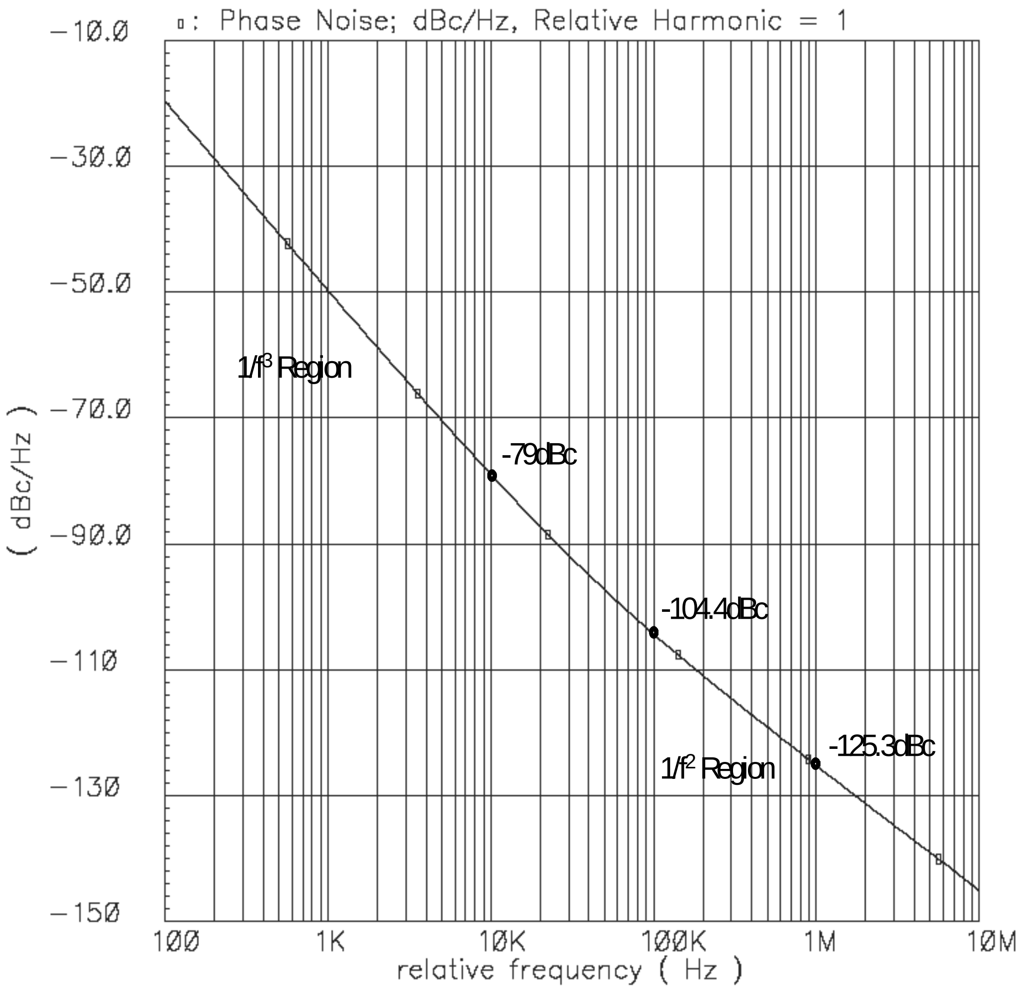


Measurement



ASIC & System State-Key Laboratory, Fudan University

Phase Noise (Simulation)



Power Voltage	3.3V
Current	3.5-10mA
Oscillating Frequency	1041MHz-1968MHz
Tuning Range	±31%
Phase Noise (Simulation)	-79dBc/Hz@10kHz -104.4dBc/Hz@10kHz -125.3dBc/Hz@10kHz

- Simulation in Cadence SpectreRF : Bias at 1.15mA
- Phase Noise < -80dBc/Hz@10kHz
- Die Size: 1120μm×1200μm

PFTN (Power-Frequency-Tuning-Normalized)

$$PFTN = 10\log\left[\frac{kT}{P_{\sup}}\left(\frac{f_{tune}}{f_{off}}\right)^2\right] - L(f_{off})$$

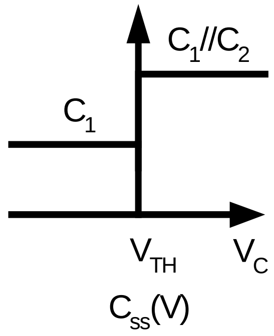
Reference	Process (μm)	Power (mW)	f_{tune} (MHz)	Fo (GHz)	Phase noise (dBc/Hz)	PFTN (dB)	Order
1.08GHz	0.35	10.23	192	1.08	-129@1MHz	-8.94	7
1.1-2GHz	0.35	33	927	1.50	-125@1MHz	-4.35	3
[13]	0.35	10	790	2.4	-115@600kHz	-6.41	5
[14]	0.7	24	81	1.8	-115@200kHz	-20.46	9
[15]	0.25	6	1	1.8	-121@600kHz	-56.15	10
[16]	0.35	12	364	1.3	-119@600kHz	-9.94	8
[17]	0.25	20	270	1.86	-143@3MHz	-4.73	4
[18]	0.25	7.25	1100	5.2	-132@3MHz	0.87	1
[19]	0.25	21.875	640	5.0	-124@1MHz	-7.08	6
[20]	0.13	2.7	1900	4.6	-112@1MHz	-0.85	2

Conclusions

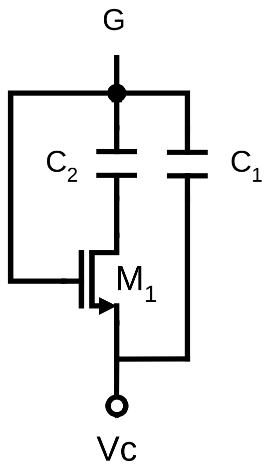
- On-chip inductors
  - ❖ Equivalent capacitance
  - ❖ Differential multilayer inductor
  - ❖ Quality factor improvement techniques
- Varactors and F-V tuning curve
  - ❖ Period calculation of LC-VCO with step-like varactor
- Optimization of LC VCO
  - ❖ High Q inductor, Lower R_s/L in on-chip inductor
- Techniques of lowering phase noise
  - ❖ Inductive control voltage
- Two design examples

Prospect(1): Switched MIM-Cap Varactor

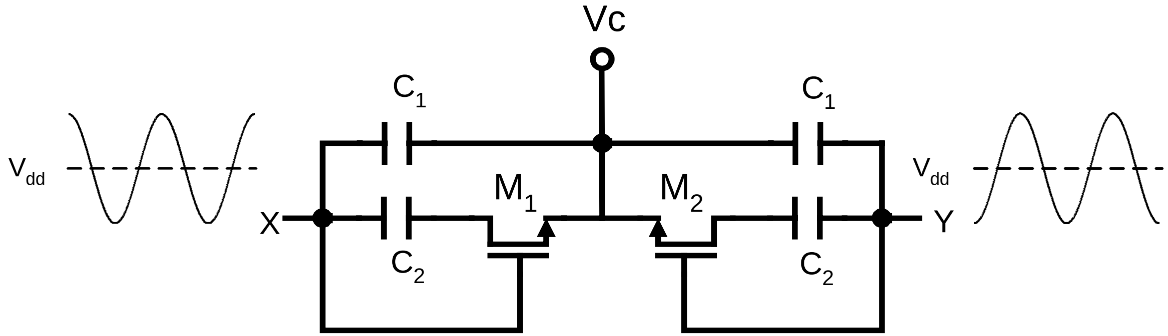
C-V Curve



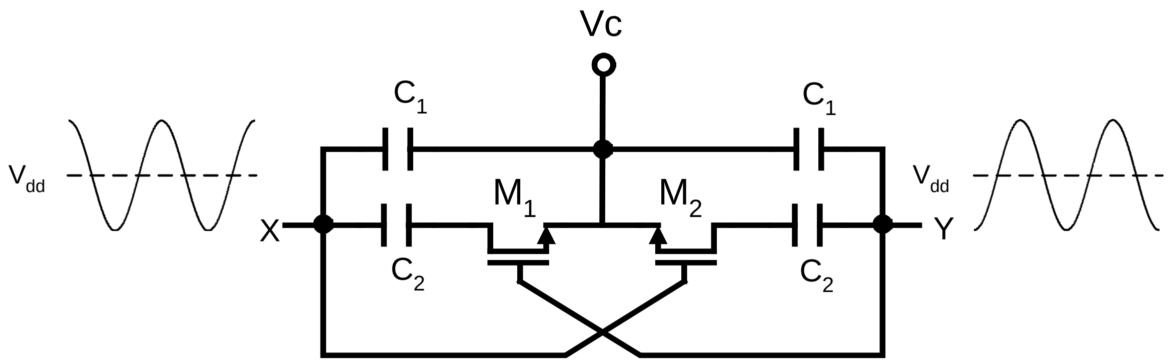
Switched MIM-Cap



Direct Model

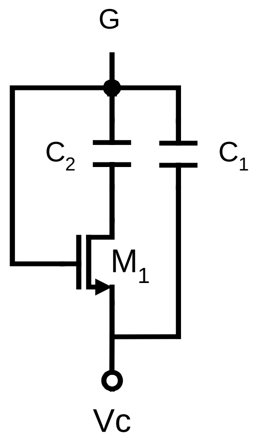


Cross Model

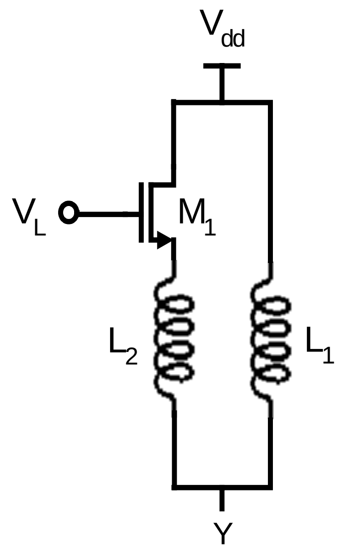


Prospect(2): Varactor and Vaructor

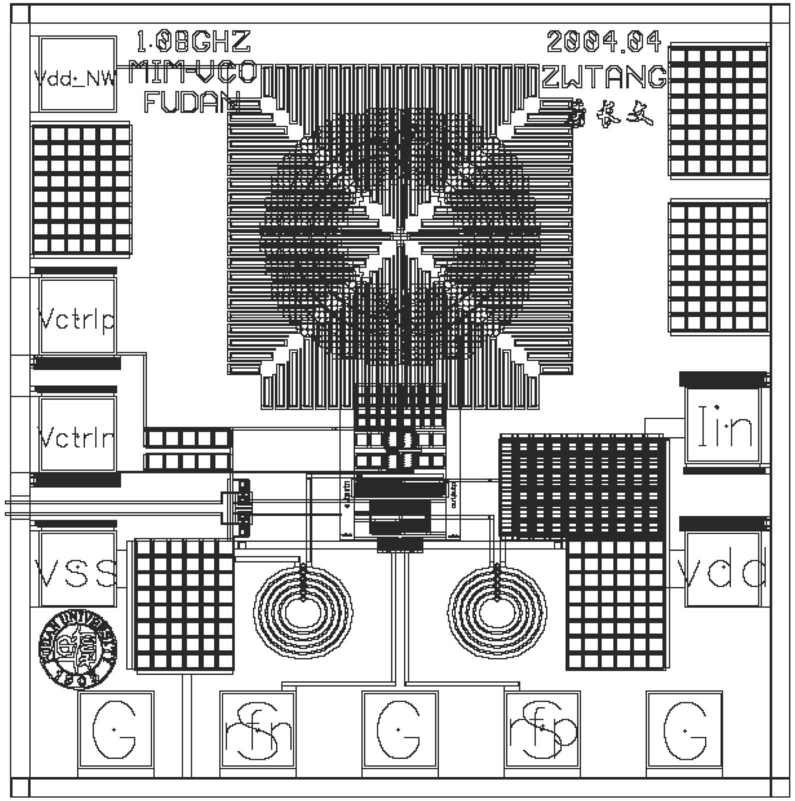
- *Var*iable Reson*ator*: *Varactor*

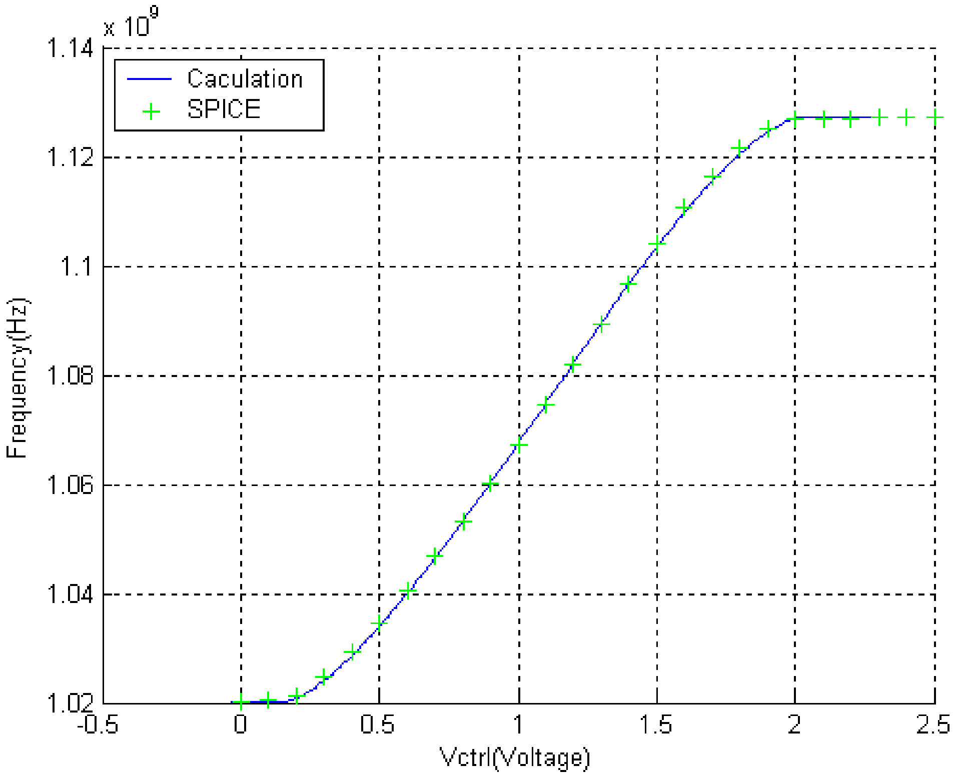


- *Var*iable Ind*uctor*: *Vaructor*



1.08GHz LC VCO with MIM Varactors





- Simulation in SpectreRF
  F-V curves, 3.3mA
- Phase Noise < -89.7dBc/Hz@10kHz

- Better phase noise in LC-VCO with MIM Varactor than in one with MOS Varactor
- Simulation agrees well with the calculation
- TSMC 0.25μm 2P5M RF/MS process

Acknowledgements

- Prof. Hao Min (Adivsor), Fudan University
- Prof. Chengshou Sun, Guoquang Zhang, Feng Zhou, Wenhong Li, Fudan University
- Prof. Qianling Zhang, Junyan Ren, Zengyu Zheng, Lianxing Yang, Zhiliang Hong, Dian Zhou, Fudan University
- Prof. Lingling Sun, Jiang Hu, HIZEE University
- Fuxiao Li, Zhengyu Zhu, No. 55 Institute of Science and Technology
- Prof. Xiaowei Sun, Rong Qian, Shanghai Institute of M.S & IT
- Hongyan Jian, Jie He, Shi Shu, Fengling Yang, TV Tuner Group
- Qiang Li, Yifeng Han, RFID Group, Haiqing Zhang, Yawei Guo
- MPW service at ICC
- Supported in part by Shanghai Science & Technology Committee under SDC Project
- Supported in part by Fudan-Infineon Joint Lab

Thanks!