(MO4B-4)

A Fully Integrated 1.175-to-2GHz Frequency Synthesizer with Constant Bandwidth for DVB-T Applications

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Outline

- Reasons that cause the variation of loop bandwidth
- Wideband VCO with constant tuning gain (K_{VCO}) and band step
- Automatic frequency control (AFC) and charge pump
- Circuit details and measurement results

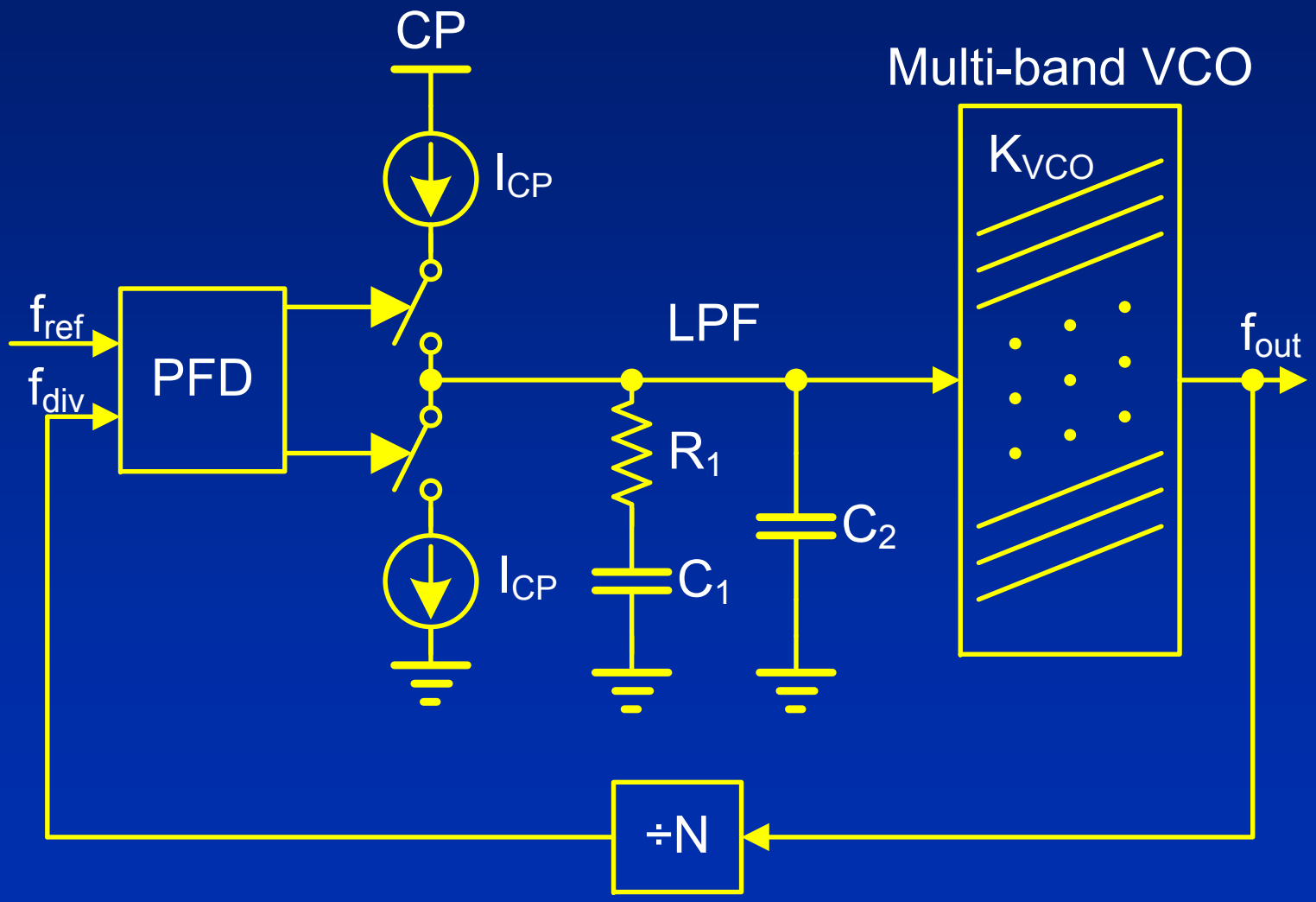
Motivation

- Dual-conversion DVB-T architecture needs a 1.175-to-2GHz frequency synthesizer
- Loop bandwidth changes due to VCO tuning gain (K_{VCO}) and division ratio
- Variation of loop bandwidth may result in loop instability and phase noise deterioration
- To ensure loop bandwidth constant, some techniques are explored...

Pros & Cons

- Good points
  - Single LC-VCO is used
  - Loop bandwidth variation is within ±10%
  - Phase noise is nearly constant
  - Integrated rms phase error is sub-1°
- Problems
  - Process limits the minimum values of capacitors and varactors
  - Add a little complexity in layout design

Diagram of Third-Order PLL



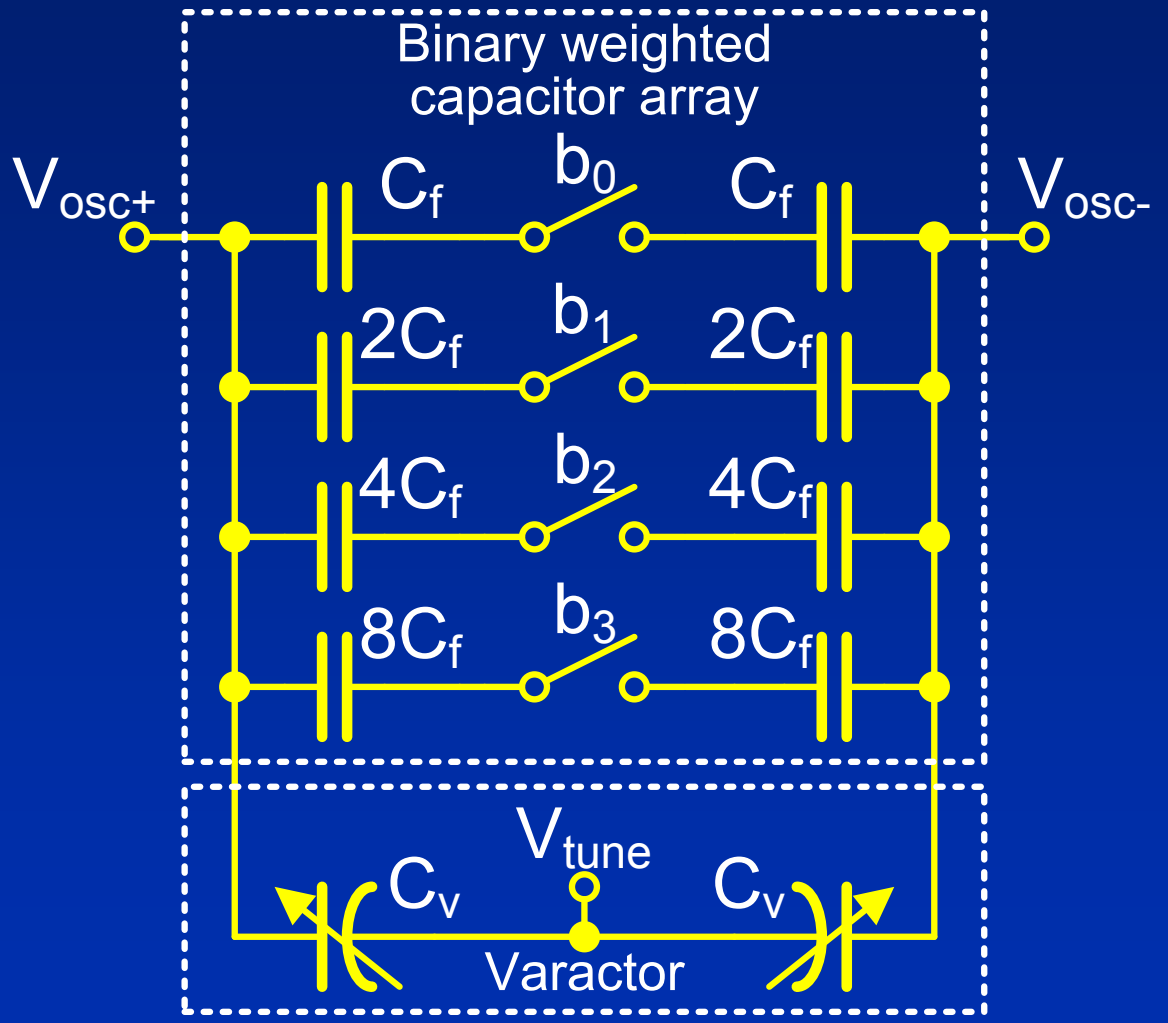
Definition of loop Bandwidth

- Open-loop cut-off frequency is selected as loop bandwidth, but not intuitively
- Loop gain is a good substitute
- For typical third-order PLL with second-order passive filter, loop gain can be expressed as

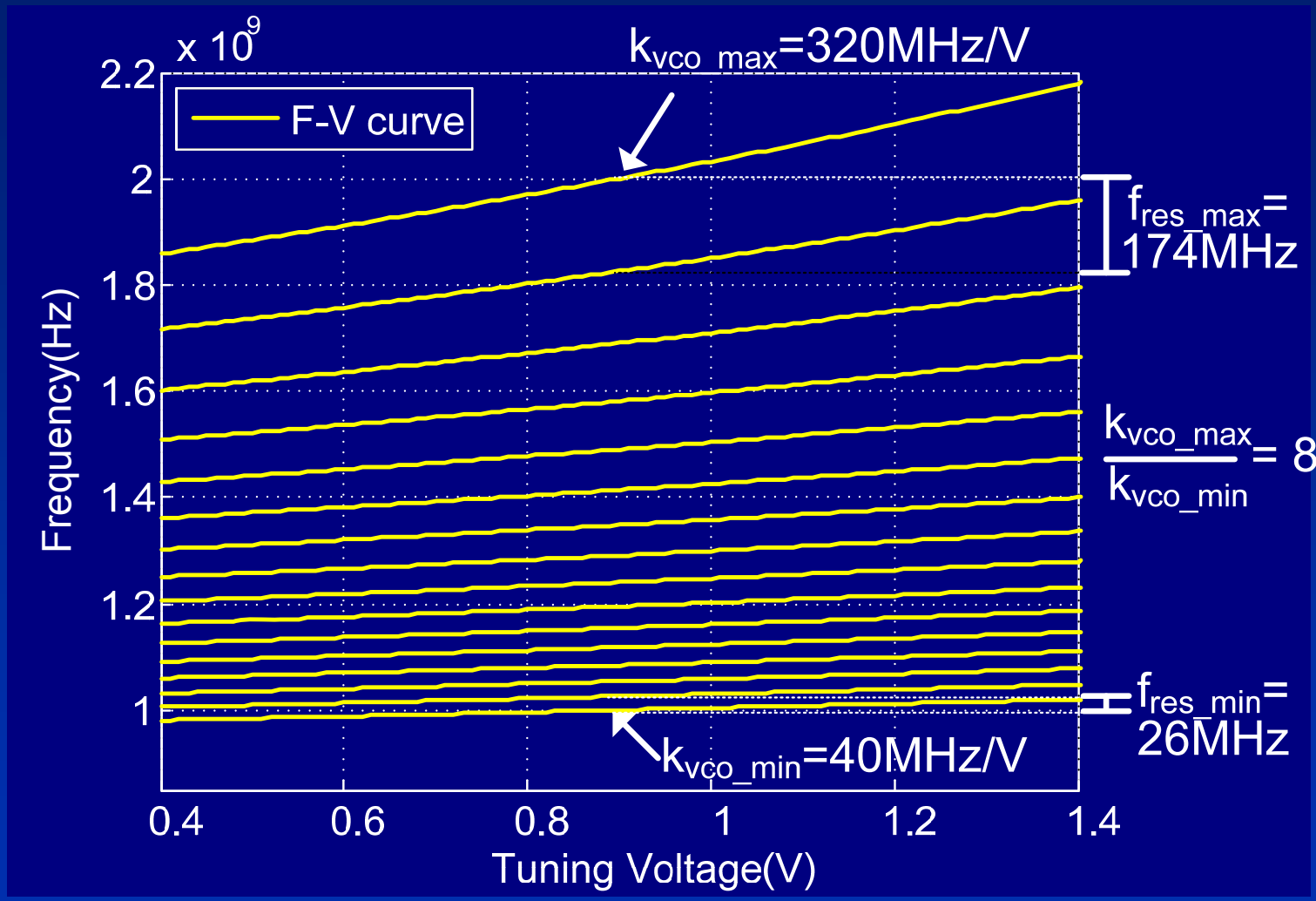
$$BW = \frac{I_{CP} K_{VCO} R_1}{2\pi N} \cdot \frac{b}{b+1} \approx \frac{I_{CP} K_{VCO} R_1}{2\pi N} \quad (b>10)$$

- K_{VCO} and N are variables

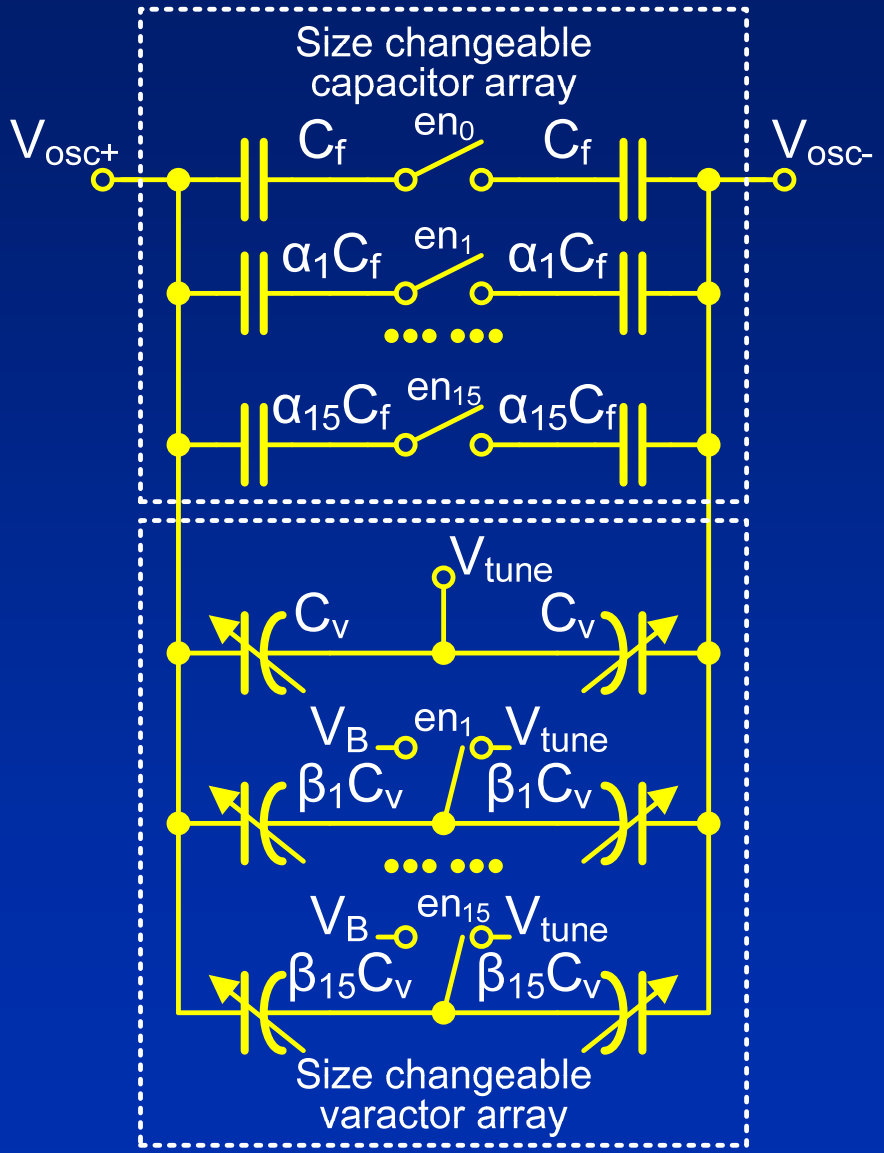
Conventional Capacitor Array



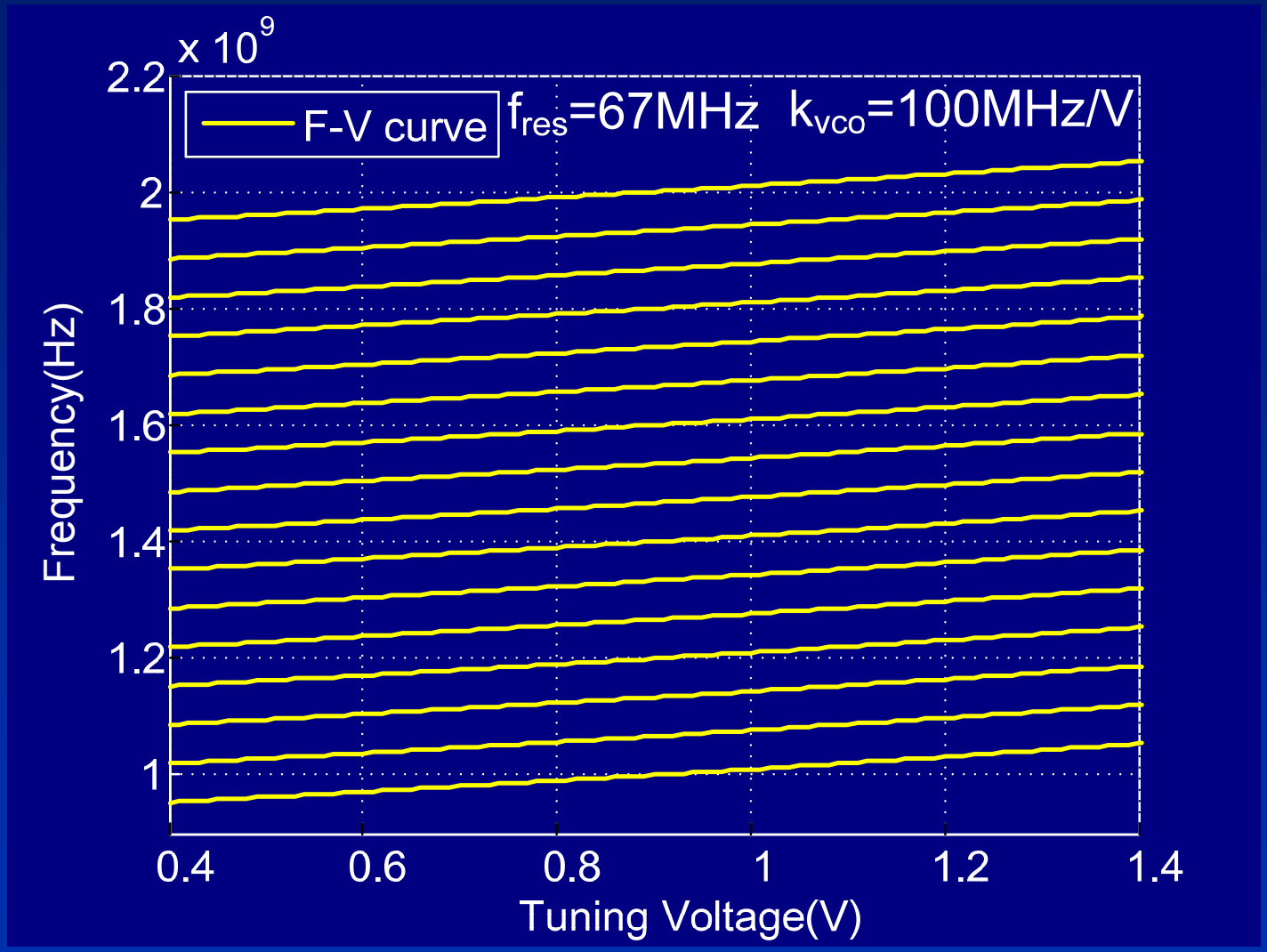
F-V Curves of Conventional Topology



Proposed Capacitor Array



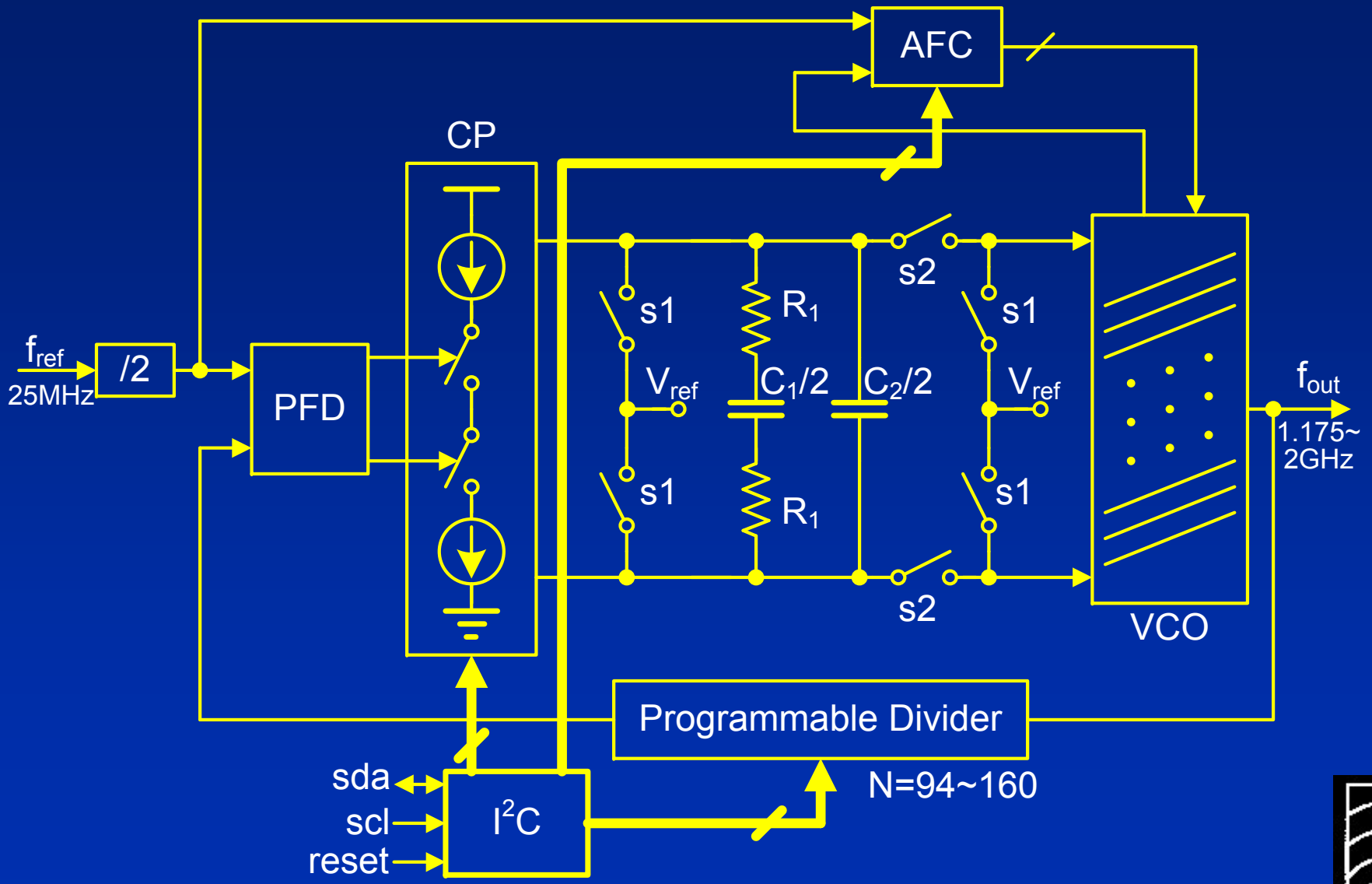
F-V Curves of Proposed Topology



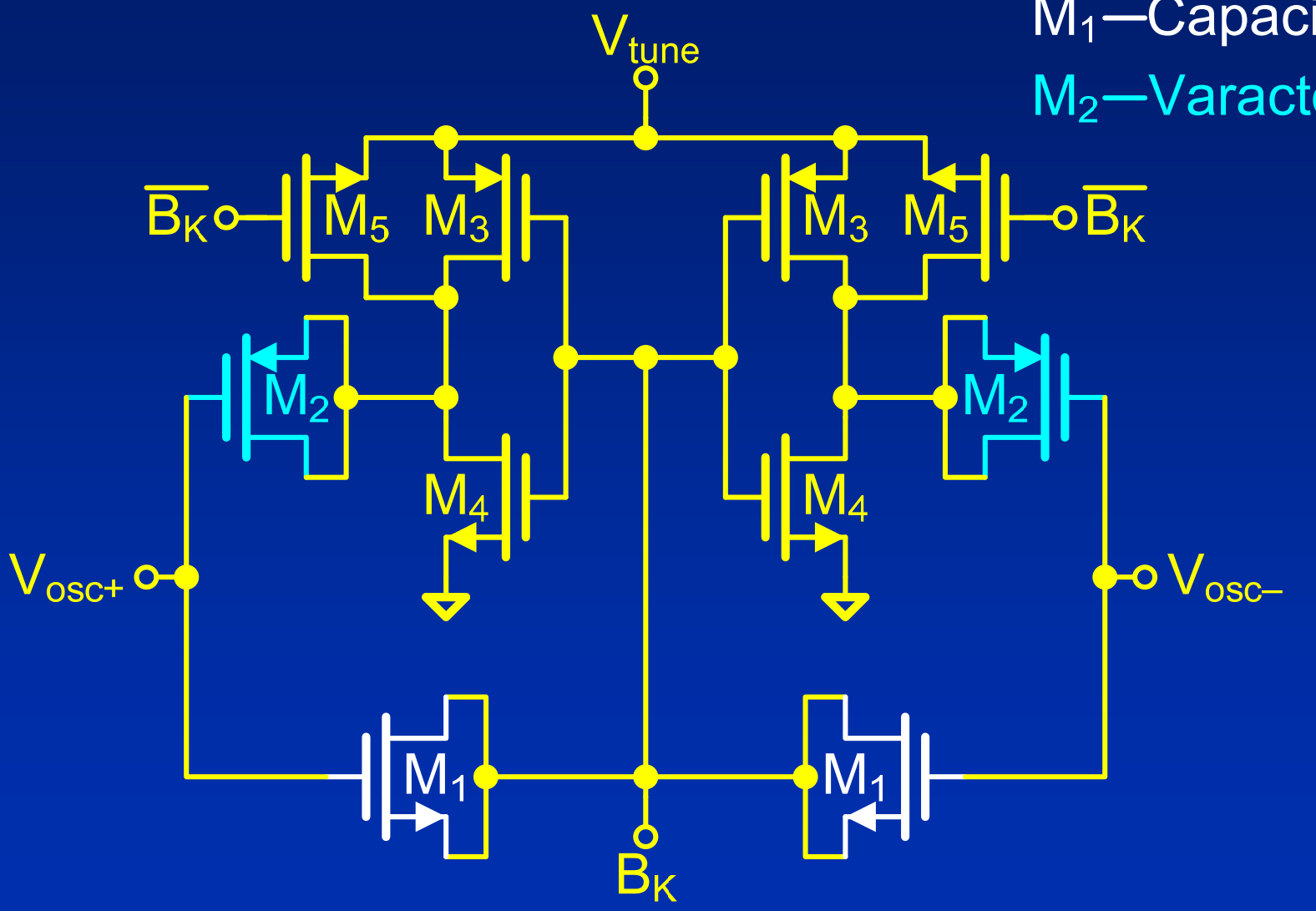
AFC & Charge Pump

- The region near the middle of one single F-V curve is linear and maximal
- AFC guarantees that the band of which the center frequency is closest to the target value is chosen
- I_{CP} is programmed to match division ratio and I_{CP}/N is maintained

High Level Diagram of IC



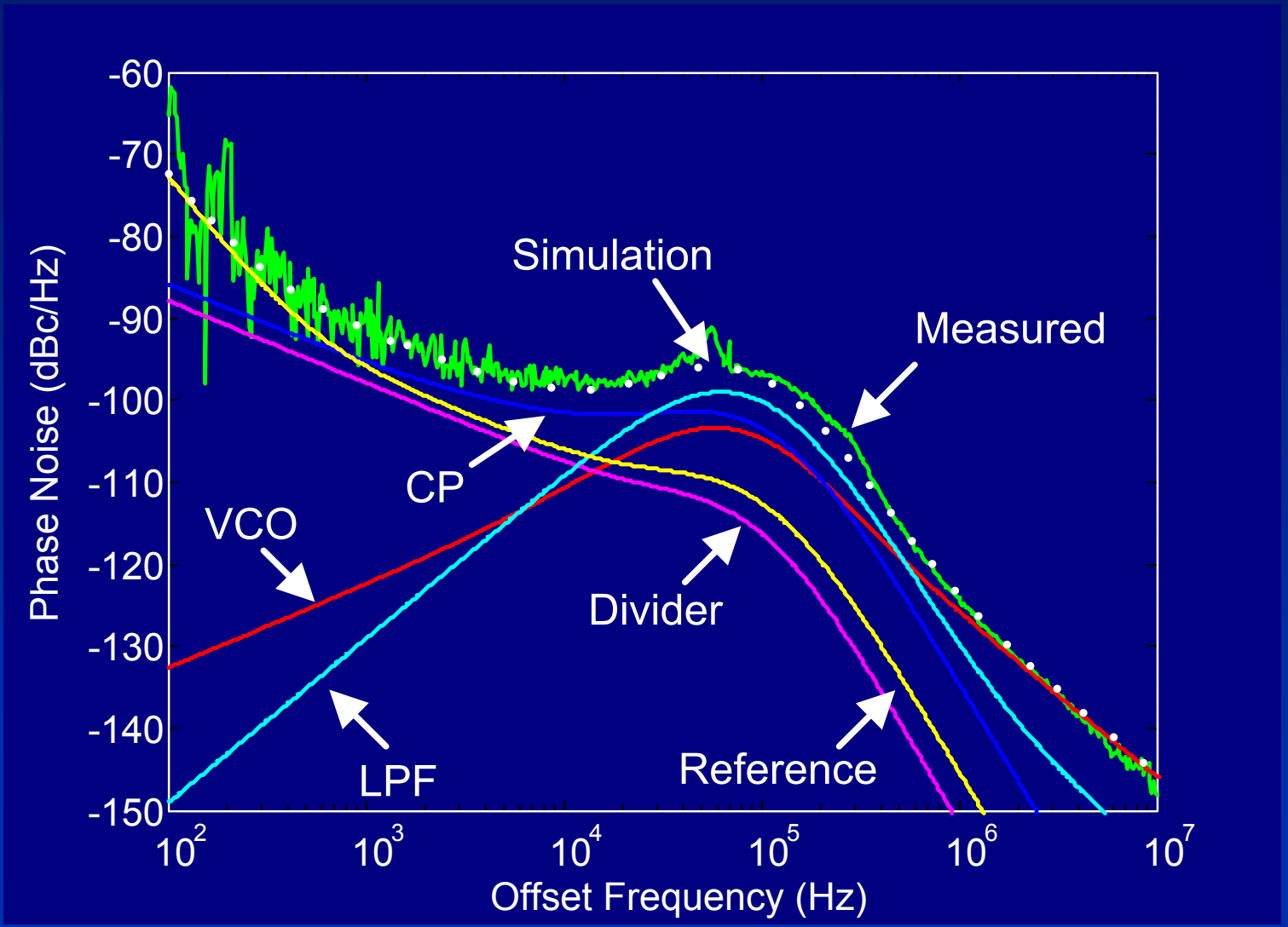
Unit of Capacitor and Varactor



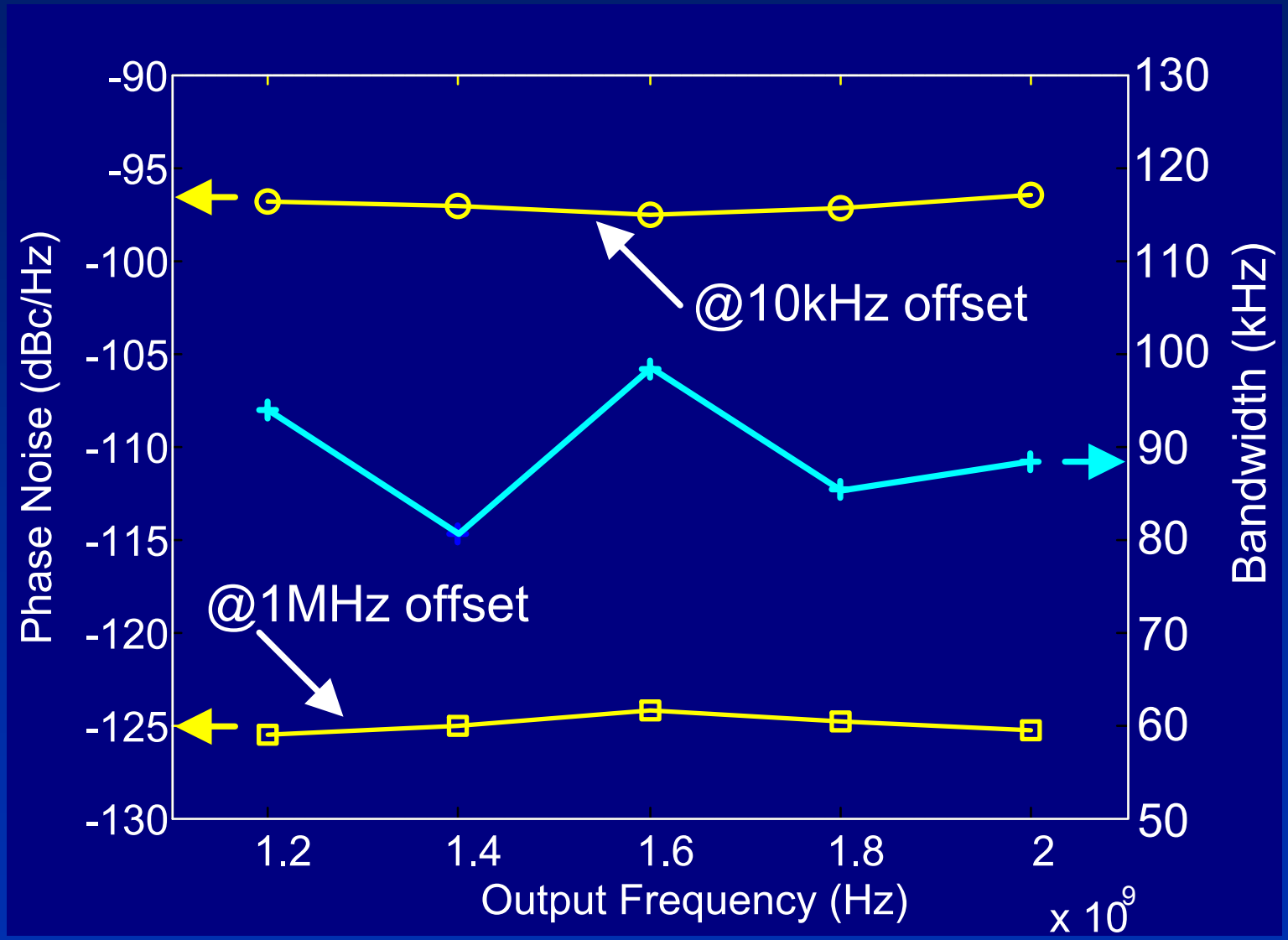
Other IC Details

- LC-VCO: Differentially tuned, complementary cross-coupled, single differential inductor and two tail inductors
- Charge Pump: Differentially with common-mode feedback
- Divider: Cascaded 2/3 dividers, two stages CML and six stages CMOS
- LPF: MIM capacitor, poly resistor

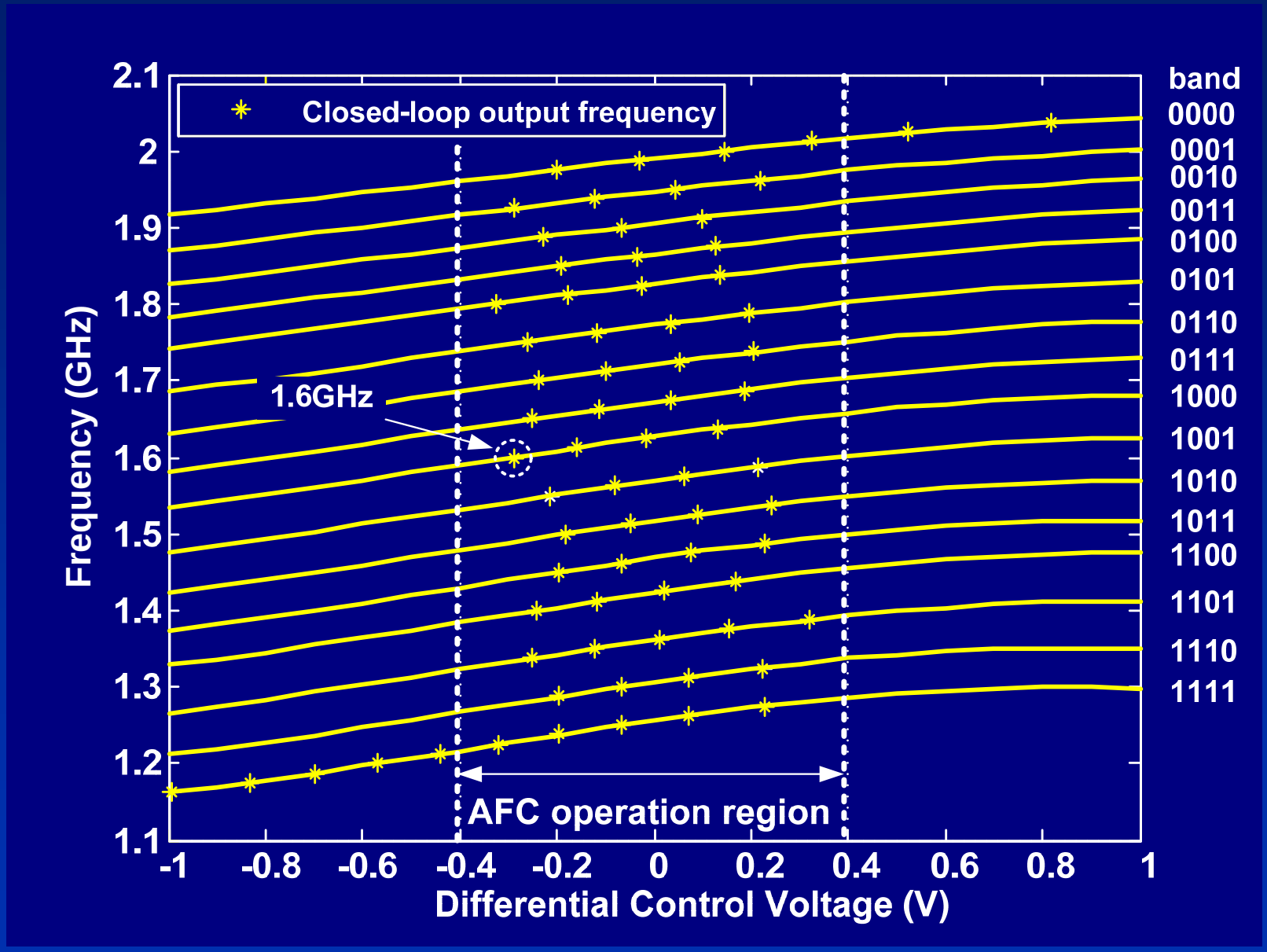
Phase Noise at 1.6 GHz Frequency



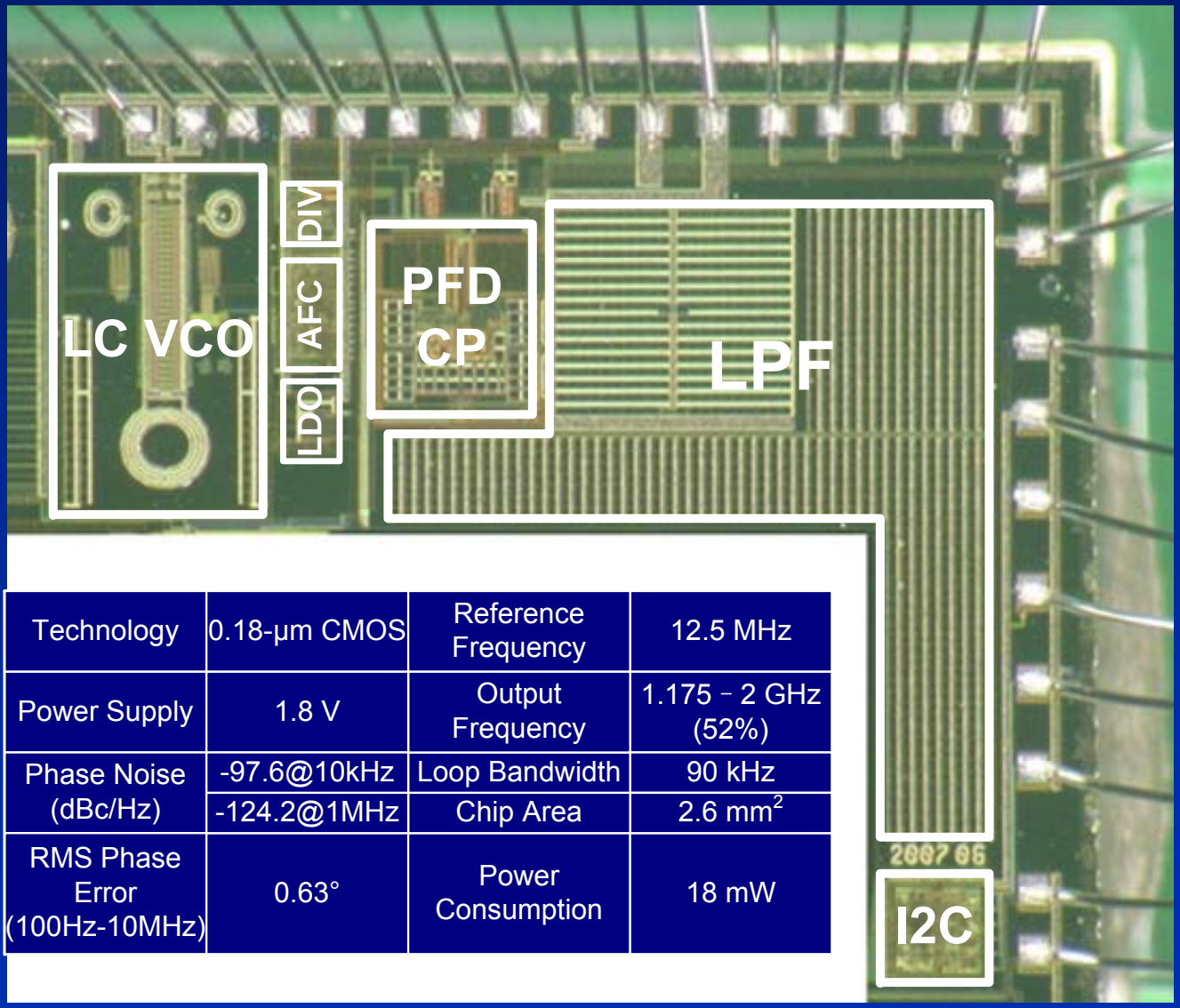
Phase Noise and Bandwidth



F-V Curves of 16 sub-bands



Die Microphotograph and summary



Technology	0.18-μm CMOS	Reference Frequency	12.5 MHz
Power Supply	1.8 V	Output Frequency	1.175 – 2 GHz (52%)
Phase Noise (dBc/Hz)	-97.6@10kHz	Loop Bandwidth	90 kHz
	-124.2@1MHz	Chip Area	2.6 mm^2
RMS Phase Error (100Hz-10MHz)	0.63°	Power Consumption	18 mW

Performance Comparisons

Ref.	ISSCC'06	ISSCC'07	This Work
Output Freq.	2.24-4.48GHz	1.1-2.2GHz	1.175-2GHz
VCO type	Ring	Three LC	Single LC
Phase noise (dBc/Hz)	-98@100kHz -100@1MHz	-90@10kHz	-97.6@10kHz -124.2@1MHz
Phase Error	0.8°	1.5°	0.63°
Power	132mW	N.A.	18mW
Tech.	0.13-μm CMOS	0.18-μm CMOS	0.18-μm CMOS

Conclusion

- Have used the loop gain instead to indicate the loop bandwidth intuitively
- Have made both capacitors and varactors changeable to maintain K_{VCO} and band step
- Have demonstrated loop bandwidth is nearly constant and phase noise is maintained across the wideband frequency range