A Fully Integrated 1.175-to-2GHz Frequency Synthesizer with Constant Bandwidth for DVB-T Applications

Lei Lu, Lu Yuan, Hao Min and Zhangwen Tang*

ASIC & System State Key Laboratory, Fudan University, Shanghai, China, 201203

Abstract — **A fully integrated 1.175 to 2GHz differentially tuned frequency synthesizer aimed for DVB-T tuners is implemented in 0.18-μm CMOS. Techniques are proposed to make the loop bandwidth constant across the whole output frequency range to maintain phase noise optimization and loop stability. It exhibits in-band phase noise of -97.6dBc/Hz at 10kHz offset and integrated phase error of 0.63° from 100Hz to 10MHz. The chip draws 10mA from a 1.8V supply while occupying 2.6mm² die area.**

Index Terms — **Frequency synthesizer, wideband, tuning gain (K_{VCO}), constant bandwidth, phase noise.**

I. INTRODUCTION

The dual-conversion architecture of digital video broadcasting-terrestrial (DVB-T) tuners which receive signals in the 48-862MHz frequency range, demands the use of a wideband frequency synthesizer as the first local oscillator (LO) [1]. The wideband frequency synthesizer should meet stringent phase noise requirement over the whole frequency range from 1.175GHz to 2GHz without sacrificing loop stability. To cover such a wideband frequency range, switching capacitor array is usually used in LC voltage-controlled-oscillator (VCO) to extend the tuning range with low VCO tuning gain (K_{VCO}), which avoids degrading the phase noise performance [2]. However, the loop bandwidth (BW), which determines the phase noise optimization and loop response characteristics, will change due to the variation of division ratio and tuning gain of multi-band VCO [3].

The block diagram of the wideband frequency synthesizer is shown in Fig. 1, which is completely integrated including a phase-frequency detector (PFD), a rail-to-rail differential charge pump (CP), a passive loop filter (LPF), an wideband LC-VCO, a programmable divider, an automatic frequency control (AFC) block and an I2C controller. In order to suppress noise from substrate and power supply, charge pump, LPF and LC-VCO are all differentially configured.

This paper is organized as follows: Section II shows some wideband issues; Section III presents the proposed solutions; Section IV describes the experimental results. Finally, some conclusions are drawn in Section V.

---

* Corresponding author. Email: zwtang@fudan.edu.cn
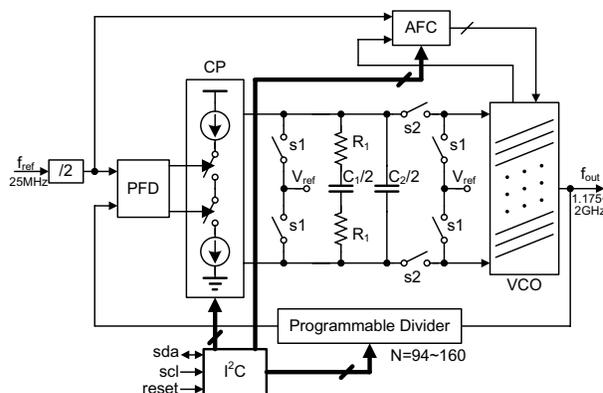
Fig. 1. Diagram of wideband frequency synthesizer with differential tuning.

II. DESIGN CONSIDERATIONS

A. Bandwidth

Because the synthesizer is a closed-loop system, its loop bandwidth, which describes the rate of system response and indicates whether it is stable, is an important parameter and about 1/20 of the reference frequency. On the other hand, phase noise optimization requires a certain bandwidth with respect to the given charge pump and VCO circuits. For every different output frequency, the loop bandwidth must be constant to minimize phase noise variation and guarantee loop stability over a wideband frequency range. Usually open-loop cut-off frequency is selected as the loop bandwidth by designers, however, for third or higher order loop there is no intuitive expression about it. Loop gain is a good indication of low-pass corner frequency for the open-loop transfer function and is defined as bandwidth. For typical third-order PLL, loop gain can be expressed as [4]

$$BW = \frac{I_{CP}K_{VCO}R_1}{2\pi N}\frac{b}{b+1} \approx \frac{I_{CP}K_{VCO}R_1}{2\pi N} \quad (b > 10) \qquad (1)$$

where I_{CP} is the sink or source current of charge pump, K_{VCO} is the VCO tuning gain, N is the division ratio, R_1 is the loop filter resistor and b is the ratio of C_1 over C_2. To keep the bandwidth constant without changing the

position of poles and zeros when N varies, a simple way is to make I_{CP} match N and hold K_{VCO}.

(a)

(b)
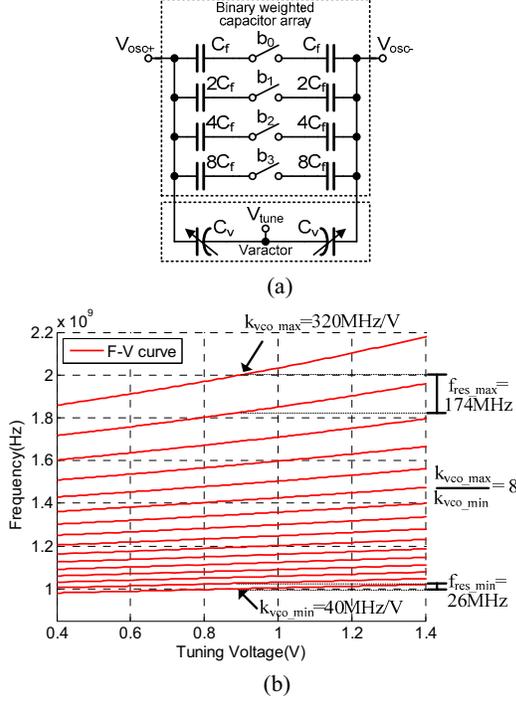
Fig. 2. Conventional topology (a) Switching capacitor array and one varactor unit (b) F-V curve with large variations of VCO tuning gain and band step.

B. VCO Tuning Gain

Frequency synthesizers for RF receivers usually employ an LC voltage-controlled oscillator (VCO). The targeted 800MHz frequency range requires an oscillation gain of 500MHz/V, with which a 1.6V tuning range is allowed for the charge pump. Such a high K_{VCO} may worsen the phase noise performance. To cover a wideband frequency range with low K_{VCO}, switching capacitor array is usually adopted, which is shown in Fig. 2(a). Varactor C_V is tuned by the control voltage to change the output frequency continuously, while a binary weighted capacitor array is controlled digitally to shift the output frequency band discretely, where 4bit is used for example.

Although the switching capacitor topology is useful to extend the output frequency range while maintaining a lower K_{VCO}, it has two disadvantages. Firstly, equal capacitor is switched in or out of the bank whenever a lower or higher band is required. Due to the nonlinearity of frequency to capacitance, K_{VCO} will change by a factor of 8 when the output frequency doubles by reducing the tank capacitance to a quarter [5]. The simulated F-V curve is shown in Fig. 2(b), where a tank inductance of

4nH is used. Such a large VCO gain variation alters the bandwidth greatly, so the phase noise performance will deteriorate and the loop will turn into instability. Secondly, band frequency difference may increase the complexity of the method of AFC, which will be described in the next section.

(a)

(b)
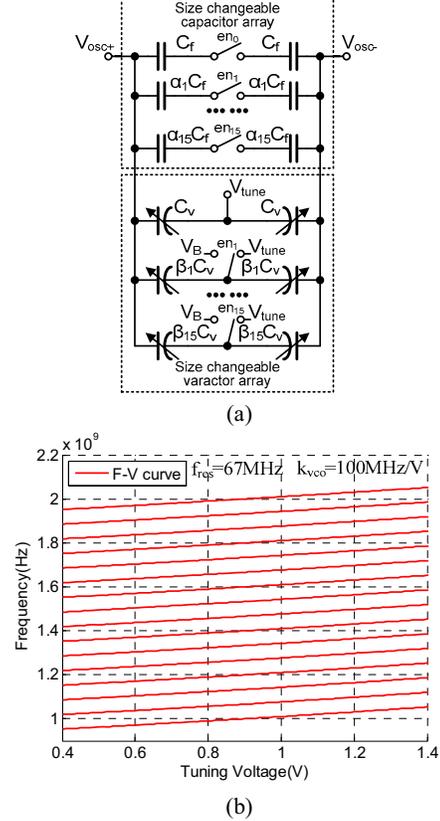
Fig. 3. Proposed topology (a) Size changeable capacitor and varactor array (b) F-V curve with constant VCO tuning gain and band step.

III. SOLUTIONS

A. Wideband VCO

To minimize the variations of both the analog tuning gain K_{VCO} and band step for wideband applications, a proposed architecture is shown in Fig. 3(a). The idea is to make both the size of capacitors and varactors changeable. Instead of using one fixed analog varactor and a binary weighted capacitor array, a number of capacitors and varactors with different values are adopted. At lower frequency band the gain K_{VCO} is low, so a majority of varactor units are connected to the analog control voltage, and other varactor units are connected to the power supply

or ground to get minimum fixed capacitance. On the contrary, at higher frequency band only a minority of varactor units are switched in. On the other hand, to obtain equal frequency band step, the fixed capacitors are also made changeable.

In this frequency synthesizer, a digital controlled capacitor array (DCCA) divides the whole tuning range into 16 sub-bands to keep a relatively low analog tuning gain, while an extra digital controlled varactor array (DCVA) is inserted to equalize the tuning sensitivity. Assuming α_i (i=1, 2, $\cdots$, 15) the capacitor ratio of DCCA units and β_i (i=1, 2, $\cdots$, 15) the varactor ratio of DCVA units, total capacitance $C_{tot,n}$ across the tank at the center frequency of the nth sub-band can be expressed as

$$C_{tot,n} = \begin{cases} C_P + C_f + (\beta_1 + \cdots \beta_{15})C_{V,\min} + C_{V(0.9)} & (n=1) \\ C_P + (1+\alpha_1 + \cdots \alpha_{n-1})C_f + (\beta_n + \cdots \beta_{15})C_{V,\min} \\ \quad + (1+\beta_1 + \cdots \beta_{n-1})C_{V(0.9)} & (n=2,\cdots,15) \\ C_P + (1+\alpha_1 + \cdots \alpha_{15})C_f + (1+\beta_1 + \cdots \beta_{15})C_{V(0.9)} & (n=16) \end{cases} \quad (2)$$

where C_P is the parasitic capacitance and $C_{V,\min}$ is the minimum capacitance of the varactor. Note that n=1 is the highest frequency band. Similarly, the tuning gain $K_{VCO,n}$ of the nth sub-band can be calculated as

$$K_{VCO,n} = \begin{cases} \dfrac{1}{4\pi\sqrt{LC_{tot,n}^{\;3}}} \cdot \dfrac{\partial C_V}{\partial V_{tune}}\bigg|_{V_{tune}=center} & (n=1) \\ \dfrac{1+\beta_1 + \cdots \beta_{n-1}}{4\pi\sqrt{LC_{tot,n}^{\;3}}} \cdot \dfrac{\partial C_V}{\partial V_{tune}}\bigg|_{V_{tune}=center} & (n=2,\cdots,16) \end{cases} \quad (3)$$

where $\partial C_V/\partial V_{tune}$ is the slope of C-V curve for varactor C_V at center frequency. Therefore, by setting α_i and β_i properly, the K_{VCO} and band step variations can be greatly reduced. The simulated F-V curve of the proposed architecture is shown in Fig. 3(b). During the frequency range from 1GHz to 2GHz, the frequency band step is 67MHz uniformly and K_{VCO} is 100MHz/V for each band.

B. AFC

Due to the nonlinearity of the C-V curve of the varactor, K_{VCO} of each frequency band can only be made equal in the middle of the tuning range. During a single F-V curve, the slope near the middle is linear and maximal. The AFC algorithm senses the VCO output center frequency of each band and compares it to the targeted value which is determined by the division ration. The band of which the center frequency is closest to the targeted value will be selected. As long as the overlapping ratio between two adjacent bands exceeds 50%, all output frequency points can fall near the middle of the tuning range and have rather linear tuning gains. In this way, the tuning gain variations can be minimized further.

C. Charge Pump

The frequency synthesizer alters its output frequency by changing division ratio N. So when N varies, the loop bandwidth changes and the loop characteristics are affected. Charge pump current I_{CP} can be programmed to match the division ratio. Some current banks can be in parallel with the major current sources and sinks to calibrate the total charging and discharging current. By compensating I_{CP}, the term I_{CP}/N can be a constant.

IV. EXPERIMENTAL RESULTS

A prototype is implemented and measured in 0.18-μm CMOS process. The measured phase noise at oscillation frequency of 1.6GHz is plotted in Fig. 4 and compared to the simulation result. The spot phase noise is –97.6dBc/Hz at 10kHz offset and -124.2dBc/Hz at 1MHz offset. The integrated phase error from 100Hz to 10MHz is 0.63° rms. The measured and simulated curves agree very well from 100Hz to 10MHz. Phase noise contributions of all blocks are also depicted for simulation results. Charge pump dominates at in-band and out-of-band phase noise is mainly determined by VCO. Phase noise plots at frequency offset of 10kHz and 1MHz are shown in Fig. 5. The curves have a flat characteristic across the whole output range, where the error is below 1dB. It is also shown that the closed-loop has an average measured bandwidth of 90kHz and the error is within ±10%.

Fig. 4. Comparisons of simulation and measured phase noise at the oscillation frequency of 1.6GHz.

The measured closed-loop output frequency is shown in Fig. 6, including 71 points of division ratio from 93 to 163. The tuning gain varies from 70MHz/V to 90MHz/V, of which the variation is only ±12.5% in such a wide frequency range of 825MHz. Due to the AFC operation,

the control voltages of all output frequency fall between 0.55V to 0.95V, which are in the linear gain region.

The die micrograph is shown in Fig. 7, which also includes measured performance summary. Table I presents a performance comparison with other frequency synthesizers recently reported for DVB applications.
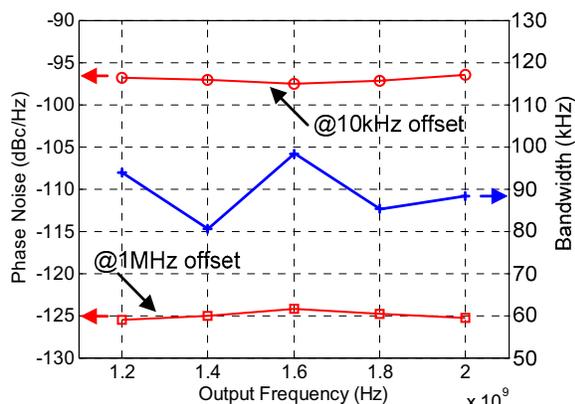
Fig. 5.   Measured phase noise and bandwidth.
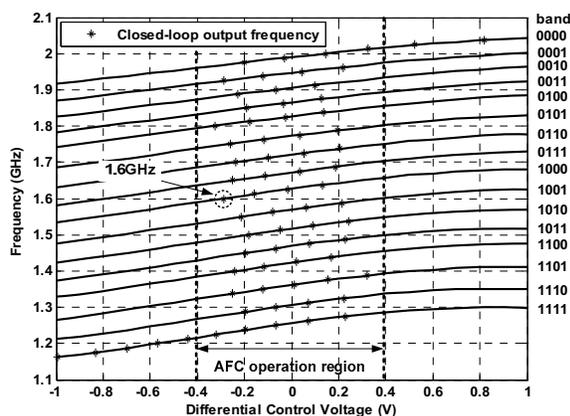
Fig. 6.   Measured tuning curves of 16 sub-bands.
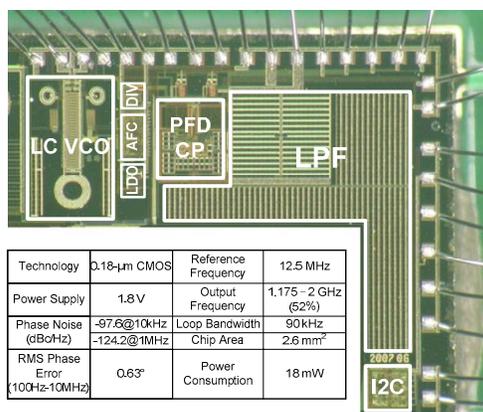
Fig. 7.   Die micrograph and performance summary.

Ref.	[6]	[7]	This Work
Output Frequency	2.24-4.48GHz	1.1-2.2GHz	1.175-2GHz
VCO type	Ring	Three LC	Single LC
Phase noise (dBc/Hz)	-98@100kHz -100@1MHz	-90@10kHz	-97.6@10kHz -124.2@1MHz
RMS phase error	0.8°	1.5°	0.63°
Power	132mW	N.A.	18mW
Technology	0.13-μm CMOS	0.18-μm CMOS	0.18-μm CMOS

V. CONCLUSIONS

Constant bandwidth is essential in phase noise optimization and loop stability for frequency synthesizers. Some techniques are presented to maintain the bandwidth over a wideband frequency range. A 1.175-2GHz synthesizer has been fabricated and validated in 0.18-μm CMOS process. It acquires flat phase noise characteristics across the whole tuning range with a power consumption of 18mW from a 1.8V supply.

ACKNOWLEDGEMENT

REFERENCES

[1] D. Saias, et al., "A 0.12μm CMOS DVB-T Tuner," *ISSCC Dig. Tech. Papers*, pp. 430-431, Feb. 2005.

[2] S. Levantino, et al., "Frequency dependence on bias current in 5-GHz CMOS VCOs: impact on tuning range and flicker noise upconversion," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1003-1011, Aug. 2002.

[3] John G. Maneatis, et al., "Self-biased high-bandwidth low-jitter 1-to-4096 multiplier clock generator PLL," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1795-1803, Nov. 2003.

[4] Floyd M. Gardner, *Phaselock Techniques*, Third Ed., New York: Wiley, 2005.

[5] D. Hauspie, E-Ch. Park and J. Craninckx, "Wideband VCO with simultaneous switching of frequency band, active core, and varactor size," *IEEE J. Solid-State Circuits*, vol. 42, pp. 1472-1480, July 2007.

[6] A. Maxim, R. Poorfard and J. Kao, "A sub-1.5°rms Phase-Noise Ring-Oscillator-Based Frequency Synthesizer for Low-IF Single-Chip DBS Satellite Tuner-Demodulator SoC," *ISSCC Dig. Tech. Papers*, pp. 618-619, Feb. 2006.

[7] M. Gupta, S. Lerstaveesin, D. Kang, et al., "A 48-to-860MHz CMOS Direct-Conversion TV," *ISSCC Dig. Tech. Papers*, pp. 206-207, Feb. 2007.