HIGH-PERFORMANCE ALL-DIGITAL QUADRATURE FREQUENCY SYNTHESIZER/MIXER

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ABSTRACT

In this paper, a high-performance all-digital quadrature frequency synthesizer/mixer applied to QAM modulation and demodulation is presented, which synthesizes 12-bit sine and cosine waveforms with a spectral purity of –83.0dB. The synthesizer covers a bandwidth from dc to 100 MHz in steps of 0.0466Hz with a corresponding switching speed of 5 ns at 200MHz clock frequency. Also, it is capable of frequency, phase and quadrature amplitude modulation. In this design, an efficient ROM look-up table method for calculating the sine and cosine function is employed, and a compression algorithm that only calculates one-eighth sine function is adopted to reduce the volume of ROM. By taking advantage of sine and cosine symmetries, the size of the ROM look-up table is only 1/51 of that of traditional one. The resulting chip fabricated in 0.35um five-level metal CMOS process has a complexity of about 20,000 gates with core area of 2.00×1.00 mm^2.

1. INTRODUCTION

TRADITIONAL high-bandwidth frequency synthesizers are based on phase-locked loop (PLL), and traditional high-frequency mixers are implemented in analog mixer technology. However, thanks to the CMOS technology progress, digital techniques are today capable of handling high frequency synthesizer/mixer. High performance quadrature frequency synthesizers/mixers play an extremely important role in modern digital communications. They offer many advantages including fast switching response, fine frequency resolution, large bandwidth, and good spectral purity. Meanwhile, in the past few years, improvements in digital-to-analog converter (DAC) technology have made quadrature frequency synthesizer/mixer feasible at RF frequency. So they become widespread in frequency agile communications system such as CDMA digital cellular telephones, spread spectrum wireless LAN's, HDTV. For example, a tunable quadrature amplitude modulation (QAM) modulator and demodulator are shown in Fig. 1.

The architecture (Fig. 2) of direct digital frequency synthesizer (DDFS) used in this design was originally introduced by Tierney, Rader, and Gold [1]. An overflowing L-bit accumulator is utilized to generate the phase argument of the sine and cosine function generator. Each overflow of the phase argument represents one period of a sine and cosine wave. The input Frequency Control Word (FCW) of the phase accumulator controls the frequency of the generated sine and cosine waveform.

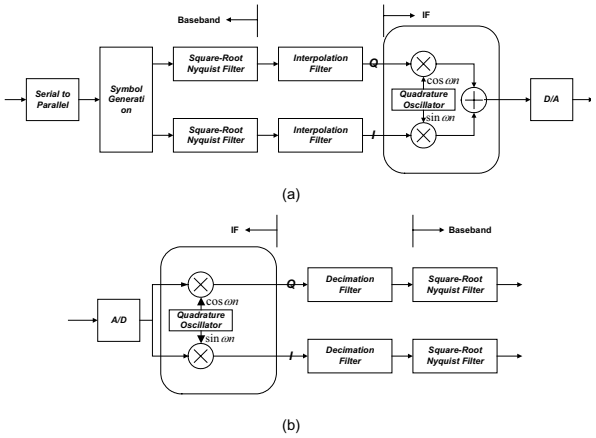

Fig. 1. Tunable QAM Modulator (a), and Demodulator (b)

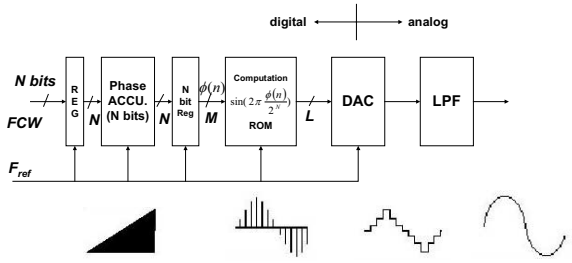

Fig. 2. Architecture of Direct Digital Frequency Synthesizer

The sine and cosine function generator is a ROM look-up table that stores the sine and cosine samples. Frequency resolution can be doubled by each addition of one bit to the word length of the phase accumulator.

For a given Frequency Control Word (FCW), clocking frequency (f_{clk}), and phase accumulator word length (L), the output frequency (f_{out}) of the synthesizer is given by

$$f_{out} = \frac{f_{clk} \cdot FCW}{2^L} \tag{1}$$

and the frequency resolution is given by

$$\Delta f = \frac{f_{clk}}{2^L} \tag{2}$$

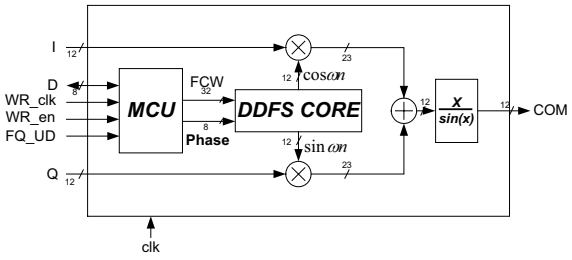

Fig. 3. Architecture of Quadrature Frequency Synthesizer/Mixer

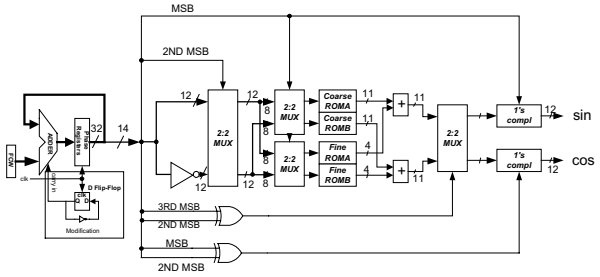

Fig. 4. Optimized Architecture of DDFS

In this paper, the word length of the phase accumulator is 32 bits and the maximum clock frequency is 200MHz. Thus the minimum frequency resolution is 0.0466Hz. The switching speed between two frequencies is one clock cycle, 5ns.

Fig. 3 is the architecture of the quadrature frequency synthesizer/mixer, which consists of four main modules: direct digital frequency synthesizer, modified Booth multiplier with Wallace adder tree, anti-SINC FIR filter with CSD coefficients and a simple microcontroller. Direct digital frequency synthesizer employs one-eighth sine waveform compression algorithms to achieve high frequency resolution and high bandwidth. 12-bit×12-bit multipliers adopt modified Booth encode and Wal-lace adder tree to improve the speed of multiplication. An anti-SINC FIR filter is used to compensate the loss of D/A converter's frequency response before D/A output. The coefficients of this filter are Canonic Signed-Digit (CSD) code, which utilize minimum shift-adder to complete multiplication operation avoiding many of complicated multiplications. The internal control word registers (such as FCW, Phase offset) are wrote or read through a simple microcontroller to reduce the number of I/O pads of control signals.

2. ARCHITECTURE DESIGN ISSUES

2.1 Direct Digital Frequency Synthesizer

This design is based on the optimized architecture of Nicholas and Samueli[2], Zhangwen Tang and Han Min[3]. The optimization of direct digital frequency synthesizer (DDFS) involves trading off the finite word lengths and sine computation methods against the sine-wave spectral purity and maximum clock rate. Fig. 4 shows a block diagram of DDFS in this design, which employs eighth sine waveform compression algorithms to decrease the volume of the ROM look-up table.

2.1.1 1/8 Sine Waveform Compression Technique

As we all known, arbitrary functions can be partitioned into coarse and fine ROM samples [2], [3], [4]. Let A+B+C be total number of bits of the phase address, with A being the most significant bits, B the next most significant bits, and C the least significant bits. Then using this algorithm, the coarse ROM would have 2^{A+B} samples, and the fine ROM would have 2^{A+C} samples. According to the conclusion in [4], A=4, B=4 and C=4 is optimal. The output word length of the coarse ROM is 11 bits,

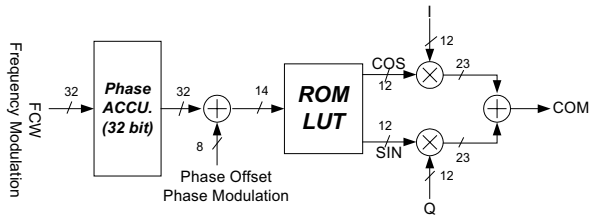

Fig. 5. Modulation Capabilities

and that of the fine ROM is 4 bits. Thus, $2^{14}\times12$ sine samples are compressed into $2^8\times11$ coarse samples and $2^8\times4$ fine samples resulting in a compression ratio of 51:1. Thus, by taking advantage of sine and cosine symmetries, the size of the look-up table ROM is only 1/51 of that of traditional one.

2.1.2 Quadrature Ouputs

For a design where quadrature outputs are desired, a simple method would be to store both sine and cosine samples from 0 to π/2. This would double the size of the ROM look-up table. Instead, one could take advantage of one-eighth wave symmetry of a sine and cosine waveform, since cosine samples from 0 to π/4 are the same as sine samples from π/4 to π/2. Similarly, sine sample from 0 to π/4 are the same as cosine sample from π/4 to π/2. Hence, one need only store sine and cosine samples from 0 to π/4. The third MSB of the phase accumulator can be used to select between these samples.

2.1.3 Modulation Capabilities

The modulation capabilities [5] of this chip include frequency modulation, phase modulation, quadrature amplitude modulation, and frequency mixing. Frequency modulation is performed directly by modulating the Frequency Control Word. Phase modulation is obtained by adding a phase offset to the phase accumulator output before addressing the ROM look-up table. Furthermore, this chip accepts only an 8-bit word for phase modulation. Finally, quadrature amplitude modulation and frequency mixing are obtained by adding a complex multiplier block to the sine and cosine outputs of the quadrature DDFS as shown in Fig. 5. The word length for I and Q rails for amplitude modulation are 12 bits each. The complex multiplier block is made up of two 12-bit×12-bit multipliers.

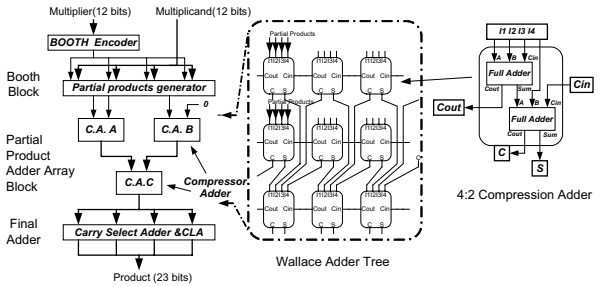

Fig. 6. 12bits×12bits Multiplier with Modified Booth Algorithm and Wallace Adder Tree

2.2 12-bit×12-bit Multiplier

The structure of 12-bit×12-bit multiplier is shown in Fig. 6. This multiplier uses a parallel structure with Booth's algorithm and Wallace's adder tree. The multiplier consists of the following three blocks: Booth block, adder array block and final adder. By applying the modified Booth algorithm [6], the number of partial products is halved. Since this multiplier performs 12-bit multiplications, 6 partial products are generated. By employing the Wallace adder tree and a 4:2 compressor adder [7], only two addition stages are needed in order to add 6 partial products. This addition is performed in the form of a tournament by using the Wallace adder tree method. The addition of the partial products uses the 4:2 compressor adder, which can sum up four partial products concurrently. The 4:2 compressor adder can add without propagating the carry to a higher position, and it generates a 23-bit sum and carry.

Finally, the 23-bit sum and carry is added with the 23-bit carry propagation. This adder consists of a 4-bit carry look-ahead adder and an 8-bit carry select adder to propagate the carry at high speed.

2.3 Anti-SINC FIR filter

Digital-to-analog (D/A) converters introduce an inherent sin(x)/x amplitude distortion (Fig.7a) into the spectrum of signals being converted. For many systems, the performance degradation due to this distortion is not acceptable and compensation is required. A digital compensation filter prior to D/A conversion has the advantage that the x/sin(x) (Anti-SINC) compensation is accurate for all sampling rates.

In this paper an 11-tap x/sin(x) linear-phase FIR digital filter [8] is used, as shown in Fig. 7b. A transpose-form structure with 2-digit CSD coefficients to each tap is chosen for the realization of the compensation filter. Therefore, each tap multiplier is implemented with at most a single adder/subtracter and some hard-wired shifts. A carry save addition (CSA) scheme is used for the implementation of the adders to avoid carry propagation. And pipeline registers were inserted after every adder stage. Consequently, the critical path consists of only a single full-adder

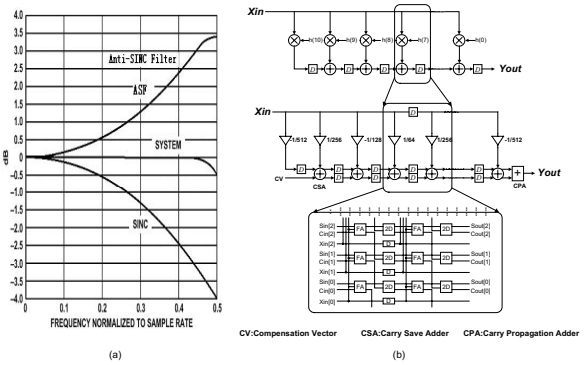

Fig. 7. (a) SINC Amplitude Distortion,
(b) Transpose-form Realization of 11-tap Anti-SINC FIR Filter

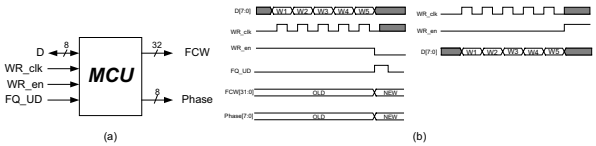

Fig. 8. (a) Simple Microcontroller,
(b) Timing Diagram of Read and Write

and a pipeline register. Therefore, this FIR filter can work in high clock rate.

2.4 Simple microcontroller

In order to reduce the number of pads of controlling signals, a simple microcontroller (Fig. 8a) is used to write and read 32-bit Frequency Control Words and 8-bit phase offset. The timing diagram of this simple microcontroller is shown in Fig. 8b. The 40-bit controlling registers are wrote and read in 5 clock cycles through 8-bit bidirectional data bus. WR_clk, WR_en and FQ_UD are clock signal, enable signal and update signal separately.

3. CIRCUIT AND LAYOUT DESIGN ISSUES

The whole chip was designed using VHDL language in Active-HDL4.2 environment. Top-Down design methodology was adopted to design the whole chip in RTL design stage. In logic synthesis stage, Bottom-Up design methodology was employed in Synopsys design compiler environment. Each module of the whole chip was synthesized in Europractice 0.35-um CMOS standard cell library. Top circuit was shown in Fig.9a. And each module was placed&routed in Cadence Silicon Ensemble. The floorplan of whole silicon chip is Fig.9b. The resulting chip fabricated in 0.35um five-level metal CMOS process has a complexity of about 20,000 gates with core area of 2.00×1.00 mm^2. The photomicrograph of the packaged chip is shown in Fig. 10.

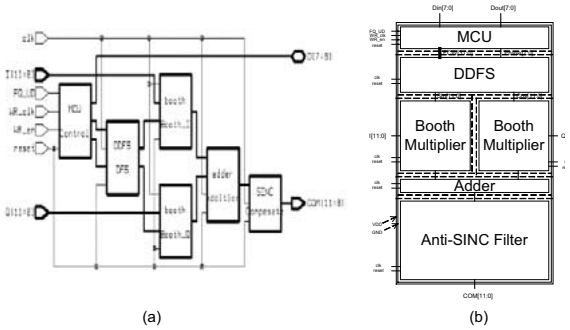

Fig. 9 (a) Top Circuit of the Whole Chip,
(b) Floorplan of Layout

4. SIMULATION AND MEASUREMENT

To verify the chip functionality, cosimulations with a synthesizable testbench were run in software and hardware environments. We built a test board with two FPGA chips (Xilinx SpartanII and Virtex), one for generating stimulus signals, another for sampling the outputting signals. It should be mentioned that due to parasitic effects on the PCB, we were not able to conduct the measurements up to 200MHz. Instead, we used a lower master clock of 100MHz. The 50-MHz mode was measured completely. Fig.11 was the FFT diagram of outputting signal. In Fig.11, the worst-case spurious component is at –83.0 dB.

5. CONCLUSION

An implementation of a high-performance all-digital quadrature frequency synthesizer/mixer is presented. It has been designed that operates at 200MHz and synthesized –83.0 dBc spectrally pure sine and cosine waveforms. By taking advantage of sine and cosine symmetries, the size of the ROM look-up table is only 1/51 of that of traditional one. The chip is capable of frequency, phase and quadrature amplitude modulation. The resulting chip fabricated in 0.35um five level metal CMOS process has a complexity of 20,000 gates with core area of 2.00 $\times$1.00 mm^2.

6. ACKNOWLEDGMENT

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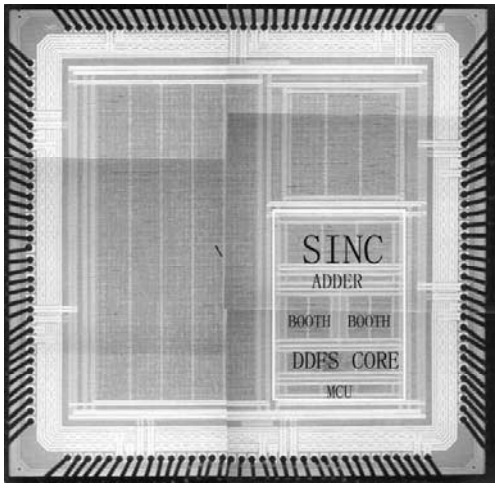

Fig. 10. Photomicrograph of the Packaged Chip

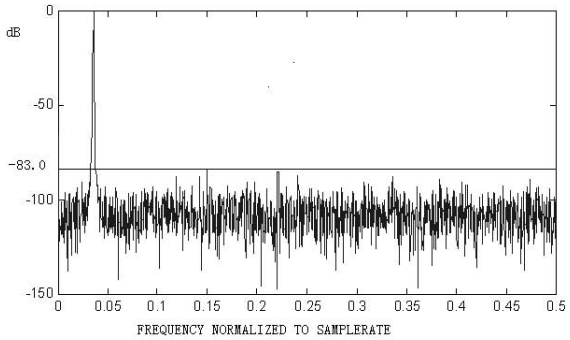

Fig. 11. FFT Diagram of Outputting Signal

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