Standard *CMOS* Technology On-chip Inductors with *pn* Junctions Substrate Isolation

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Abstract- New substrate isolation structures using pattern stacked *pn* junctions for on-chip inductors in standard *CMOS* technology are presented. For the first time, through increasing the reverse bias voltage to *pn* junctions, the lower substrate eddy loss due to the *pn* junction substrate isolation is reliably validated and the maximum quality factor is improved by 19%. The inductor without substrate shielding layer is compared to the inductor with metal one pattern ground shielding, pattern *n*-well, n^+ diffusion, dual *pn* junctions isolation.

I. Introduction

Monolithic inductor is an important component in highly integrated radio frequency circuits for wireless communication systems. The inductor designers aim at realizing a substantially greater quality factor at circuit operation frequency without altering the fabrication process, such as a symmetric inductor that is excited differentially.

In this paper, the stacked *pn* junctions substrate isolation structures (***JSIS***) are developed. Reducing substrate losses due to ***JSIS*** are validated. The ***Q*** and self-resonant frequency (f_{SR}) of the inductor with the different substrate isolation are analyzed.

II. *pn* Junctions Substrate Isolation

The substrate loss is caused by the eddy currents (***EC***) and capacitive coupling substrate currents (***CCSC***), which is induced by electromagnetic coupling to the substrate as shown in Fig. 1. 90% of magnetic energy is dissipated within a depth of 10μm below the substrate surface [1]. To prevent the occurrence of such an energy loss mechanism, the stacked *pn* junctions substrate isolation structures inserted above or in substrates were proposed.

Most of substrates in standard ***CMOS*** technology are *p* semiconductor. The *pn* junction can be formed at the interface between n^+ diffuse layer / *n*-well and *p* substrate as shown in Fig.1 (a), (b), which call ***NP*** and N^+P, respectively. For single well technology, vertical dual *pn* junctions (P^+NP) can be formed by diffusing p^+ on the *n*-well as shown in Fig. 1(c). For deep *n*-well technology, vertical dual *pn* junctions (***PNP***) can be made by forming *p*-well on the deep *n*-well as shown in Fig. 1(d), and vertical three *pn* junctions (***NPNP***) can be formed on the base of ***PNP*** by diffusing n^+ on the *p*-well as shown in Fig. 1(1). The junction capacitance would be formed in series with the oxide capacitance between the inductor and the silicon substrate, thus the equivalent $C_{m\text{-}s}$ is greatly reduced.

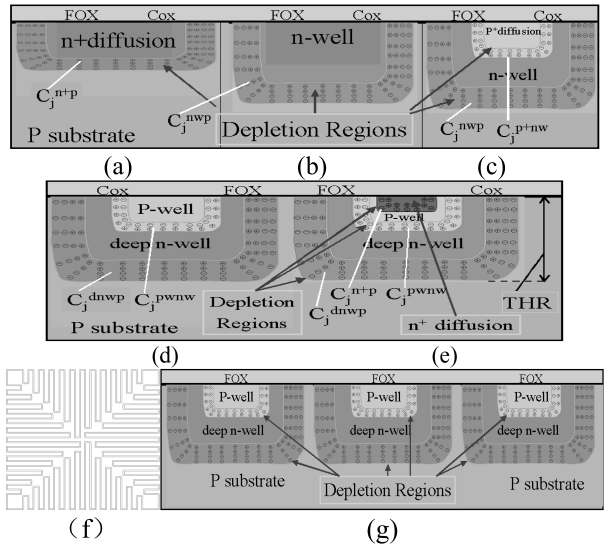

Fig.1. *pn* junction substrate isolation structures

Fig.1 (f) and Fig.1 (g) are the planform and cross section of the dual *pn* junctions substrate isolation, respectively. The resistance of the p^+/n^+ diffusion or well is less than that of substrate. The *pn* junction must be made to pattern like metal ground shielding in order to protest again eddy current. Thus, the thickness of high resistance (***THR***) is equivalent to the depth of the bottom pn junction in substrate as shown in Fig.1 (e). The structures can interrupt the flowing path of the induced current, thus reducing energy loss.

Fig. 2 is the lumped elements model of a two-port on-chip inductor.

III. Experiment and Discussions

Inductors have been fabricated in a 0.35μm four metal ***CMOS*** processes.

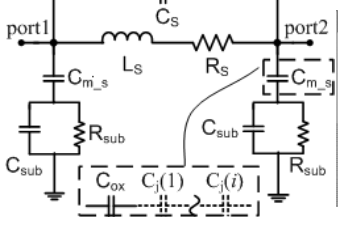

Fig. 2. Lumped elements model of a two-port on-chip inductor

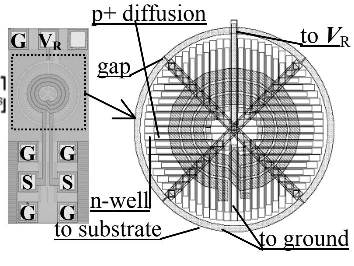

Fig. 3. A single-end spiral inductor with ***PNP*** isolation structure

A. Eddy Currents Loss

The die photo and layout of the ***PNP*** substrate structure is shown in Fig. 3. The *p*-substrate and p^+ diffusion are connected to ground while *n*-well is connected to bias voltage ($\boldsymbol{V}_R$). Thus electric field of inductor are terminated at p^+ diffusion, the *pn* junction capacitor does not have effect on the parasitical capacitance and f_{SR} of the inductor in order to validate the effect on lowering eddy current loss. Ohmic loss from the eddy currents is only substrate loss.

Quality factors and self-resonant frequency of the inductor with *n*-well voltages are shown in Fig.4. Increasing the voltage applied to the *n*-wells increases the depletion region laterally between them, and vertically beneath them. With rising ***THR***, the substrate eddy currents are reduced, therefore, *L*s is increased and *R*s is decrease. Thus, the maximum quality factor is increased with V_R from 0V to 3V by further 19% and the frequency of the maximum ***Q*** (f_{MQ}) and f_{SR} of the inductor are reduced because the reduced quantity of the inductance due to eddy currents is decreased. From 4V V_R the depletion regions of two adjacent *n*-wells touch and the lateral *pn* junction dies away at 7V V_R and the ***THR*** is not the depth of the bottom pn junction in substrate only but the relatively thinner thickness of the depletion of the *pn* junction (Note: Source voltage of the technology is 3.3V). So the results from increasing V_R from 3V to 7V are reverse to the results from increasing V_R from 0V to 3V.

B. Quality Factor and Self-resonant Frequency

Thickness of the FOX under inductor with *pn* junctions layer is thinner than that of the FOX under inductor without *pn* junctions layer, so the $\boldsymbol{C}_{ox}$ increases. But vertical *pn* junctions capacitors are serially connected with the oxide capacitance between the inductor and the silicon substrate, the decrement of the parasitical capacitance due to *pn* junctions approximately counteract the increment of the $\boldsymbol{C}_{ox}$. *pn* junctions substrate isolation lower the eddy currents loss inductor, therefore, the inductance increase because that the reduced quantity of the

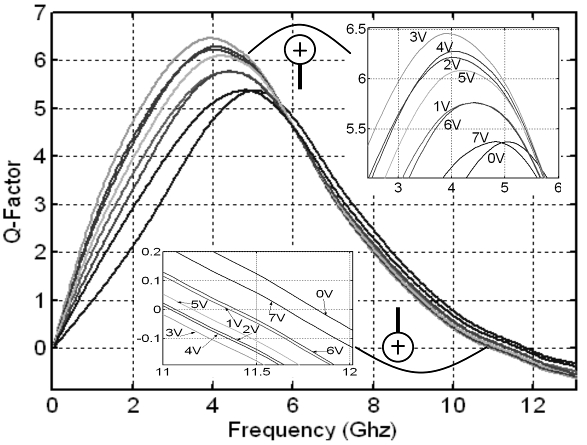

Fig. 4. Quality factors of the inductor with *n*-well distance 1.1 μ m and at *n*-well different bias voltages

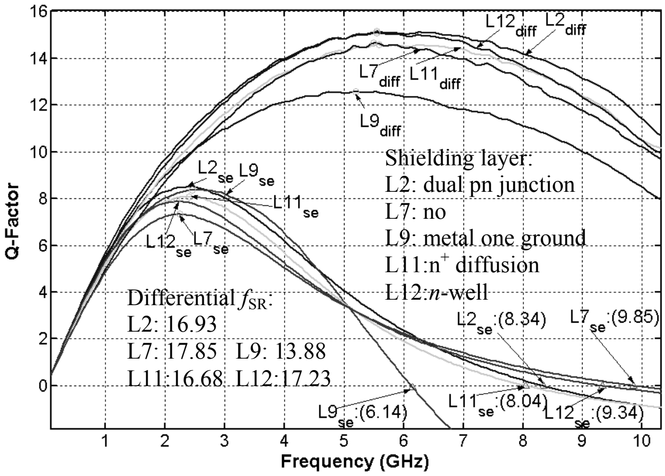

Fig. 5. The ***Q*** and ***SRF*** of the same inductor with the different pattern shielding (subscript se and diff represent single-end and differential, respectively)

inductance due to eddy currents is decreased. Hence, ***Q*** of the inductor with ***JSIS*** are lager than that of the inductor without ***JSIS***. According to (2), the difference of the f_{SR} of the inductor with ***JSIS*** and without ***JSIS*** is indistinctive, especially at differential f_{SR}, as shown in Fig. 5. The results are different from previous report [2] that *pn* junction substrate isolation can increase the f_{SR} of the inductor.

IV. Summary and Conclusions

New substrate isolation structures using pattern stacked *pn* junctions for on-chip inductors in standard *CMOS* technology are presented. Thus depletion layers lower the ***CCSC*** and ***EC***, reduces substrate loss, and the ***Q*** factor of inductor is improved.

The ***Q*** of the inductors with ***JSIS*** are lager than that of the inductor without ***JSIS***. However, the difference of the f_{SR} of the inductor with ***JSIS*** and without ***JSIS*** is indistinctive, especially at differential f_{SR}.

Acknowledgments

The authors would like to thank Prof. Lingling Sun, Jincai Wen, Zhanfei Chen and Prof. Fuxiao Li for measurements.

References

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