A Wideband CMOS Variable Gain Low Noise Amplifier Based on Single-to-Differential Stage for TV Tuner Applications

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***Abstract*—A wideband CMOS variable gain low noise amplifier (VGLNA) used for TV tuner is presented. A single-to-differential (S2D) circuit other than an off-chip balun is applied for high gain mode and a resistive attenuator is for five steps (6dB per step) attenuation in low gain mode. The performance of S2D, especially the noise factor is analyzed. The chip is implemented in a 0.18-μm 1P6M mixed-signal CMOS process. Measurements show that in the 50-860MHz frequency range, the VGLNA achieves 15dB maximum gain, 31dB variable gain range, a minimum 3.8dB noise figure and 2.6dBm IIP3 at 15dB gain while consumes 5.7mA from a 1.8V supply.**

***Index Terms*—LNA,S2D,Attenuator,Wideband,Tuner,Balun**

I. Introduction

Although many efforts have been exerted, implementation of fully integrated chip for TV tuner application is still a great challenge, to the standard of DVB-C (50M-860MHz) for example. Recent works on wideband LNA [1-2] based on off-chip balun have shown good performances, such as low NF, high linearity and excellent input matching. However, the off-chip balun adds extra cost, loss and much PCB size; meanwhile, an on-chip passive balun may account for large die area and not be acceptable for low frequency and wideband applications.

Thus, a single-to-differential stage (S2D) [3-6] is adopted in order to replace the balun for less area and cost without degrade the performances. Ref [3] has made S2D a part of the RF front-end, however, an off-chip inductor is applied and performance analysis of the S2D is not given. In [6], a balun-LNA is presented with excellent performances for less gain and phase error, but it can not maintain the performances at 50MHz and in high input levels situation; a capacitive attenuator is employed in [9], but it needs an extra circuit for input matching and the scheme requires one Gm-stage for each attenuation. In this paper, a fully integrated wideband LNA based on S2D with resistive attenuator for TV tuner applications is implemented.

A double-conversion low-IF (DLIF) DVB-C tuner RF architecture is shown in Fig.1. The LNA based on S2D stage is used as a replacement of traditional scheme which employs differential LNA with an off-chip balun.

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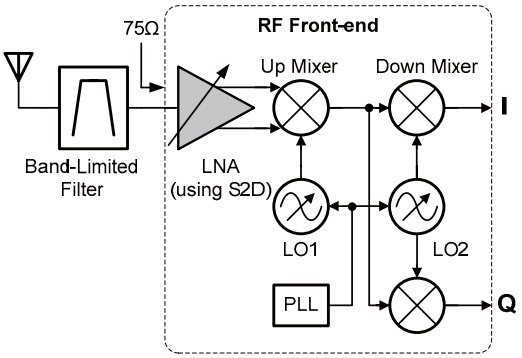

Fig. 1 A fully integrated tuner architecture using S2D

This paper is arranged as follows: the performances of S2D are analyzed in section II; we then turn to attenuator design in section III; the architecture of LNA is given in section IV; section V shows the chip implementation and measurements; the last section is for conclusion.

II. Single-to-Differential Stage

A. Introduction of S2D Stage

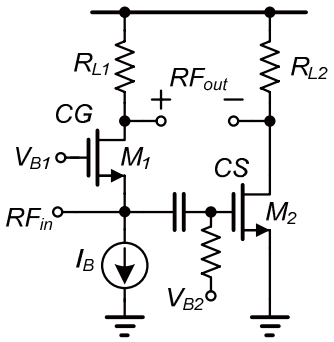

Fig. 2 A well-known schematic of single-to-differential circuit

A traditional well-known S2D circuit is shown in Fig.2. In this circuit, M_1 is configured as a common gate (CG) stage for positive amplifier with its load R_{L1}, the CG stage also provides input impedance matching over a wide range of frequency; M_2 together with R_{L2} is as a common source (CS) stage to offer a same amplitude but anti-phase output signal compared to the CG stage. The output differential signal could be sent to the following stage such as an up-conversion

mixer in Fig.1. I_B is a current bias for CG stage and can be replaced by an off-chip inductor [3-4] or a resistor [6].

It has found that the S2D circuit in Fig.2 can achieve a low NF because the noise originated from M_1 appear to be common-mode at the differential outputs [5], thus it can be greatly restrained if the S2D stage is followed by a fully differential circuit with high CMRR.

A modified S2D circuit is given in Fig.3. Here, M_1 is for CG stage and input matching, M_4 is for CS amplifier. M_2 and M_5 are used as MOS loads to improve linearity [7]. C_1 together with R_1 forms a high pass positive path for gain enhancement and makes sure that M_1 can be in saturation for a higher gain. The configuration of C_1 with R_1, M_1 with M_2 can reduce noise originated from M_1 [8]. For integration, M_3 is applied as a current bias for CG stage, obviously, it adds a part of noise to output, and the impact on the noise performance will be discussed next.

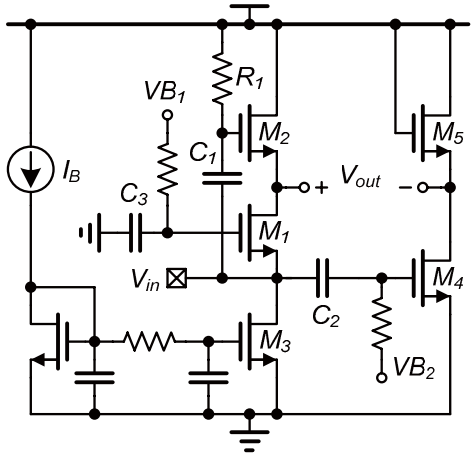

Fig. 3 Proposed S2D Circuit

B. *Performance Analysis*

1) Input matching

If C_3>>C_{gs1}, the input impedance of the S2D is

$$Z_{in}=\left(g_{m1}+sC_{gs1}+sC_{gs4}\right)^{-1} \tag{1}$$

Set g_{m1}=1/R_S for wideband input matching without taking care of the effect of input capacitances, however, as frequency increases, the input impedance will be greatly affected by the gate-source capacitances of M_1 and M_4, thus the dimensions of M_1 and M_4 should keep small enough for good input matching. Unfortunately, a small dimension will bring much impact of flicker noise at 50MHz. As a tradeoff between input matching and noise figure, a minimum length of 0.35-μm is adopted for M_1-M_2 and M_4-M_5 here.

2) Gain of the S2D stage

The voltage gain of differential output versus single-ended input can be represented as

$$A_V=\frac{V_d}{V_s}=\left(1+\frac{g_{m1}}{g_{m2}}+\frac{g_{m4}}{g_{m5}}\right)\frac{1}{1+g_{m1}R_S} \tag{2}$$

The first part in parentheses is for RC path to positive output, the second is due to CG stage and last part is the gain of CS stage. For balanced output applications, the amplitudes of positive and negative outputs should be equal

$$1+\frac{g_{m1}}{g_{m2}}=\frac{g_{m4}}{g_{m5}} \tag{3}$$

3) Noise Factor

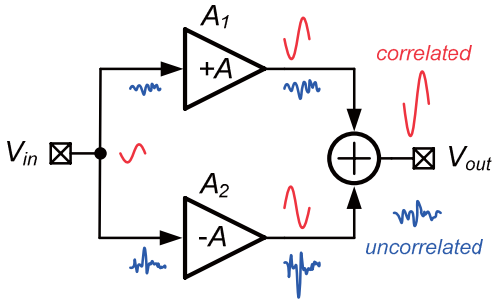

Fig. 4 Noise figure analysis for S2D

A simple way of analysis for S2D in Fig.2 or Fig.3 is given in Fig.4. The differential signal amplified by A_1 and A_2 is correlated and doubles in amplitude when added if a same gain is assumed for A_1 and A_2. The noises originated from the two amplifiers are uncorrelated and should be superposed in power [7], thus the SNR_{out} is improved compared to a simple amplifier. The noise factor is calculated to be

$$F=1+\frac{\overline{V_{out,n1}^2}+\overline{V_{out,n2}^2}}{\left(2A_V\right)^2 4kTR_S} \tag{4}$$

Here, $V_{out,n1}$ is output noise from A_1 and $V_{out,n2}$ is output noise of A_2 under the CG input matching. The same gain is A_V and R_S represents the source impedance. Apply the noise factors of the two stages, an alternative expression is

$$F=1+\frac{F_1-1}{4}+\frac{F_2-1}{4} \tag{5}$$

Here, F_1 is noise factor of A_1 and F_2 is of A_2. The derived noise factor can be seen in (6) with substitution of the noise factors of CS and CG stage respectively. Noise from M_3 is not included here.

$$F=1+\frac{\gamma_1\left(R_S-g_{m2}^{-1}\right)^2}{4R_S A_V^2 g_{m1}^{-1}}+\frac{\gamma_2}{A_V^2 g_{m2}R_S}+\frac{\gamma_4 g_{m4}}{A_V g_{m5}^2 R_S}+\frac{\gamma_5}{A_V^2 g_{m5}R_S} \tag{6}$$

Using small-signal model for each noise source in Fig.3 (M_1-M_5) under the conditions of (2) and (3), the actual noise factor of Fig.3 can be represented as

$$F=1+\frac{\gamma_1}{A_V^2}+\frac{\gamma_2}{A_V^2 g_{m2}R_S}+\gamma_3 g_{m3}R_S+\frac{\gamma_4 g_{m4}}{A_V g_{m5}^2 R_S}+\frac{\gamma_5}{A_V^2 g_{m5}R_S} \tag{7}$$

The second term in (6) is different with (7) because the noise from M_1 can also be a correlated output at CS stage and noise of M_3 can be seen as an outside input noise in (6), thus (6) and (7) will coincide. According to simulation, the main sources of noise come from M_4, M_2 and M_3, it is a tradeoff between power dissipation and low noise figure.

III. Attenuator Design

Passive attenuator is often used to deal with high input levels ahead of LNA without adds much non-linearity in order to achieve high dynamic range [9] when nonlinearity becomes a dominate factor for deterioration of SNR. The attenuator based on resistors has excellent linearity and accounts for less area, impedance matching can be available alone.

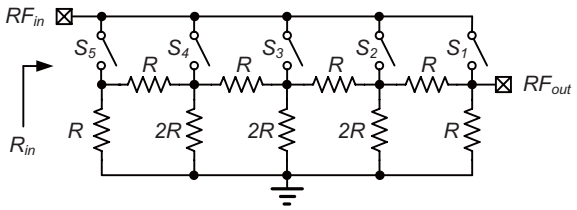

Fig. 5 A five steps resistive attenuator

Fig.5 shows a resistive attenuator with five gain steps. Attenuation is realized by controls of switches S_1-S_5. The switch is implemented by NMOS with minimum channel length and the resistors are implemented by active n-diffusion resistors with flat resistance response over the bandwidth. When one of the switches is on, the impedance seen from RF_{in} is a constant, given as

$$R_{in} = \frac{2}{3}R \tag{8}$$

If the source impedance is 75Ω, the value for R in Fig.5 can be calculated to be 112.5Ω.

IV. Architecture of LNA

The whole simplified LNA is shown in Fig.6, $S2D_1$ is used for low noise figure and input matching at 15dB fixed gain when the attenuator and $S2D_2$ is shut down. Attenuator with $S2D_2$ is in the low gain path for attenuation and input matching when $S2D_1$ is disabled, the gain step is 6dB. C_1 is an AC-coupled capacitor for $S2D_2$ and should be chosen large enough to avoid much gain loss at 50MHz. The outputs are switched between the two different work modes. In this scheme, only two S2D stages are used.

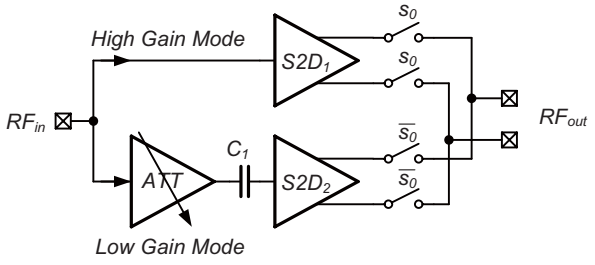

Fig. 6 Simplified schematic of VGLNA

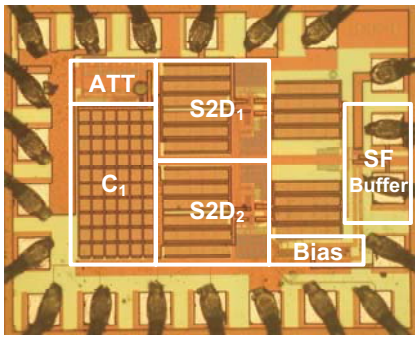

Fig. 7 Die Microphotograph of the Wideband LNA

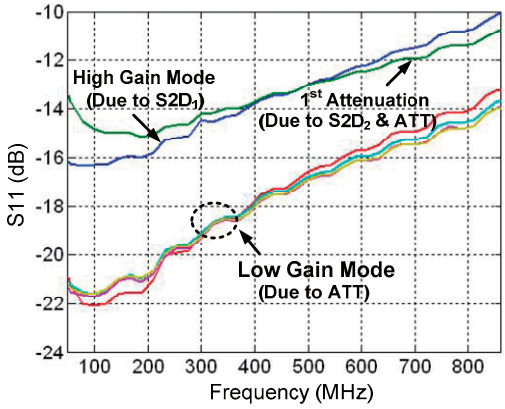

Fig. 8 Measured input return loss (S11) versus frequency

V. Chip Implementation and Measurement

The chip was fabricated in a 0.18-μm 1P6M mixed-signal CMOS process and the microphotograph is shown in Fig.7. The total area of this VGLNA is 0.6×0.48 mm^2 excluding all the ESD protected PADs and source follow buffers.

Input return loss (S11) is measured and plotted in Fig.8. Due to input capacitances, the S11 degrades as the frequency increases; however, the curves of S11 at all gain steps are still below -10dB over the whole bandwidth.

Measured NF is 3.8-5.0dB from 50-860MHz as shown in Fig.9, the increment of NF at high frequency is due to output mismatch and gain drops, while at 50MHz, the contribution of flicker noise grows rapidly.

IIP3 illustrated in Fig.10 is 2.6dBm and IIP2 is 8.6dBm at 15dB gain with two-tone tests. The input referred 1dB compression point is -6dBm which is in accordance with the simulated -5.8dBm.

Measurements show a maximum gain of 15dB and the gain step is about 6dB.The NF and IIP3 as function of gain control steps are given in Fig.11. It can be seen that NF increases from 4.2dB to 35.4dB and IIP3 increases from 2.6dBm to 24.6dBm as the gain drops from 15dB to -16dB at the frequency of 500MHz. IIP3 is limited by non-linearity of input NMOS switch (S_i in Fig.5) if it exceeds 20dBm.

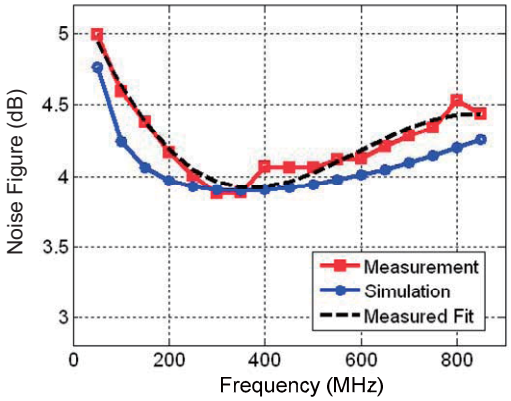

Fig. 9 Measured and simulated NF at 15dB gain

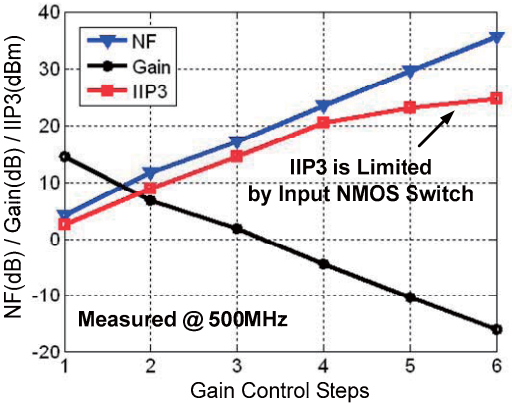

Fig. 11 Measured NF / Gain / IIP3 at all gain steps

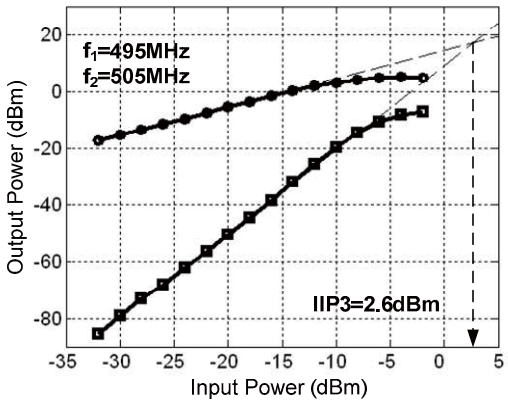

Fig. 10 Measured IIP3 at 15dB gain

TABLE I
Summary of Measurements & Performance Comparison

	[3]	[9]	[10]	This work
Technology	0.18μm CMOS	0.18μm CMOS	SiGe BiCMOS	0.18μm CMOS
Supply (V)	1.8	1.8	2.9	1.8
BW(MHz)	470-860	470-870	473-767	50-860
S11(dB)	<-10	<-11	N/A	<-10
Gain(dB)	25	16	19	15
NF(dB)	4.5	4.3	2.7	4.2
IIP3(dBm)	-4	-1.5	-14	2.6
Power(mW)	16	22	25	10
Area (mm^2)*	0.52	0.32	N/A	0.29
FOM	0.143	0.072	0.008	1.117

* The PADs are not included.

VI. Conclusion

In this paper, a CMOS wideband variable gain low noise amplifier based on S2D stage is presented; a resistive attenuator is employed to realize a 6dB gain step and input matching in low gain mode. Measurements show that in 50-860MHz frequency range, the VGLNA achieves good input matching (S11<-10dB), an average noise figure of 4.2dB, 15dB maximum gain, 31dB variable gain range and an IIP3 of 2.6dBm at 15dB gain while it only draws 5.7mA from a 1.8V supply.

Table I has summarized the measurements of this VGLNA, performance comparison is also given. Among all the works without off-chip balun used for TV tuner applications, this work provides a moderate NF, a much higher IIP3 and consumes less power with less die area.

For comparison between the works listed here, a FOM is introduced [1]

$$FOM = \frac{Gain \cdot IIP3}{P_{dc} \cdot (F-1)} \cdot \frac{BW}{f_c} \quad (9)$$

In (9), *Gain* and *F* are in absolute values, *IIP3* and P_{dc} are in milliwatts and the bandwidth is replaced by BW/f_c. This work achieves a better FOM compared with the other works, as can be seen in TABLE I.

Acknowledgment

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