An Accurate 1.08-GHz CMOS LC Voltage-Controlled Oscillator

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Abstract — An accurate 1.08-GHz CMOS LC voltage -controlled oscillator is implemented in a 0.35μm standard 2P4M CMOS process. In this paper we present a new convenient method of calculation of oscillating period. With this period calculation technique, the frequency tuning curves agree perfectly with the experiment. At a 3.3-V supply, the LC-VCO measures a phase noise of –82.2 dBc/Hz at a 10kHz frequency offset while dissipating 3.1mA current. Chip size is 0.86mm × 0.82mm.

I. INTRODUCTION

The explosive growth in wireless communications has driven universities and companies to produce wireless transceivers at low-cost, low-power, and compact size. Recently, all of RF components, such as low-noise amplifiers (LNAs), mixer, local oscillators (LOs), and IF Filters, seem possible to be integrated in CMOS scaled technology. On-chip passive elements such as spiral inductors and varactors make on-chip implementation of LC-tank voltage-controlled oscillators (VCOs) easy.

A complementary cross-coupled negative-G_m LC-tank oscillator is shown in Fig. 1, which employs both NMOS and PMOS cross-coupled pairs. Many published papers [1]-[3], have employed this type of LC-tank VCO, but oscillator's tuning curves were obtained from SPICE simulations or measurements. The prediction of oscillator's tuning curves is quite challenging due to highly nonlinear characteristics of varactors. A numerical method is shown in [3], but it is quite complex and time-consuming. The tuning curves must be numerically computed again if bias current changes.

In this paper, we investigate the I-V locus of step-like MOS varactors in a LC-VCO and predict the tuning curves through the oscillating period calculation of a serial LC tank in time domain [4], [9]. An accurate 1.08-GHz CMOS LC voltage-controlled oscillator is implemented in a 0.35μm standard 2P4M CMOS process. The theoretical analyses agree perfectly with the simulation and measurement of a CMOS complementary LC-tank VCO.

II. CIRCUIT DESIGN

The complementary cross-coupled negative-Gm LC-tank voltage-controlled oscillator in Fig. 1 has been implemented in 0.35μm 2P4M 3.3V CMOS process. On-chip spiral inductor is a symmetric differential multilayer inductor. Four metals are parallelly and serially connected with a lot of vias to decrease the serial resistor of spiral inductor and increase the inductance in unit silicon area. And a center-connected

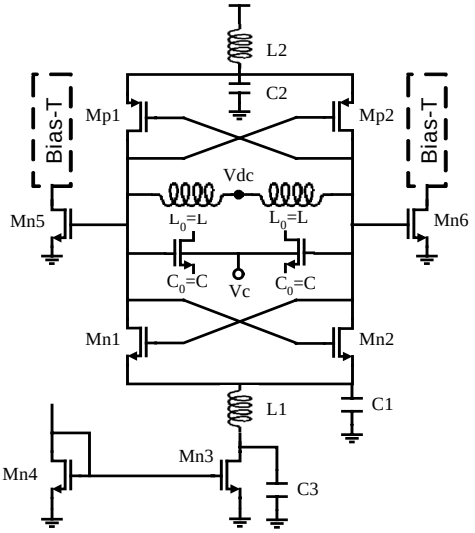

Fig. 1. CMOS complementary cross-coupled LC-tank VCO

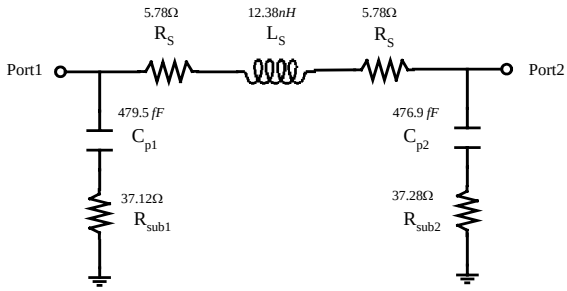

Fig. 2. PI model of on-chip spiral inductor

patterned ground shield (PGS) is employed to improve quality of inductors at low frequency (1-2GHz) [5]. On-chip differential spiral inductor is 12.4nH, so the single-end inductor features 6.2nH. The maximum Q arrives seven at 1.1GHz. The compact equivalent pi model shown in Fig. 2 is extracted with ASITIC [6].

The transconductances of cross-couple NMOS and PMOS devices are chosen to be equal so that DC voltage of LC-tank oscillator is maintained at approximately $V_{dd}/2$. First, the oscillating waveform can have the maximum swing. Secondly, the VCO gain (K_V) can decrease and the phase-noise performance can be improved. The MOS devices are implemented using the minimum gate length (0.35μm). The open-drain NMOS devices are the output buffers, which is used to drive the off-chip Bias-T circuits. In order to decrease the Miller-effect capacitor, the length of open-drain NMOS devices is 60μm. The lengths of current-mirror are larger than the minimum length so that the channel length modulation (CLM) is attenuated and 1/f noise is decreased.

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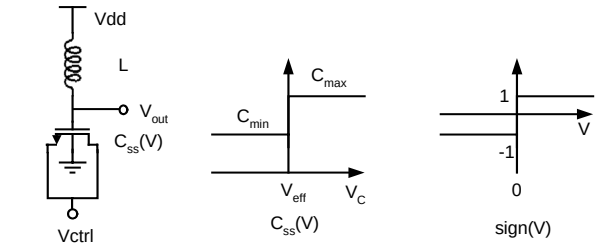

(a) Serial LC Tank (b) Step-like Varactor (c) Unit Step Function

Fig. 3. Serial LC-tank and step-like varactor

Two additional inductors, L1 & L2, resonate at double frequency with the parasitic capacitors C1 & C2 at each common-source node, to avoid Q-degradation by triode region MOS transistors in the stacked differential pairs [7]. The filtering capacitor C3 is used to low the 1/f noise and effect of channel length modulation (CLM) [1].

III. FREQUENCY TUNING CHARACTERISTIC

Most of varactors used in LC-tank VCO circuits are Inversion-MOS (I-MOS) and Accumulation-MOS (A-MOS). Their characteristics both are step-like, and have large nonlinearity. The tuning curves of an LC-VCO will substantially deviate from the ideal curve $1/\sqrt{LC}$ when a step-like varactor is used [3]. Both I-MOS and A-MOS are step-like capacitors (Fig3. (b) and (c)). The small-signal capacitance is given by,

$$C_{ss}(V) = \begin{cases} C_{max} & V \geq V_{eff} \\ C_{min} & V < V_{eff} \end{cases} \quad (1)$$

where $V_{eff} = V_G - V_{ctrl} - V_{TH}$ is *effective control voltage* (ECV).

The presence of on-chip inductors in Fig. 1 imposes that the dc value of differential oscillating voltages has to be a constant voltage V_{dc}. Neglecting the tank losses in on-chip inductors and varactors, the half circuit of LC-tank VCO can be considered as a serial LC-tank structure (Fig. 3(a)). The value of inductor is L, and the step-like varactors can be mathematically represented as below,

$$C_{ss}(V) = \frac{1}{2}(C_{max} + C_{min}) + \frac{1}{2}(C_{max} - C_{min})\, sign(V - V_{eff}) \quad (2)$$

Fig. 4 shows the oscillating voltage waveforms of the serial LC tank simulated in HSPICE. Each waveform consists of two segmental sinusoids with different size, which join at the effective control voltage (ECV). With the ECV from low to high, there exist four regions as below,

1) When $V_{eff} \leq V_{dc} - A_{min}$, the oscillating waveform is a sinusoid with the minimum amplitude A_{min} and minimum frequency ω_{min};
2) When $V_{eff} \geq V_{dc} + A_{max}$, a sinusoid with the maximum amplitude A_{max} and maximum frequency ω_{max};
3) When $V_{dc} - A_{min} \leq V_{eff} \leq V_{dc}$, two partial sinusoids join at ECV. One is over V_{eff} with the amplitude A_{min} and frequency ω_{min}; the other is below V_{eff} with the amplitude $\theta_1 A_{max}$ (θ_1 is an *ellipse similar factor, ESF*) and frequency ω_{max}.
4) When $V_{dc} \leq V_{eff} \leq V_{dc} + A_{max}$, it consists of two segmental sinusoids joined at ECV. One is above V_{eff} with the amplitude $\theta_2 A_{min}$ (θ_2 is another ESF) and frequency ω_{min}; the other is below V_{eff} with the amplitude A_{max} and frequency ω_{max}.

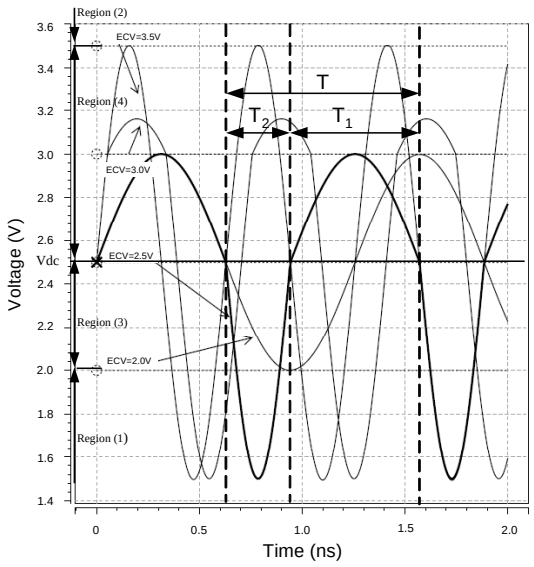

Fig. 4. Voltage waveforms of a varactor at different ECV

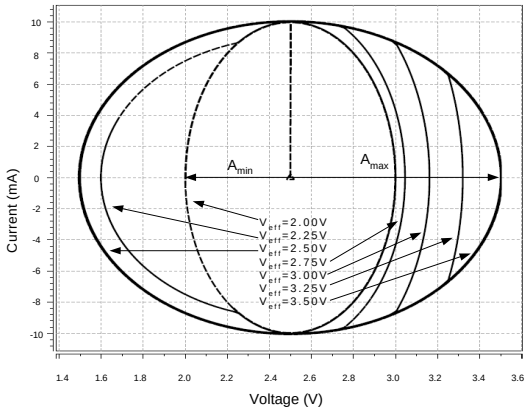

Fig. 5. I-V locus of a varactor

The I-V locus of a step-like varactor in the serial LC-tank circuit is shown in Fig. 5. It is consists of two ellipses of different size joined at the ECV. The above four regions satisfy the following ellipses' equations:

1) When $V_{eff} \leq V_{dc} - A_{min}$, the I-V locus holds

$$\left(\frac{V - V_{dc}}{A_{min}}\right)^2 + \left(\frac{I}{\omega_{min} C_{max} A_{min}}\right)^2 = 1; \quad (3)$$

2) When $V_{eff} \geq V_{dc} + A_{max}$, it holds

$$\left(\frac{V - V_{dc}}{A_{max}}\right)^2 + \left(\frac{I}{\omega_{max} C_{min} A_{max}}\right)^2 = 1; \quad (4)$$

3) When $V_{dc} - A_{min} \leq V_{eff} \leq V_{dc}$, two segmental sinusoids respectively hold

$$\left(\frac{V - V_{dc}}{A_{min}}\right)^2 + \left(\frac{I}{\omega_{min} C_{max} A_{min}}\right)^2 = 1, \quad \text{for } V \geq V_{eff},$$

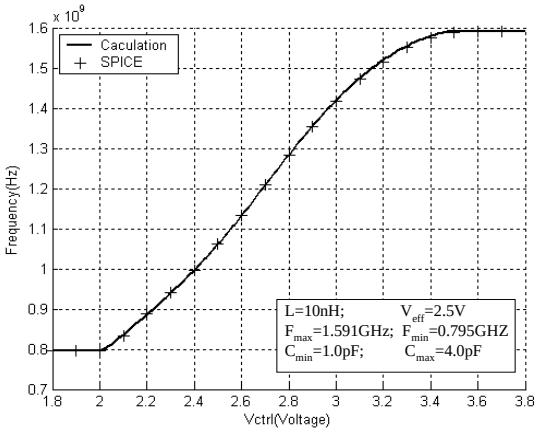

Fig. 6. Oscillator's tuning curve: simulated in SPICE, and calculated by (12) and (14)

$$\left(\frac{V-V_{dc}}{A_{max}}\right)^2+\left(\frac{I}{\omega_{max}C_{min}A_{max}}\right)^2=\theta_1^2,\quad \text{for}\, V\le V_{eff}, \quad (5)$$

where the ESF θ_1 satisfies $A_{min}/A_{max}\le\theta_1\le 1$. Especially when $V_{eff}=V_{dc}$ and $\theta_1=1$, it satisfies

$$I_{max}=\omega_{min}C_{max}A_{min}=\omega_{max}C_{min}A_{max} \quad (6)$$

where I_{max} is the maximum current in the inductor or varactor.

4) When $V_{dc}\le V_{eff}\le V_{dc}+A_{max}$, two segmental sinusoids respectively hold

$$\left(\frac{V-V_{dc}}{A_{min}}\right)^2+\left(\frac{I}{\omega_{min}C_{max}A_{min}}\right)^2=\theta_2^2,\quad \text{for}\ V\ge V_{eff},$$

$$\left(\frac{V-V_{dc}}{A_{max}}\right)^2+\left(\frac{I}{\omega_{max}C_{min}A_{max}}\right)^2=1,\quad \text{for}\ V\le V_{eff}, \quad (7)$$

where the ESF θ_2 satisfies $1\le\theta_2\le A_{max}/A_{min}$.

The oscillating periods in the above four regions can be calculated mathematically.

1) When $V_{eff}\le V_{dc}-A_{min}$, the oscillating period is

$$T=T_{max}=2\pi\sqrt{LC_{max}} \quad (8)$$

2) When $V_{eff}\ge V_{dc}+A_{max}$, the oscillating period is

$$T=T_{min}=2\pi\sqrt{LC_{min}} \quad (9)$$

3) When $V_{dc}-A_{min}\le V_{eff}\le V_{dc}$, the oscillating period is a sum of two intervals, $T=T_1+T_2$, shown in Fig. 4. T_1 is the time on the first ellipse; T_2 is the time on the second ellipse. At the ECV, the voltage and current of the varactor are V_{eff} and I_{eff}. From (6) (8) and (9), we obtain the amplitude ratio

$$\frac{A_{max}}{A_{min}}=\sqrt{\frac{C_{max}}{C_{min}}} \quad (10)$$

Substituting (10) in (5) leads to the ESF θ_1

$$\theta_1=\sqrt{1-\left(\frac{V_{eff}-V_{dc}}{A_{min}}\right)^2+\left(\frac{V_{eff}-V_{dc}}{A_{max}}\right)^2} \quad (11)$$

Thus, the oscillating period is,

$$T=T_1+T_2=\frac{\frac{\pi}{2}+asin\left(\frac{|V_{eff}-V_{dc}|}{A_{min}}\right)}{\pi}T_{max}+\frac{\frac{\pi}{2}-asin\left(\frac{|V_{eff}-V_{dc}|}{\theta_1 A_{max}}\right)}{\pi}T_{min}$$

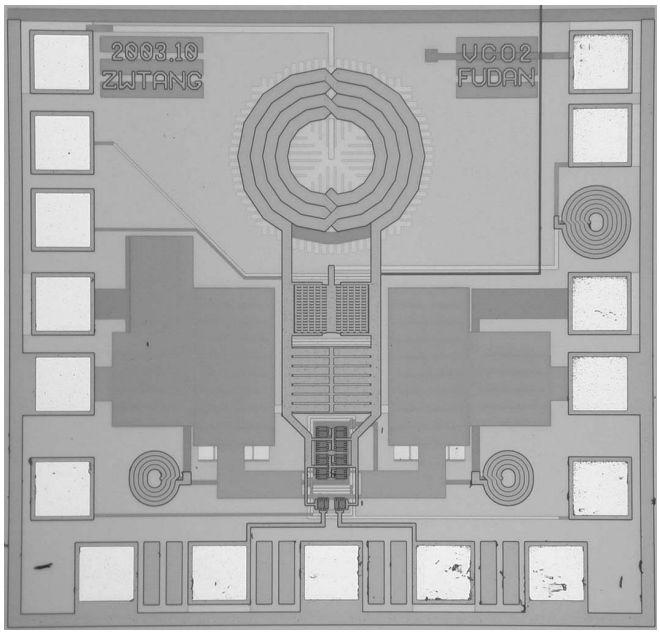

Fig. 7. Microphotograph of CMOS LC VCO

$$=\frac{1}{2}(T_{max}+T_{min})+\frac{1}{\pi}\left(asin\left(\frac{|V_{eff}-V_{dc}|}{A_{min}}\right)T_{max}-asin\left(\frac{|V_{eff}-V_{dc}|}{\theta_1 A_{max}}\right)T_{min}\right) \quad (12)$$

4) When $V_{dc}\le V_{eff}\le V_{dc}+A_{max}$, The same as Case 3). Solving (7), we can obtain the ESF and oscillating period,

$$\theta_2=\sqrt{1-\left(\frac{V_{eff}-V_{dc}}{A_{max}}\right)^2+\left(\frac{V_{eff}-V_{dc}}{A_{min}}\right)^2} \quad (13)$$

$$T=\frac{1}{2}(T_{max}+T_{min})+\frac{1}{\pi}\left(-asin\left(\frac{V_{eff}-V_{dc}}{\theta_2 A_{min}}\right)T_{max}+asin\left(\frac{V_{eff}-V_{dc}}{A_{max}}\right)T_{min}\right) \quad (14)$$

To validate the above method of oscillating period calculation, an ideal LC tank in Fig. 3(a) is simulated in HSPICE. Its parameters are L=10nH, C_{max}=4pF, C_{min}=1pF, and A_{min}=0.5V. In Fig. 6, the cross line is the simulation result in HSPICE, and the solid line is the calculation result from (12) and (14). The simulation agrees well with the calculation.

As the oscillator has a very large signal swing (nearly full power supply), the oscillating period is interpolated between T_{max} and T_{min}. The resulting frequency-voltage (F-V) curve, which is shown in Fig. 6., varies linearly with ECV in a range defined by the oscillation amplitude. Although the capacitance-voltage (C-V) characteristic of MOS varactors is step-like, the F-V curve is well linear. Contrary to widely held beliefs in [8], the linear C-V relationship of MOS varactors is no need.

IV. EXPERIMENT VALIDATION

Fig. 7 shows the microphotograph of LC VCO in Fig.1. At a 3.3-V supply, the tail current of LC-VCO is 3.1mA, and the centre frequency is 1.08GHz. The oscillator's tuning curve in Fig. 8 is obtained by the measurement of the fundamental frequency at different control voltages. On-chip differential spiral inductor is 12.38nH, so the single-end inductor features 6.19nH. The maximum and minimum capacitances in LC-VCO are 4.30pF (C_{max}) and 3.180pF (C_{min}). The

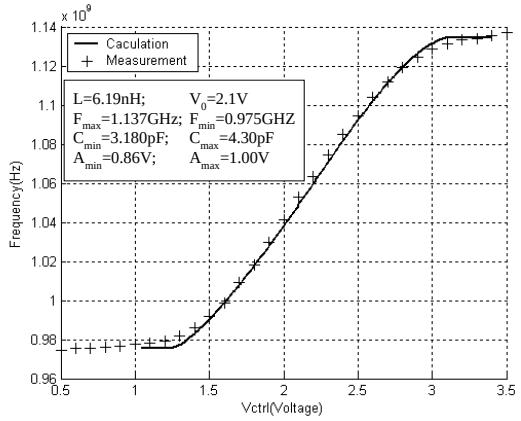

Fig. 8. F-V tuning curve of the measurement and calculation

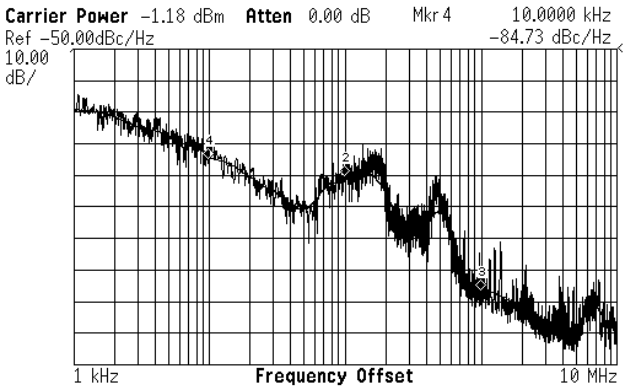

Fig. 9. Phase noise

maximum and minimum frequencies are 1.137GHz and 0.975GHz respectively. And the DC voltage is 2.1V, the minimum amplitude is 0.86V, the maximum amplitude is 1.0V calculated by (10). In Fig. 8, the cross lines are the results of measurement, and the solid lines are calculated by (12) and (14). The measurement agrees well with the results obtained from the theoretical oscillator tuning curves' equation (12) and (14), over the entire tuning range.

COB packaged chips are measured on a Agilent E4440A (3Hz~26.5GHz) PSA Series Spectrum Analyzer with Phase Noise Module. Fig. 9 shows a typical phase noise at 1.7V control voltage. The phase noise measured at different ECV voltages, is shown in Fig. 10. The worst phase noise is -82.2 dBc/Hz at a 10kHz frequency offset.

V. CONCLUSIONS

An accurate 1.08-GHz CMOS LC-tank voltage-controlled oscillator is implemented in a 0.35μm standard 2P4M CMOS process. A new convenient method of calculation of frequency tuning curves is proposed. The calculated F-V curves agree perfectly with the experiment. At 3.3V, the phase noise of the LC-VCO is measured to be -82.2 dBc/Hz at a 10kHz frequency offset. The tail current is 3.1mA.

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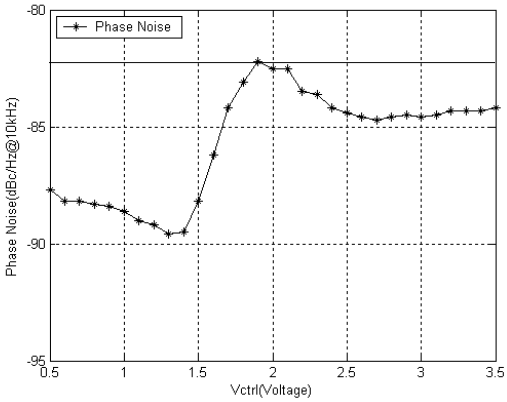

Fig. 10. Phase noise at 10kHz frequency offset

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