20.7 A 50-to-930MHz Quadrature-Output Fractional-N Frequency Synthesizer with 770-to-1860MHz Single-Inductor LC-VCO and Without Noise Folding Effect for Multistandard DTV Tuners

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There are many Digital TV (DTV) standards around the world, such as DVB-T/C/H in Europe, ATSC-C/M/H in North America, TDMB in China, ISDB-T in Japan and DMB-T in South Korea. In recent years, next generations of DVB standards (e.g. DVB-T2 and DVB-C2) are proposed, which adopt 256 QAM and even 4k QAM modulation to obtain higher performance. Often the DTV tuners employ a direct-conversion Zero-IF architecture, which demands the use of a wideband fractional-*N* synthesizer as the local oscillator (LO) to cover the frequency range of 50 to 900MHz. This LO needs to meet a very stringent phase noise requirement with an adequate target phase noise of –98dBc/Hz at a 10kHz offset and integrated rms phase error less than 0.25° [1]. However, it is well known that the performance of fractional-*N* PLLs is significantly influenced by the circuit nonlinearity. Nonlinearity results in the noise-folding phenomenon, which can seriously degrade the in-band phase noise and raise reference and fractional spurs [2].

This paper presents a wideband quadrature-output fractional-*N* synthesizer, which adopts only one single-inductor *LC*-VCO core with a frequency tuning range of 82.9%. A phase-frequency detector and charge pump (PFD/CP) linearization technique is proposed to completely eliminate the noise folding effect without raising the PLL reference spurs, which is achieved within the PFD circuit, rather than in the CP.

In the PFD/CP circuits, nonlinearity is mainly caused by the inevitable matching errors between the up and down currents. Adding a dc offset current to the CP avoids the nonlinearity by shifting operation to a linear region. However, this increases the phase noise contribution from the PFD and CP and results in a strong reference spur. A sampled loop filter technique reduces the reference spurs, but brings the problems of clock feedthrough and charge injection [2]. Figure 20.7.1 shows the modified PFD circuit and the corresponding timing diagram. This proposed PFD consists of only one more MUX, one more delay cell and one more DFF than a conventional one. When the control signal *mod* is high, a delayed reference clock f_{dref} is used to trigger resetting all DFFs. The rising edge of signal *up* and falling edge of signal *dn* are synchronized by the rising edge of f_{dref}, rather than the lagging one of rising edges of f_{ref} and f_{div} in the conventional PFD. Hence, the PFD/CP operation region is shifted to a linear part of the transfer curve, in which only PMOS transistors in CP adjust the turn-on time. Therefore, without the requirement of matching between NMOS and PMOS transistors, the PFD/CP transfer characteristic is perfectly linear, and static phase offset does not exist between f_{ref} and f_{div} when PLL is locked. Since nonlinearity no longer exists in the proposed PFD/CP, a fractional-*N* synthesizer without noise folding effect is realized, which has much smaller reference spurs and much lower in-band phase noise. In addition, two issues should be considered. Firstly, to avoid the error function when f_{div} lags far behind f_{ref} during PLL settling time, the proposed PFD is in the conventional mode (i.e. the control signal *mod* is low). After the PLL is locked, the proposed PFD works in the linearization mode (i.e. *mod* is high). Secondly, the delay time t_d must larger than the maximum phase offset between f_{ref} and f_{div}. The suitable value of t_d can be obtained from the results of statistics and Monte Carlo simulations.

Figure 20.7.2 shows the block diagram of the wideband fractional-*N* synthesizer and divider chain with frequency division by a factor of two or its power, such as 2, 4, 8 and 16, to extend the frequency coverage below the range of the core PLL. To meet the frequency range of 50 to 900MHz for DTV applications, an *LC*-VCO core with a frequency tuning range of 800 to 1800MHz is required, which must satisfy that the ratio between the maximum frequency f_{vcomax} and the minimum frequency f_{vcomin} must be larger than 2. Otherwise, an *LC*-VCO core with much higher frequency and a divide-by-3 divider must be designed [3]. For synthesizer use of such a wideband *LC*-VCO with multiple bands, an automatic frequency control (AFC) technique is used to select the sub-band of the *LC*-VCO whose center frequency is closest to the target frequency, automatically [4].

Figure 20.7.3 shows the detailed schematic of the wideband *LC*-VCO core with single on-chip inductor. The on-chip differential inductor employs a two-path configuration in the top Thick Metal to improve the Quality (*Q*) and to decrease the parasitic capacitance. All of the capacitors and varactors are realized with inversion MOS (I-MOS) transistors. In order to broaden the frequency range of the *LC*-VCO core, a native inversion NMOS transistor M0 with the C_{max}/C_{min} ratio larger than ten is adopted in the capacitor array. The wideband *LC*-VCO has a low tuning gain (K_{VCO}) by dividing the tuning range into 256 sub-bands. To maintain both K_{VCO} and band steps between center frequencies of two adjacent sub-bands, switched capacitors and switched varactors are both adjusted simultaneously with different unit values, where α_1~α_{255} and β_1~β_{255} are programmed coefficients and thermometer coding is used. The purpose of the level shift is to cancel the threshold offset in the varactors, which makes the maximal K_{VCO} of each band fall in the middle of the differential control voltages.

The wideband fractional-*N* synthesizer has been fabricated in a 0.18µm CMOS process with a total power consumption of 36mW from a 1.8V supply. The die area is 0.8mm^2, including LPF and excluding PADs. Figure 20.7.4 shows the measured 3dB closed-loop bandwidth, integrated rms phase error, and I/Q imbalance performances. The measured 3dB closed-loop bandwidth is about 98kHz. The integrated rms phase error from 100Hz to 40MHz is below 0.5° across the whole tuning range of the *LC*-VCO, and is below 250m°, 150m°, 75m° and 50m° in the divided-by-2, 4, 8 and 16 frequency ranges, respectively. The I/Q imbalance performance is indirectly measured by an image rejection ratio (IRR) in the immediate frequency (IF) output of a quadrature downconversion mixer. The measured IRR is over 45dBc in the divided-by-2 frequency range, and is over 50dBc in the divided-by-4, 8 and 16 frequency ranges without any calibration.

Figure 20.7.5 shows the typical measured phase noise in fractional-*N* mode. The phase noise of the PLL is –109dBc/Hz at 10kHz offset and –119dBc/Hz at 1MHz offset. The spot phase noise almost decreases 6dB per divided-by-2. When the conventional PFD works, the in-band phase noise is deteriorated 10dB due to the noise folding effect. Figure 20.7.6 shows that the worst reference spur is below 75dBc when using the proposed PFD and the worst IRR is 45dBc. The die micrograph and performance summary are shown in Fig. 20.7.7. It is to be noted that the state-of-the-art circuit employs a PLL that uses only one single-inductor *LC*-VCO with an f_{vcomax}/f_{vcomin} ratio much larger than 2.

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[4] Lei Lu, Zhichao Gong, Youchun Liao, Hao Min, and Zhangwen Tang, "A 975-to-1960MHz Fast-Locking Fractional-*N* Synthesizer with Adaptive Bandwidth Control and 4/4.5 Prescaler for Digital TV Tuners," *ISSCC Dig. Tech. Papers*, pp. 396-397, Feb. 2009.

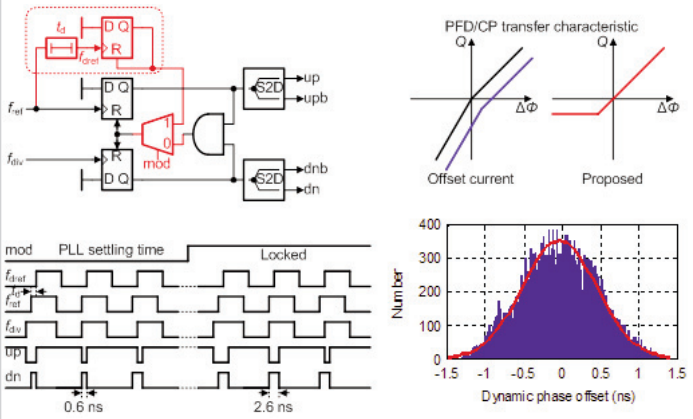

Figure 20.7.1: Proposed PFD circuit, corresponding timing diagram, PFD/CP transfer characteristic, and dynamic phase offset distribution between f_{ref} and f_{div} in PLL fractional mode.

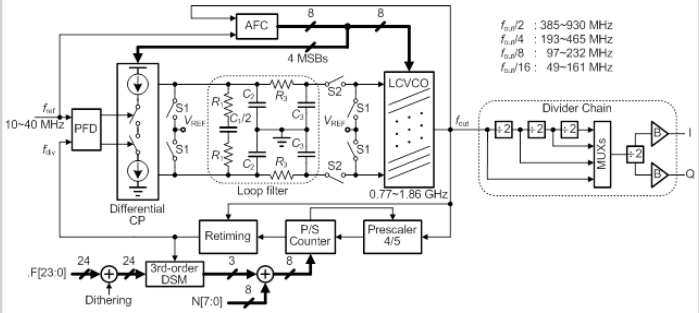

Figure 20.7.2: Block diagram of the fully-integrated quadrature-output fractional-*N* synthesizer.

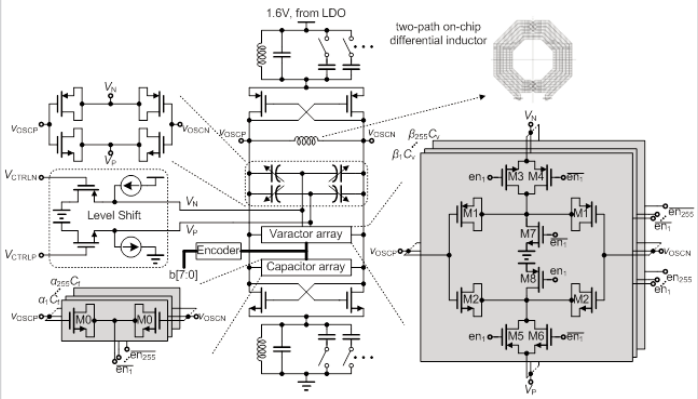

Figure 20.7.3: Detailed schematic of wideband *LC*-VCO core with a two-path differential inductor.

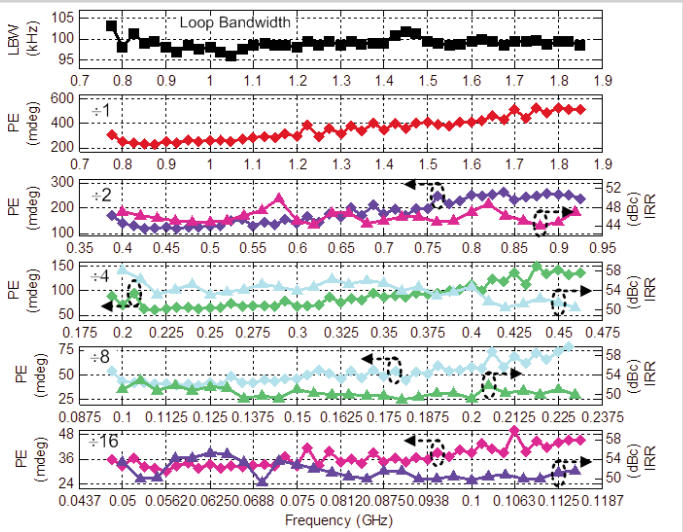

Figure 20.7.4: Measured 3dB closed-loop bandwidth, integrated rms phase error, and I/Q imbalance (IRR) across the whole output range.

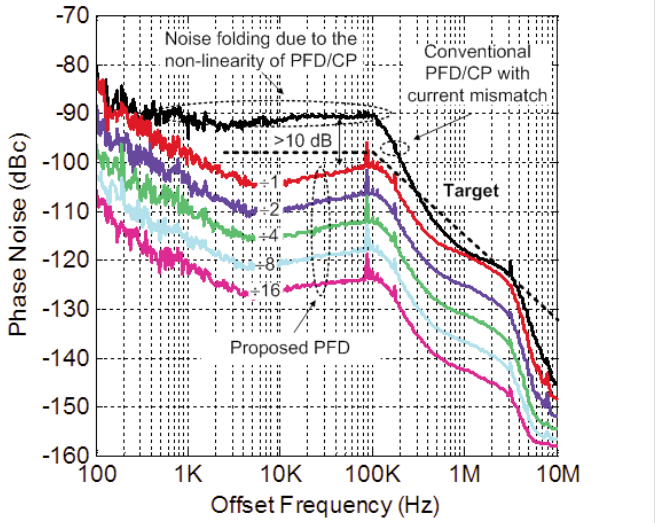

Figure 20.7.5: Measured phase noise of PLL with conventional PFD and with proposed PFD, and of output divided by 2, 4, 8 and 16.

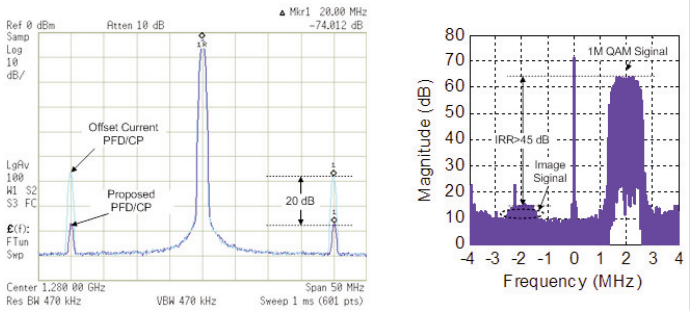

Figure 20.7.6: Measured reference spurs and I/Q imbalance (IRR).

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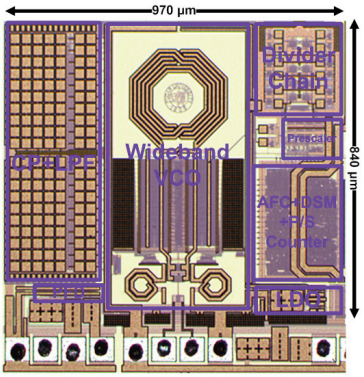

Technology	0.18-μm CMOS	Ref. Frequency	10~40 MHz	
Die Area	0.97 mm × 0.84 mm	Output Frequency	0.77~1.86 GHz (82.9%)	
Supply Voltage	1.8 V	Phase Noise (dBc/Hz)	–102@10 kHz (in-band)	
Current	20 mA		–119@1 MHz	
Bandwidth	95~105 kHz	Phase Error (rms)	0.3°~0.5° (100 Hz~40 MHz)	
Reference Spur	>74 dBc	Locking Time	30 μs (14 μs for AFC)	
Divided by	2	4	8	16
Phase Noise (dBc/Hz)	–108@10 kHz	–114@10 kHz	–120@10 kHz	–126@10 kHz
	–125@1 MHz	–131@1 MHz	–137@1 MHz	–143@1 MHz
Phase Error	<250 mdeg	<150 mdeg	<75 mdeg	<50 mdeg
I/Q Imbalance	IRR>45 dBc	IRR>50 dBc	IRR>50 dBc	IRR>50 dBc

Figure 20.7.7: Die micrograph and performance summary.

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