23.4 A 975-to-1960MHz Fast-Locking Fractional-*N* Synthesizer with Adaptive Bandwidth Control and 4/4.5 Prescaler for Digital TV Tuners

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There is a high demand for high-performance tuners to meet the digital video broadcasting-terrestrial (DVB-T) standard. Often the DVB-T tuners employ a double-conversion zero-IF (DZIF) architecture that demands a wideband fractional-*N* synthesizer as the first local oscillator (LO_1) to cover the frequency range of 975 to 1960MHz. This LO_1 needs to meet a stringent phase-noise requirement with an adequate target phase noise of –87dBc/Hz at a 10kHz offset and integrated rms phase error less than 1° [1]. Because of the very wide frequency range, the variation of loop bandwidth may affect the phase-noise performance and loop stability.

This paper presents a wideband fractional-*N* synthesizer whose loop bandwidth is controlled adaptively. A fast automatic frequency-control (AFC) technique which selects the subband of the VCO is proposed to reduce the residual fractional error to 1/16 of the reference frequency f_{ref}. A new 4/4.5 prescaler is adopted to lower the quantization noise by reducing the quantization step size to 0.5.

Figure 23.4.1 shows the block diagram of the wideband fractional-*N* synthesizer and a simplified *LC*-tank of the wideband VCO. Charge pump (CP) and VCO are both differentially configured to suppress common-mode noise from control lines, substrate and power supply. The loop filter (LPF) is fully integrated in differential mode to save the die area. The loop bandwidth of the fourth-order synthesizer can be expressed as

$$\text{Loop bandwidth} = \frac{I_{cp}K_{vco}f_{ref}}{2\pi f_{vco}}\frac{R_1C_1}{C_1+C_2+C_3} \quad (1)$$

where I_{cp} is the CP current, K_{vco} is the VCO tuning gain, f_{vco} is the output frequency, R_1, C_1, C_2, and C_3 are parameters of LPF. Two factors affect the loop bandwidth. Firstly, the VCO gain K_{vco} may change greatly in the conventional *LC*-tank which employs binary-weighted switched capacitors and unchanged varactors. In this design, the wideband VCO has a low tuning gain by dividing the tuning range into 256 subbands. To maintain both K_{vco} and band steps between center frequencies of two adjacent subbands, switched capacitors and switched varactors are both adjusted simultaneously with different values of units, where α_1 to α_{255} and β_1 to β_{255} are programmed coefficients and thermometer coding is used here [2]. Secondly, 4 MSBs of the AFC output are used to set the CP current I_{cp} adaptively, thus making I_{cp} match the selected subband of VCO and proportional to the output frequency f_{vco}. Therefore, without changing LPF parameters, the loop bandwidth is adaptively controlled by maintaining K_{vco} and making I_{cp} match f_{vco} across the whole wide frequency range.

To control the wideband multi-band VCO, the AFC technique is used to select the subband of VCO whose center frequency is closest to the target frequency automatically. Conventional AFC compares feedback signal f_{div} with reference signal f_{ref}, and shifts the subband of VCO according to the binary-search algorithm [3]. However, AFC operates when the PLL is open, then f_{div} only comes from the signal divided by the integer modulus *N* of the division ratio *N.F*, which ignores the fractional modulus *.F*, thereby causing the residual fractional error to amount to as high as $1\cdot f_{ref}$. Figure 23.4.2 shows the proposed division-ratio-based AFC that can reduce the fractional error effectively. During the period T_{cntr}, the VCO clock f_{vco} is counted to N_{cntr}. At the same time, the target frequency relates with N_{dec}, and N_{dec} is obtained from the product of *p* multiples of $N.F_{dec}$, which includes the integer modulus and 4 MSBs of fractional modulus of the desired division ratio *N.F*. Then the subband of VCO is shifted up or down according to the value of the difference ε between N_{cntr} and N_{dec}. The frequency counting error is $1/T_{cntr}$, so the unit comparison time T_{cntr} should be long enough to reduce the frequency counting error. In addition, the decoded modulus N_{dec} should be an integer, hence *p* can be selected as an integer power of two, where *p*=16 is chosen in this design. The remaining undecoding modulus induces the residual fractional error, which results in a maximum of $2^{-4}\cdot f_{ref}$. Due to the high-speed property for counting VCO clock directly, cascaded asynchronous divide-by-2 counters with a multiplexer is used. The multiplexer outputs f_{vco} during T_{cntr} when *hold* is low, and N_{cntr} is read after the last counter finishes. To save the power, the first three counters are realized in TSPC logic and remaining counters employ digital circuits.

Figure 23.4.3 shows the schematic of the feedback divider which includes a new 4/4.5 prescaler and a double-edge-triggered retiming circuit. This prescaler consists of 4 DFFs, 2 MUXs and 2 D-latchs, and the remaining 4 AND gates can be embedded into the DFF and the D-latch to increase the maximal working frequency. DFF1 and DFF2 are triggered at the falling edge and DFF3 and DFF4 are triggered at the rising edge. The multiplexer MUX5 chooses *Q*2 or *Q*4 to output every half clock period in turn. Two latches (Dlatch6 and Dlatch7) and one multiplexer (MUX8) form a double-edge-triggered flip-flop (DTFF) [4]. When the control signal *mod* is high, the DTFF is enabled, and the prescaler works in divide-by-4.5 mode. *Q*8 lags half a period behind *Q*5 and DFF1-4 and MUX5 swallow half extra period of input signal f_{vco} due to the delay of *Q*8. To match the double-edge-triggered property of the prescaler and eliminate the accumulated jitter in the feedback divider, another DTFF is used to retime the feedback signal triggered by the high-speed VCO clock. The power spectral density (PSD) of PLL phase noise contributed by the DSM is proportional to the PSD of quantization noise, which is determined by the quantization step. By using the 4/4.5 prescaler, the quantization step size is reduced to 0.5, so a 6dB improvement of phase noise contributed from the DSM can be achieved.

The wideband fractional-*N* synthesizer is fabricated in a 0.18µm CMOS process with a total power consumption of 25mW from a 1.8V supply. The die area is 1.58mm^2, including LPF and PADs. Figure 23.4.4 shows the measured 3dB closed-loop bandwidth and integrated rms phase error from 100Hz to 40MHz across the 1GHz tuning range. When adaptive I_{cp} control is enabled, the closed-loop has an average 3dB bandwidth of 92.5kHz with the variation less than 10.3%. While adaptive I_{cp} control is disabled, the bandwidth variation is about 70.4%. In calibration-enable mode, the rms phase error is from 0.6° to 1.05°.

Figure 23.4.5 shows the typical measured phase noise in fractional-*N* mode. The phase noise is –95dBc/Hz at a 3kHz offset and –126.5dBc/Hz at a 1MHz offset. Figure 23.4.6 shows that the synthesizer has a total locking time of 20µs with only 6.4µs for AFC, while the conventional AFC counting the signal divided by 8 from VCO consumes 42.4µs. The die micrograph and performance summary are shown in Figure 23.4.7.

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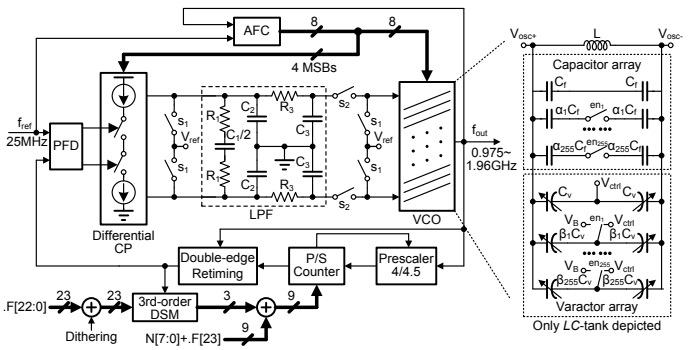


Figure 23.4.1: Block diagram of the fully integrated fractional-*N* synthesizer and simplified *LC*-tank of the wideband VCO. Switched capacitors and varactors are adjusted to maintain VCO gain and band steps simultaneously.

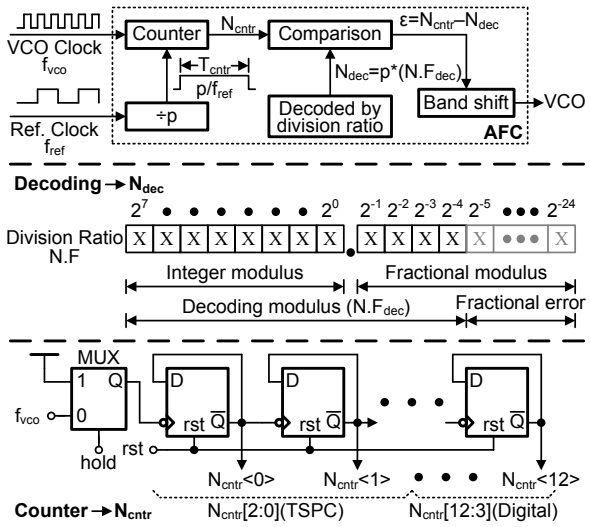


Figure 23.4.2: Block diagram and principle of the presented division-ratio-based fast AFC technique.

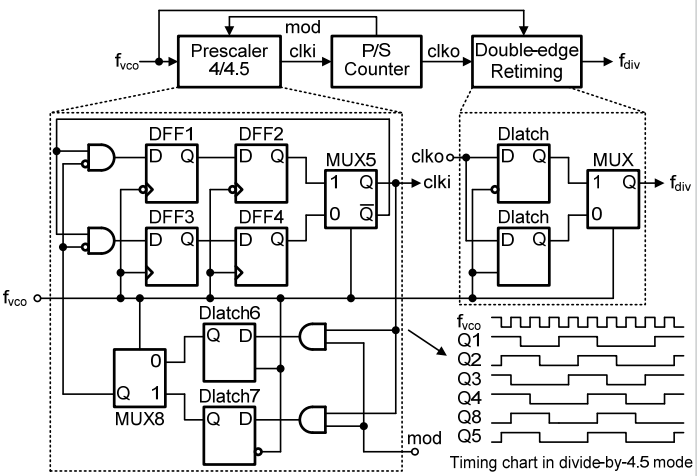


Figure 23.4.3: Schematic of the 4/4.5 prescaler and double-edge-triggered retiming circuit.

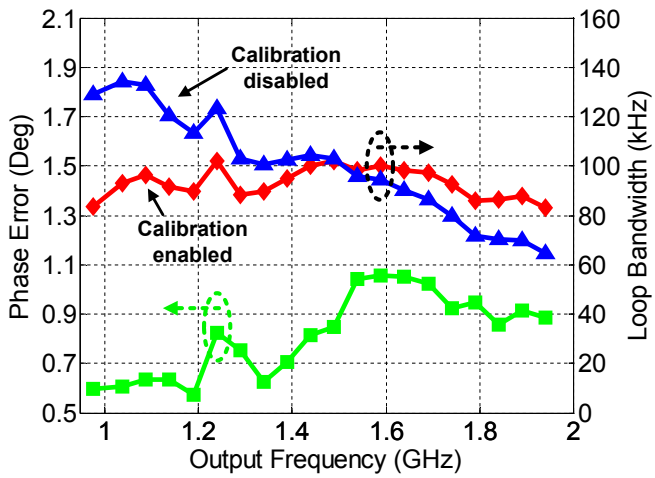


Figure 23.4.4: Measured integrated rms phase error and 3dB closed-loop bandwidth across the entire output range. Disabled calibration is to fix the I_{cp} at the value with output frequency of 1.5GHz in enabled calibration mode.

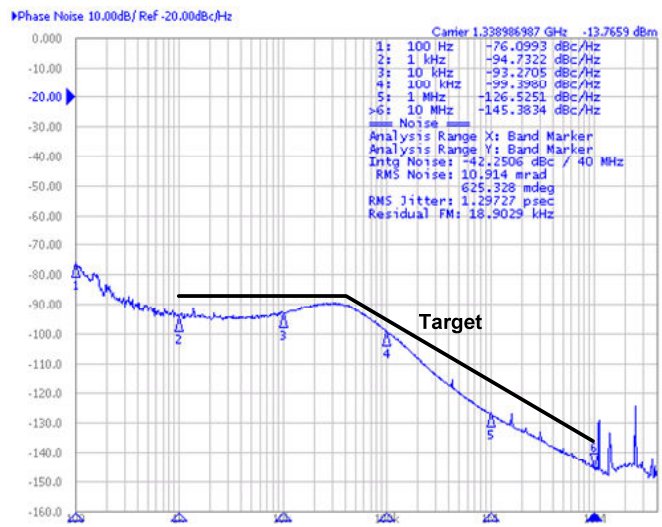


Figure 23.4.5: Measured phase noise with the division ratio of 53.56.

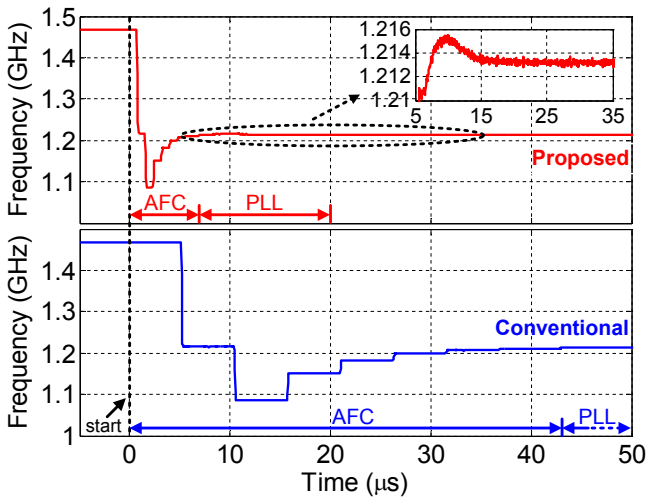
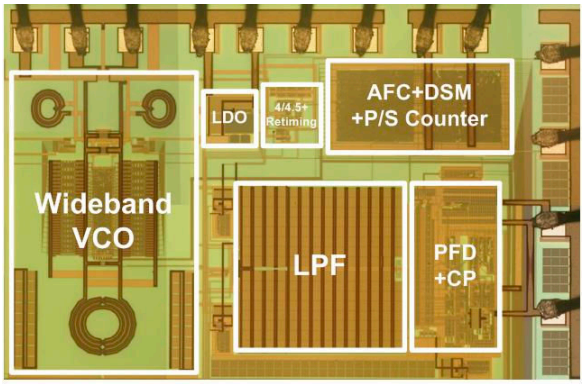


Figure 23.4.6: Comparison of the measured total locking time, including AFC and PLL phases, between the presented and conventional architectures.



Technology	0.18μm CMOS	Ref. Frequency	25 MHz
Die Area	1.58 mm × 1 mm	Output Frequency	0.975 to 1.96 GHz (67.1%)
Supply Voltage	1.8 V	Phase Noise (dBc/Hz)	-91@3 kHz (in-band)
Current	14 mA		-123@1 MHz
Bandwidth	83 to 102 kHz	Phase Error (rms)	0.6° to 1.05° (100Hz to 40MHz)
Freq. Resolution	<1.5 Hz	Locking Time	20 μs (6.4 μs for AFC)

Figure 23.4.7: Die micrograph and performance summary. Phase noise results represent the worst case of fractional-*N* performance.

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