A Fully Differential Charge Pump with Accurate Current Matching and Rail-to-Rail Common-Mode Feedback Circuit

Zhenyu Yang, Zhangwen Tang, and Hao Min
State Key Laboratory of ASIC & System, Fudan University
Shanghai, China
Email: zyyang@fudan.edu.cn

***Abstract*—A fully differential charge pump is proposed in this paper. It adopts the replica technique to eliminate the effect of channel-length modulation, and the charging and discharging currents can match well in a wide output range. A rail-to-rail common-mode feedback circuit is employed to ensure the large swing of the charge pump unrestricted. The charge pump is designed and fabricated in SMIC 0.18μm CMOS process. The measured reference spur-level is about -73dBc and the in-band phase noise is nearly -90dBc/Hz@1KHz. The power dissipation of the charge pump is only 1mW.**

I. INTRODUCTION

Frequency synthesizers have been widely used in modern RF communication systems. The typical frequency synthesizer includes PFD, Charge pump, Loop filter, VCO and Divider. Recently, the fully differential charge pump circuit has been widely used in order to improve the spur performance, but the differential current matching characteristic in conventional fully differential charge pumps[1~2] will be worse because of the effect of channel-length modulation. This paper presents a new fully differential charge pump circuit, which adopts the replica technique to improve the current matching characteristic, without reducing the output swing.

The contents of this paper are as follows. Section II analyses the drawbacks of conventional fully differential charge pumps. Section III describes the novel charge pump in detail. The microphotograph of the chip and the experimental results are all presented in section IV, followed by the conclusions in section V.

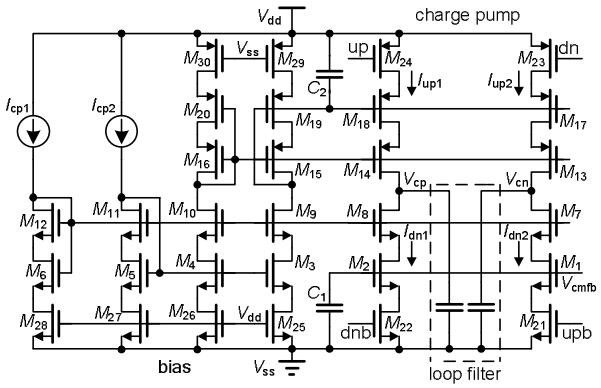

Fig.1 Conventional fully differential cascode charge pump circuit

II. CONVENTIONAL FULLY DIFFERENTIAL CHARGE PUMP

Compared with the single-end charge pump, the fully differential cascode charge pump[2] which is shown in Fig. 1 has larger output swing, better current matching characteristic and weaker effect of clock feedthrough.

M_1~M_{20} form the cascode current mirrors to increase the output impedance so that the current variation is less sensitive to the output voltage. M_{21}~M_{24} are source-switches for the charge pump, which can minimize the turn-on and turn-off time. M_{25}~M_{30} are used for replica biasing to give the same bias condition when the charge pump is turned on. Capacitors C_1 and C_2 are added to reduce the charge coupling to the gate. But, there are two drawbacks: (1) the cascode transistors M_7, M_8 and M_{13}, M_{14} limit the output swing of the charge pump, which is not appropriate for the low supply voltage application. (2) as $|V_{cp}-V_{cn}|$ becomes larger, the matching characteristic of differential charging and discharging currents will be worse.

To illustrate this, let us define the output voltages as follows:

$$V_{cp} = V_{cm} + \frac{V_{diff}}{2}\ ,\ V_{cp} = V_{cm} - \frac{V_{diff}}{2} \tag{1}$$

where V_{cm} is the desired common-mode voltage and V_{diff} is the differential-mode voltage. When the value of V_{diff} isn't equal to zero, the values of I_{up1}、I_{dn1}、I_{up2} and I_{dn2} will change due to the effect of channel-length modulation. We can assume for simplicity that:

$$\begin{aligned} I_{up1} &= I_{cm} - \Delta I\ ,\ I_{dn1} = I_{cm} + \Delta I \\ I_{up2} &= I_{cm} + \Delta I\ ,\ I_{dn2} = I_{cm} - \Delta I \end{aligned} \tag{2}$$

where $\Delta I > 0$ and I_{cm} is the current when the output voltage is equal to V_{cm}. So the mismatch of single-ended charging and discharging currents is:

$$I_{up1} - I_{dn1} = -2\Delta I\ ,\ I_{up2} - I_{dn2} = 2\Delta I \tag{3}$$

And the differential charging and discharging currents mismatch is:

$$\Delta = (I_{up1} - I_{dn1}) - (I_{up2} - I_{dn2}) = -4\Delta I \tag{4}$$

Comparing (3) and (4), the effect of channel-length modulation will reduce the matching characteristic of differential charging and discharging currents and increase the level of reference spurs.

III. PROPOSED CHARGE PUMP AND CMFB CIRCUIT

A. Proposed charge pump circuit

To overcome the two drawbacks analyzed above, a fully differential charge pump with replica method to achieve better mismatch suppression is designed in this paper. As shown in Fig. 2. The rail-to-rail opamp A1 and A2 presented in [3] have enough DC gain to ensure V_{cp} and V_{cn} to be equal. The structure of the opamp A1 (A2) is shown in Fig.3.

When "up" and "dn" are the logic low level, the switches are closed, then the currents in charge pump branches(I_{up1}, I_{up2}) and the currents in replica branches(I_{p1}, I_{p2}) will satisfy the relationship that:[4]

$$I_{up1} = I_{p1} \equiv I_{n1} \ , \ I_{up2} = I_{p2} \equiv I_{n2} \tag{5}$$

Assuming

$$V_p = V_{cp} = V_{cm} + \frac{V_{diff}}{2} \ , \ V_n = V_{cn} = V_{cm} - \frac{V_{diff}}{2} \tag{6}$$

When the value of V_{diff} isn't equal to zero, the values of I_{up1}, I_{dn1}, I_{up2}, I_{dn2} and the values of I_{p1}, I_{n1}, I_{p2}, I_{n2} will change due to the effect of channel-length modulation. the expressions are:

$$\begin{aligned} I_{up1} &= I_{p1} = I_{n1} = I_{replica} + \Delta I_{replica} \\ I_{dn1} &= I_{cm} + \Delta I \\ I_{up2} &= I_{p2} = I_{n2} = I_{replica} - \Delta I_{replica} \\ I_{dn2} &= I_{cm} - \Delta I \end{aligned} \tag{7}$$

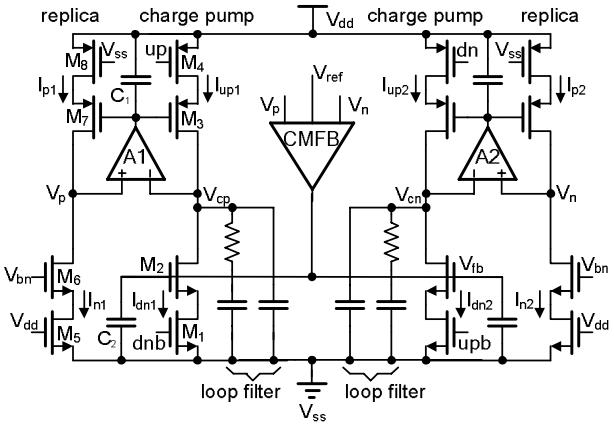

Fig.2 Proposed fully differential charge pump circuit

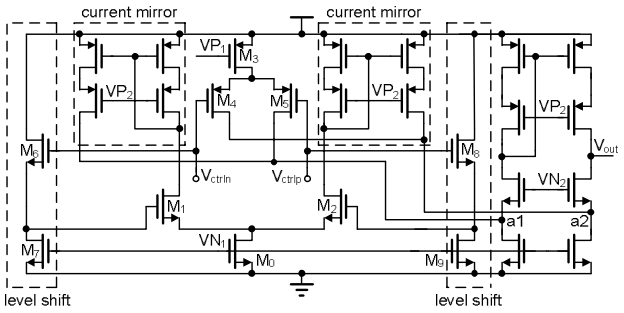

Fig.3 The opamp A1(A2) with rail-to-rail input range

Where $I_{replica}$ is the current when the output voltage is equal to V_{cm}. $\Delta I_{replica}$ is the current variations in replica branches. For simplicity, define the variations of I_{dn1} and I_{dn2} are both ΔI, and the variations of I_{n1} and I_{n2} are both $\Delta I_{replica}$, when the CMFB circuit is stable, we can induce that $V_{fb} \approx V_{bn}$. Therefore,

$$I_{n1} \approx I_{dn1} \ , \ I_{n2} \approx I_{dn2} \ , \ \Delta I_{replica} \approx \Delta I \tag{8}$$

So the differential charging and discharging currents mismatch will satisfy that

$$\begin{aligned} \Delta &= (I_{up1} - I_{dn1}) - (I_{up2} - I_{dn2}) \\ &= (I_{n1} - I_{dn1}) - (I_{n2} - I_{dn2}) \approx 0 \end{aligned} \tag{9}$$

The current variations of conventional and proposed fully differential charge pumps due to the effect of channel-length modulation are shown in Table I. Because the match between PMOS and NMOS current sources has been converted to the match between two NMOS current sources, the proposed charge pump can make the currents match better, and depress the reference spurs in frequency synthesizer.

Table I
Comparison of conventional and proposed charge pumps

$V_{cp}>V_{cn}$	I_{up1}	I_{up2}	I_{dn1}	I_{dn2}	$(I_{up1}-I_{dn1})-(I_{up2}-I_{dn2})$
conventional	-ΔI	ΔI	ΔI	-ΔI	-4ΔI
proposed	ΔI	-ΔI	ΔI	-ΔI	≈0

B. Rail-to-rail CMFB circuit

To ensure the large swing of the proposed charge pump unrestricted by CMFB circuit, a rail-to-rail input range CMFB circuit shown in Fig. 4 is presented in this paper. V_p and V_n can be chosen as the input sampling signals of CMFB circuit in order not to change the value of zeros and poles in the loop filter. The buffer amplifiers A3 and A4 copy V_p and V_n to V_{p1} and V_{n1}. The common-mode voltage V_{cm} could be got through the RC sampling network, then the voltage V_{fb}, which is the comparative result of V_{cm} and desired common-mode reference voltage V_{ref}, feeds back to the charge pump to tune the loop. Because the amplifiers A3 and A4 are rail-to-rail structure, the output swing of the charge pump won't be limited by CMFB circuit as [5]. Moreover, the noise from the CMFB circuit is common mode to the charge pump, so it has little impact on the phase noise of the frequency synthesizer.

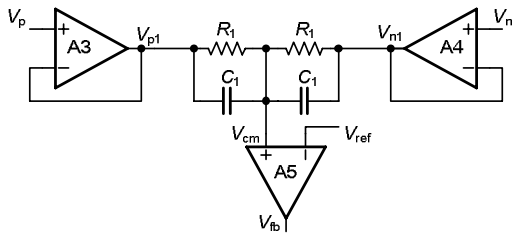

Fig.4 Rail-to-rail input range CMFB circuit

IV. EXPERIMENTAL RESULTS

The whole integer-N frequency synthesizer which includes the proposed fully differential charge pump circuit is shown in Fig. 5. A switched-capacitors bank LC tank voltage-controlled oscillator (VCO) with a fast adaptive frequency calibration (AFC)[6] is used in this design, and after the divide by two, a commonly used 4/5 prescaler, operating at the high frequency of VCO, is made as the source-coupled logic (ECL) type. The programmable counter is used as a conventional CMOS pulse swallow type.

All the circuits have been designed and fabricated in SMIC 0.18μm CMOS mixed-signal process. Fig.6 shows the microphotograph of the monolithic integer-N frequency synthesizer. The area of the charge pump is about 450μm×280μm, and the power dissipation is 1mW.

The spur and phase noise performance of the frequency synthesizer is tested by Agilent E4445A (3~26.5GHz) PSA Series Spectrum Analyzer. The division value of the divider can be changed in order to make $|V_{cp}-V_{cn}|$ largest. The waveforms of the control voltage V_{cp} and V_{cn} in locking state are shown in Fig.7, the locking time is smaller than 60μs, so the CMFB circuit shown in Fig.4 won't increase the response time of the PLL loop. The measured reference spur is shown in Fig.8. When V_{cp}≈1.25V and V_{cn}≈0.25V, the spur-level which is -73dBc should be in the worst case.

Furthermore, when the output frequency is 1.05GHz, the phase noise test result is shown in Fig.9. It can be seen that the in-band noise is nearly -90dBc/Hz@1KHz, and the RMS phase error (10Hz~10MHz) is about 1.8 degree.

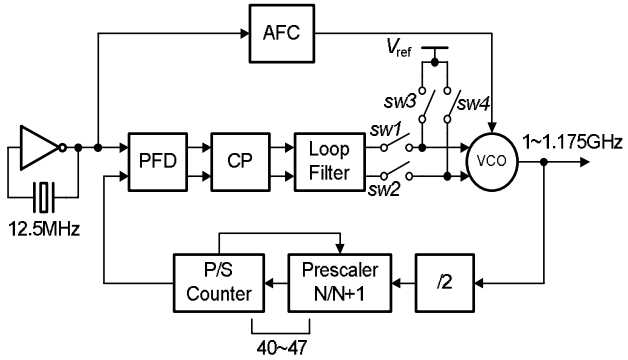

Fig.5 The block diagram of the frequency synthesizer

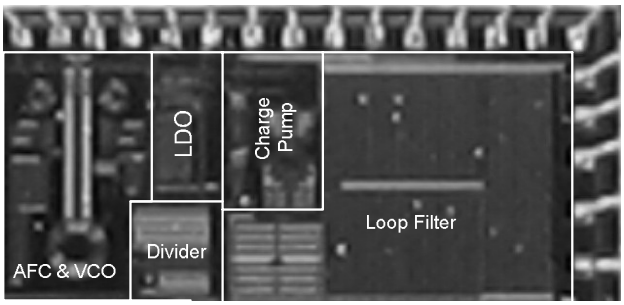

Fig.6 Microphotograph of the frequency synthesizer

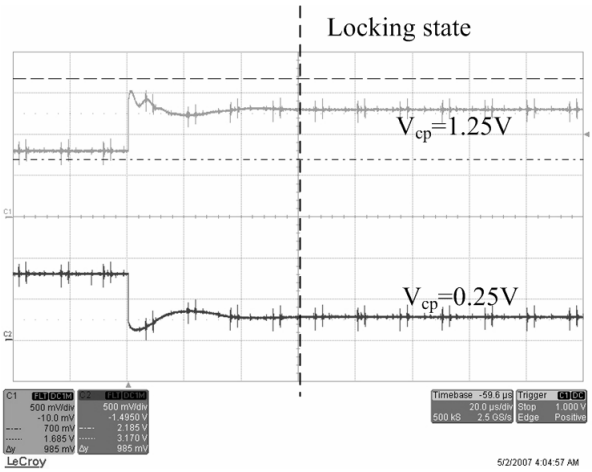

Fig.7 The waveforms of control voltages V_{cp} and V_{cn} in locking state

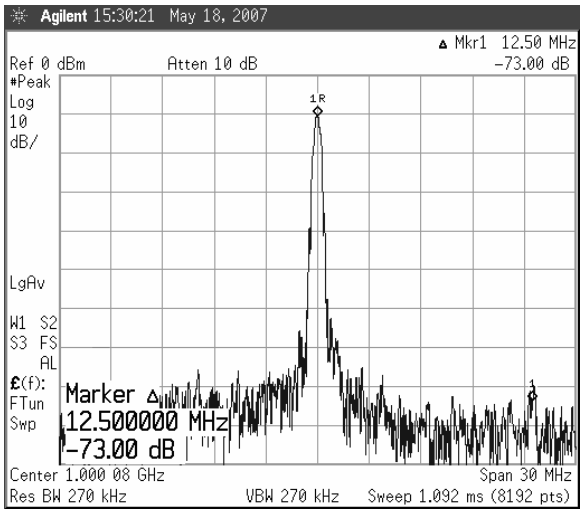

Fig.8 The measured reference spur-level when V_{cp}≈1.25V and V_{cn}≈0.25V

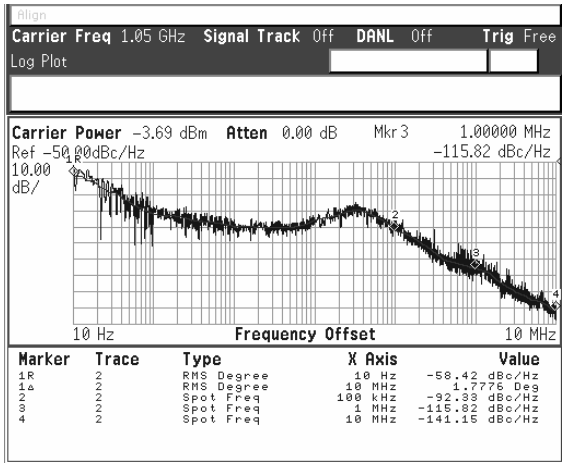

Fig.9 The measured phase noise of the integer-N frequency synthesizer at 1.05GHz

Table II gives the measurement results compared with recently published works, it can be seen that compared to those with a third-order loop filter, such as [7~8] and [9], this work performs a competitively low spur, and compared to those with a second-order loop filter such as [10] and [11], the proposed charge pump can make a great improvement in the spur performance. Also, the frequency synthesizer which adopts the proposed charge pump structure can achieve a good in-band phase noise performance.

V. CONCLUSIONS

In this paper, based on the analysis of the drawbacks of the conventional charge pump circuit which is used in integer-N frequency synthesizers, a fully differential charge pump with better suppression of output currents mismatch is proposed. The replica technique is adopted to eliminate the effect of channel-length modulation, and a rail-to-rail common-mode feedback circuit is introduced in order to ensure the large swing of the charge pump unrestricted. The experimental results show that the worst spur-level is about -73dBc, the in-band phase noise is nearly -90dBc/Hz@1KHz, and the locking time is smaller than 60μs. So the charge pump is suitable to be used in high-performance frequency synthesizers.

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Table II Comparison of measured reference spurs and phase noise

	Process	Reference Clock	Bandwidth	Spur-level	Loop filter	Phase noise (dBc/Hz)	Supply voltage
[7]	0.35μm	40(50)MHz	250KHz	-57dBc	3-order	-86@10KHz	2V
[8]	0.25μm	43MHz	80KHz	<-69dBc	3-order	-75@40KHz	1.5V
[9]	0.25μm	10MHz	25KHz	-70dBc	3-order	-63@10KHz	2.5V
[10]	0.25μm	4MHz	90KHz	-45dBc	2-order	-77@10KHz	2.5V
[11]	0.18μm	20MHz	60KHz	-74dBc	2-order	-79@10KHz	1.8V
This work	0.18μm	12.5MHz	60KHz	-73dBc	2-order	-90@1KHz	1.8V