Analysis of Self-resonant Frequency for Differential-driven Symmetric and Single-ended Inductors

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Abstract
In this paper, a distributed capacitance model (***DCM***) for monolithic inductors is developed to predict the equivalent parasitical capacitances of inductor. The ratio of the self-resonant frequency (f_{SR}) of the differentially driven symmetric inductor (f_{SR_diff}) to the f_{SR} of the single-ended driven inductor (f_{SR_se}) has been firstly predicted and explained. Compared with an equivalent single-ended configuration, experimental data demonstrate that the differential inductor offers a 127% greater maximum quality factor ($\boldsymbol{Q}_{max}$) and a broader range of operating frequencies. Design guidelines have been obtained from ***DCM***.

Key words: Distributed capacitance model (*DCM*), self-resonant frequency (f_{SR}) ratio, high quality factor (***Q***), on-chip inductor, optimum designs.

1. Introduction

Monolithic inductor is an important component in highly integrated radio frequency circuits (*RF IC*s) for wireless communication systems. But on-chip inductor has low ***Q*** due to metal ohmic loss and conductive silicon substrate loss. Many researchers found quite a few methods to improve ***Q*** of on-chip inductor [1]. A symmetric inductor that is driven differentially can realize a substantially greater factor without altering the fabrication process.

If an inductor is modeled as a simple parallel ***RLC*** tank, it can be shown that

$$Q_{ind} = 2\omega \frac{\left(E_m^{av} - E_e^{av}\right)}{P_l^{av}} \tag{1}$$

where E_m^{av}, E_e^{av}, P_l^{av} denote the average magnetic and electric energies stored and the average power dissipated in the inductor, respectively. $E_e^{av} \propto$ the total equivalent capacitance of the inductor (C_{eq}), therefore, the lower the C_{eq}, the higher Q and f_{SR} the inductor have. The f_{SR} can be defined as the frequency while ***Q*** drops to zero.

$$f_{SR} = \left(2\pi\sqrt{L_{eq}C_{eq}}\right)^{-1} \tag{2}$$

The ***DCM*** for monolithic spiral has been studied in recently years [2-4]. In this paper, DCMs of inductors are developed to accurately quantify the equivalent capacitive coupling capacitances (C_{m_m}) between the two terminals and the equivalent capacitance between the metal track and the substrate (C_{m_s}) of the symmetric inductors that are driven differentially and single-ended. Consequently the ratio of the f_{SR_diff} the f_{SR_se} has been firstly predicted and explained. Design guidelines have been obtained from ***DCM***.

2. Distributed capacitance model

Inductors that are driven differentially or single-ended (Seen Figure 1.) have different C_{eq}.

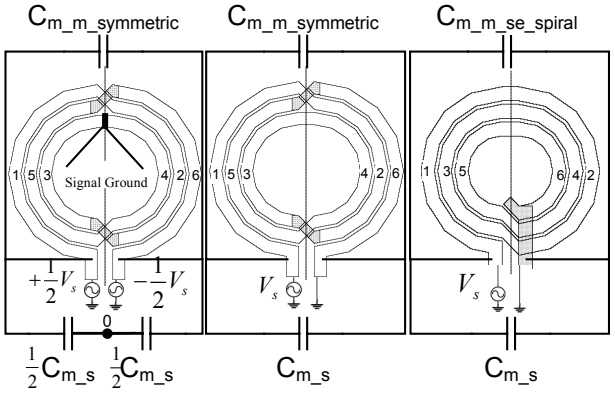


Figure 1. The planar on-chip inductors with the same track width, space, inner and outer radius: (a) Differentially driven symmetric configuration (***DSPI***); (b) Single-ended driven symmetric configuration (***SSPI***); (c) Single-ended spiral configuration (***SEPI***). (Note: 123456 are current flow direction in inductor, i.e. AC signal voltage profile or half turns serial number; Capacitances are the equivalent parasitical capacitance of the on-chip inductor.)

The electrical energy stored in the equivalent capacitor of the inductor can be divided into two parts: one is in

the metal-to-metal capacitor, i.e. E_{C,m_m} and the other is in the metal-to-substrate capacitor, i.e., E_{C,m_s} and it can be derived as

$$E_{C,total} = \frac{1}{2} C_{eq} V_s^2 = E_{C,m\_s} + E_{C,m\_m}$$
$$= \frac{1}{2} C_{m\_m} V_s^2 + \frac{1}{2} C_{m\_s} V_s^2 = \frac{1}{2} \cdot \left(C_{m\_m} + C_{m\_s} \right) \cdot V_s^2 \quad (3)$$

Therefore, the equivalent capacitor of the inductor can be expressed as

$$C_{eq} = C_{m\_m} + C_{m\_s} \quad (4)$$

2.1 Assumptions and definitions

To accurately quantify $\boldsymbol{C}_{\mathrm{m\_m}}$ and $\boldsymbol{C}_{\mathrm{m\_s}}$ in inductors, the proposed DCM can analytically calculate them rather than qualitatively approximate [2]. The fundamental assumptions of ***DCM*** can be derived from the voltage distribution over the inductor, which is called voltage profile in [3]. For the conveniences of calculation and analysis, the following assumptions are made.

1) The same layer metal traces of inductor have the same resistivity ρ, current, and metal track width ***w*** (at least in the same half turn), metal thickness ***t***.

2) Voltage distribution is proportional to the lengths of the metal tracks [3].

3) The ***k***th unit voltage difference between the adjacent half turns is regarded as constant and it is determined by averaging the beginning voltage and the ending voltage of the half turns, regardless of the type of the inductor. (Note: This assumption only using in quantifing $\boldsymbol{C}_{\mathrm{m\_m}}$, not in quantifing $\boldsymbol{C}_{\mathrm{m\_s}}$)

The length of each half turn can be defined as, $l_1, l_2, ... l_m, l_{2n}$ (***n*** is turn number, sequential *m* represent current flow direction in inductor), and the total length is defined as $l_{tot} (= l_1 + l_2 + ... + l_{2n})$. AC signal voltage of one terminal of inductor is $\boldsymbol{V}_{\mathrm{beg}}$, while that of the other is $\boldsymbol{V}_{\mathrm{end}}$. According assumptions, AC signal voltage at the end terminal of the ***m***th half turn inductor [$\boldsymbol{V}_{\mathrm{end}}$(m)] can be expressed as

$$V_{end}(m) = \frac{\sum_{j=1}^{m+1} l_j}{l_{tot}} \left(V_{beg} - V_{end} \right) \quad (5)$$

AC signal voltage at the beginning terminal of the ***m***th half turn inductor [$\boldsymbol{V}_{\mathrm{beg}}$(m)] equal to the $\boldsymbol{V}_{\mathrm{end}}$(m-1). $\boldsymbol{V}_{\mathrm{beg}}(0) = \boldsymbol{V}_{\mathrm{beg}}$.

2.2. Equivalent Capacitance C_{m_s} Formula

The lowest layer metal track of the ***m***th half turn inductor is equally divided into ***k*** units ($i \to \infty$); According to assumption 2), the voltage ***i***th unit is $\boldsymbol{V}_{\mathrm{i}}$,

$$V_i = V_{beg}(m) - \frac{i}{k} \cdot \left(\Delta V_m(i) \right) \quad (6)$$

where, $\Delta V_m(i) \overset{k \to \infty}{\equiv} \frac{1}{k} (V_{beg}(m) - V_{end}(m))$. Therefore, the electrical energy stored in the capacitor between the *i*th unit metal and the substrate can be expressed as

$$\Delta E_{c,ms}(i) = \frac{1}{2} \cdot C(i) \cdot \left(\Delta V_m \right)^2 = \frac{1}{2} \cdot \left(C_{ms} \frac{wl}{k} \right) \cdot \left(\frac{1}{k} \left(V_{beg}(m) - V_{end}(m) \right) \right)^2 \quad (7)$$

where $\boldsymbol{C}_{\mathrm{ms}}$ represents the capacitance per unit area between the ***m***th half turn and the substrate. The electrical energy stored in the equivalent capacitance between the metal tracks of the $\boldsymbol{L}_{\mathrm{ms}}$(m) and the substrate can be derived from [5]

$$E_{c,m\_s}(m) = \frac{1}{6} C_{ms} wl(m) \left(V_{beg}^2(m) + V_{end}^2(m) + V_{beg}(m) \cdot V_{end}(m) \right) \quad (8)$$

Whatever structure inductor is, we can get entire E_{c,m_s} by adding up all $E_{c,m\_s}(m)$.

Two terminal voltages of the differentially driven inductor with symmetrically planar configuration (***DSPI***), are $+\frac{1}{2} V_S$ and $-\frac{1}{2} V_s$, respectively. Hence

$$E_{c,ms\_diff} = \frac{1}{2} \bullet \left(\frac{1}{12} C_{ms} wl_{tot} \right) \bullet V_s^2 = \frac{1}{2} \bullet C_{m\_s\_diff} \bullet V_s^2 \quad (9)$$

$$C_{m\_s\_diff} = \frac{1}{12} C_{ms} \frac{wl_{tot}}{k} \quad (10)$$

where $C_{m\_s\_diff}$ is equivalent capacitance between the metal track and the substrate of the ***DSPI***.

The signal terminal voltage of the single-ended driven planar inductor (***SEPI***) is V_S and that of another terminal is 0, hence

$$E_{c,ms\_diff} = \frac{1}{2} \bullet \left(\frac{1}{3} C_{ms} wl_{tot} \right) \bullet V_s^2 = \frac{1}{2} \bullet C_{m\_s\_se} \bullet V_s^2 \quad (11)$$

$$C_{m\_s\_se} = \frac{1}{3} C_{ms} wl \quad (12)$$

where $C_{m\_s\_se}$ is the equivalent capacitance between the metal track and the substrate of the ***SEPI***.

According to equation (10) and (12), under the same equivalent area between the metal track and the substrate, we can get the following equation

$$C_{m\_s\_diff} = \frac{1}{4} C_{m\_s\_se} \quad (13)$$

The ***DSPI*** can be regarded as two ***SEPI*** that have identical substrate parasitics at signal ports, which is half

of whole inductor; Their connection point is signal ground; Signal terminal voltage is $+\frac{1}{2}V_S$ and $-\frac{1}{2}V_s$ respectively and the C_{m_s} of two inductors are in series connection, hence, we can obtain the same result as equation (13).

2.3. Equivalent Capacitance C_{m_m} Formula

The voltage difference between the ***i***th and ***j***th half turn can be expressed as

$$\Delta V_{i,j} = V_i - V_j = \frac{\sum_{k=i}^{j} l_k}{l_{tot}} \bullet \left(V_{beg} - V_{end}\right), (0 \le i, j \le n) \qquad (14)$$

The electrical energy stored in the equivalent capacitance between the metal tracks of the ***i***th half turn and ***j***th half turn can be expressed as

$$E_{c,m\_s}(i,j) = \sum_{k=1}^{N\to\infty} \Delta E_{c,m\_m}(k) = \frac{1}{2} \cdot \frac{C_{mm\_ij}(k) \cdot W \cdot \left(l_i + l_j\right) \cdot \left(\sum_{k=i}^{j} l_k\right)^2}{2l_{tot}^2} \cdot \left(V_{beg} - V_{end}\right)^2 (15)$$

where C_{mm_ij} is the unit capacitance between the ***i***th and ***j***th adjacent half turns of inductor; W is metal tracks width ***w*** of inductor (when the ***i***th half turn and ***j***th half turn are stacked) or metal thickness ***t*** (when the ***i***th half turn and ***j***th half turn are in the same layer).

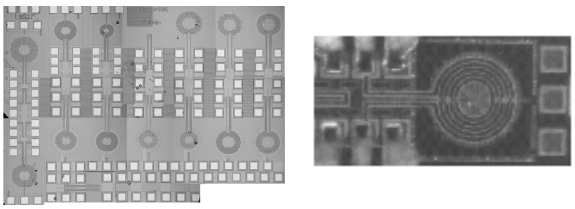
Regardless of the structures (stacked, spiral, symmetric, etc.), and driven modes (differentially or single-ended), the electrical energy stored in the equivalent capacitance between the metal can be expressed as the sum of the electrical energy stored in the equivalent capacitance between the metal traces at same layers and at the adjacent layers. Different C_{m_m} formulas can be derived from equation (15) and $E_{c,mm} = \frac{1}{2} C_{m\_m} \left(V_{beg} - V_{end}\right)^2$.

We define the C_{m_m} of the ***DSPI*** as $C_{m\_m\_diff}$, the C_{m_m} of the symmetric inductor in single-ended driven configuration (***SSEI***) as $C_{m\_m\_diff\_se}$ and the C_{m_m} of the ***SEPI*** as $C_{m\_m\_se\_spiral}$. Thus,

$$C_{m\_m\_diff} = C_{m\_m\_diff\_se} = \sum_{k=1}^{n-1} C_{mm\_k,n-k}(k) \frac{W\left(l_k + l_{n-k}\right)}{2} \left(\frac{\sum_{k=k}^{n-k} l_k}{l_{tot}} \right)^2 + \sum_{k=2}^{n} C_{mm\_k,2n+2-k}(k) \frac{W\left(l_k + l_{2n+2-k}\right)}{2} \left(\frac{\sum_{k=k}^{2n+2-k} l_k}{l_{tot}} \right)^2 \qquad (16)$$

$$C_{m\_m\_se\_spiral} = \sum_{k=1}^{2n-2} \left(C_{mm\_ij}(k) \frac{W\left(l_k + l_{k+2}\right)}{2} \left(\frac{l_{k+1} + l_{k+2}}{l_{tot}} \right)^2 \right) (17)$$

3. Model validation and design guidelines



(a) **(b)**

Figure 2. Die photos of the inductors (a) in 0.35 μm CMOS processes and (b) one inductor with probes.

In order to verify the accuracy, inductors have been fabricated in a 0.35 μm two-poly four-metal CMOS processes as shown in Figure 2 (a). The prototype chips also include the de-embed layouts to calibrate the on-wafer testing wiring and pads [6]. The ***S*** parameters were measured by a network analyzer and Cascade Microtech Probe Station using coplanar ground–signal–ground probes. The prediction error of f_{SR} and $Ratio_{f_{SR}}$ with DCM is less than 10%, demonstrating the accuracy of the DCM.

Thus, the equivalent capacitor of the inductor can be calculated, when we know the inductance, according to equation (2), (10) and (16), the ratio of the f_{SR} of the optional two inductors with equivalent inductance L_{eq1}, L_{eq2} and the equivalent capacitor C_{eq1}, $C_{eq2,}$ respectively can be expressed as

$$Ratio_{f_{SR}} = \frac{f_{SR}^{L1}}{f_{SR}^{L2}} = \sqrt{\frac{L_{eq2} \times C_{eq\,2}}{L_{eq1} \times C_{eq\,1}}} \qquad (18)$$

The inductance equal approximately, $\boldsymbol{L}_{\text{unsymmetric}} \approx \boldsymbol{L}_{\text{symmetric}}$, if the current flows in the same direction along each adjacent conductor of the planar inductors with the same geometric parameters [such as Figure 1(a),(b),(c)], and the voltage differences between the adjacent turns of the ***DSPI*** and ***SSPI*** is larger than those of the ***SEPI***, so $C_{\text{m\_m\_se\_symmetric}} = C_{\text{m\_m\_diff\_symmetric}} > C_{\text{m\_m\_se\_spiral}}$, but $4C_{\text{m\_s\_diff\_symmetric}} = C_{\text{m\_s\_se\_symmetric}} = C_{\text{m\_m\_se\_spiral}}$, therefore, $f_{\text{SR\_diff\_symmetric}} > f_{\text{SR\_se\_spiral}} > f_{\text{SR\_se\_symmetric}}$ and $Q_{\text{SR\_diff\_symmetric}} > Q_{\text{SR\_se\_spiral}} > Q_{\text{SR\_se\_symmetric.}}$ This conclusion and equation (18) can offer design guidelines to select inductor and circuit configurations.

The $Ratio_{f_{SR}}$ can be predicted and explained from equations (18). Compared with an equivalent single-ended configuration, experimental data

demonstrate that the differential inductor offers a 127% greater ***Q*** factor (maximum) and a much broader range of operating frequencies. In figure 3(a) $Ratio_{f_{SR}}(L1)/Ratio_{f_{SR}}(L2)$ =1.55. The $Ratio_{f_{SR}}$ difference of the inductors with the same metal geometry parameters can be explained by the theory that $Ratio_{f_{SR}}$ decreases with $C_{m\_m}/C_{m\_s\_diff}$ from equation (17), shown in figure 3(c). The pn junction are formed at the interface between n+ diffuse layer and p substrate, and pn junction capacitor is serially connected with the oxide capacitance between the inductor and the silicon substrate, thus the equivalent C_{m_s} are greatly reduced, but C_{m_m} of both inductors are same, i.e. $C_{m\_m}/C_{m\_s\_diff}$ is variable, resulting in different $Ratio_{f_{SR}}$. The pattern ground shielding made of the lowest layer metal make lower substrate loss than the pattern n+ floating does, therefore, $Q_{se}^{L1} > Q_{se}^{L2}$ at low frequency and $Q^{L1} < Q^{L2}$ at high frequency due to $f_{SR}^{L2} > f_{SR}^{L1}$.

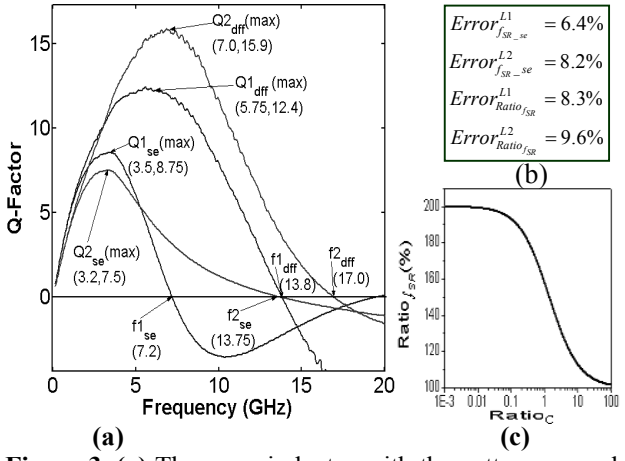


Figure 3. (a) The same inductor with the pattern ground shielding made of the lowest layer metal (L1) and pattern n+ floating (L2); (b) The prediction errors with DCM; (c) $Ratio_{f_{SR}}$ decreases with $Ratio_C = C_{m\_m}/C_{m\_s\_diff}$.

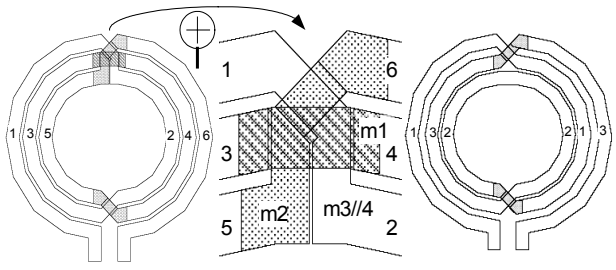


Figure 5. Two optimum symmetric on-chip inductors driven differentially. (Note:123456 is current in inductor flow direction, i.e. AC signal voltage profile; In m*i*, ***i*** represents metal layer number)

The lower the total parasitic capacitance has in an inductor, the higher quality factor the inductor has. Two optimum designs of the symmetric planar on-chip inductor driven differentially have been developed. $C_{m\_m\_diff}$ is reduced by decreasing the voltage difference between the adjacent turns in figure 2(a) through multilevel interconnects and by increasing the space of adjacent turns with larger voltage difference such as figure 2(b). According to equation (10), the $\boldsymbol{C}_{\mathrm{m\_m}}$ will be reduced if the lowest metal tracks layer of the stacked or 3D inductor has the voltage nearer signal ground.

In addition, ***DCM*** can be high accurate at different structure inductors if the current crowding effects are considered in assumption 2).

4. Conclusions

A differentially driven symmetric inductor that enhances inductor quality factor on silicon RF ICs is firstly interpreted by a distributed capacitance model (***DCM***) for monolithic inductors. Design guidelines can be obtained from ***DCM***.

Acknowledgments

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