A Simple Equivalent Circuit Model for CMOS Multi-Level Spiral Inductors

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***Abstract*—This paper presents a simple structure equivalent circuit model for multi-level spiral inductor on silicon substrates. Skin effect and proximity effect are well modeled by additional RL branch and mutual inductance. For multi-level inductors, since all metal wires couple laterally to each other through the substrate, coupling between wires and between metal layers can be modeled by a parallel combination of resistance and capacitance. Verification with measurement data from a series of multi-level spiral inductors in 2P4M Si process demonstrates accurate performance over wide band frequency range.**

***Index Terms*—inductor model, spiral inductor, multi-level, wide band.**

I. Introduction

Nowadays, on-chip spiral inductors have been widely used in monolithic radio-frequency circuits, such as low noise amplifiers, voltage-controlled oscillators and passive-element filters. Since CMOS spiral inductors are introduced, many methods have reported to enhance the inductors performance on silicon substrates. This has included the use of thick dielectric layers between the inductor metal and substrate, the use of multi-metal layers to increase the effective thickness of the spiral inductor and thereby reduce loss and the connection of multi-metal layer spirals in series to reduce the area of the inductors [1][2].

Distributed lumped element model is usually adopted in modeling multi-level spiral inductor [3][4]. It takes long time to simulate and optimization the circuit based on distributed model. However, traditional lumped element model for inductors contains frequency dependent elements, so it is not compatible with transient analysis and harmonic balance analysis. Furthermore, it cannot well modeling the character of the multi-level inductors. In this article, we presents a simple structure lumped element model for multi-level spiral inductor on silicon substrates. The components of the model have been extracted from the measured S-parameter data.

The novel equivalent circuit model is discussed in section 2 compared with traditional spiral inductor model. The model results are compared with the measurement data in section 3 and the conclusions are summarized in section 4.

II. Inductor Model

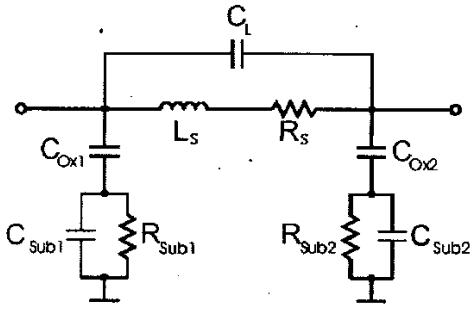

Fig 1 Traditional lumped element model for spiral inductors

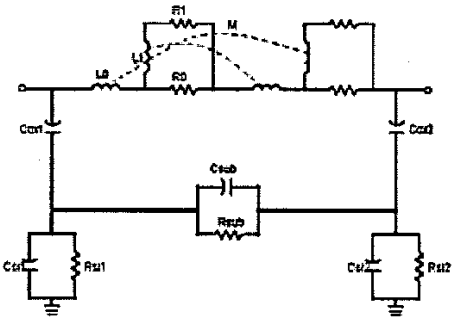

Fig 2 Proposed model for multi-level inductors

Fig. 1 reviews the traditional lumped element circuit. In this model, L and R_L represent series metal

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inductance and resistance, C_L modeling fringing and feed-through capacitance, C_{OX} modeling dielectric isolation capacitance. Substrate loss R_{SUB} and C_{SUB} are also modeled. Extracted L_S and R_S are frequency-dependent, model based on these parameters is not compatible with transient analysis. A common compromise is to extract L and R_L at a specific frequency and use these fixed values for further circuit simulation and optimization. While in wide band MMIC design, this approach will introduce significant error. Furthermore, for multi-level inductors, mutual inductance between layers and mutual inductance between metal wires cannot neglect. Traditional model, which not model these effects, is inappropriate for multi-level inductors.

In this paper, we propose a new equivalent circuit model for Multi-level spiral inductors (Fig 2). The problems mentioned above are well solved.

As we all know, the DC current is uniformly distributed inside a single metal wire, it can be modeled as L_0 and R_0 in series. At high frequencies, the current flow is limited to the outer surface of the metal wire, in order to represent the skin effect, additional RL branches can be added in parallel to R_0 [5].

Due to the close proximity between wires in a spiral inductor, the current in each segment can induce eddy currents in other segments and cause the resistance to increase, causing deterioration of Q. In [6], stacked wires have large mutual coupling coefficient K and as a result, the mutually induced eddy current is more significant compared to the adjacent wires in the same layer. So mutual inductance M should be modeled in multi-level inductors.

For multi-level inductors, since all metal wires couple laterally through the substrate, coupling between wires and coupling between metal layers can be represented by a parallel combination of R_{SUB} and C_{SUB}. The shunt RC structure has been addressed in the distributed model [7], while our model can save much time due to its simple structure.

Fig 2 shows the ultimate equivalent circuit model proposed for multi-level on-chip inductors. Dielectric isolation capacitance are modeled by C_{OX}, and substrate loss R_{SUB} and C_{SUB} are also modeled. Feed-through capacitance modeling the parasitic capacitive coupling between input and output ports of the spiral inductor is neglected, due to existent capacitive coupling through C_{OX1}, C_{SUB} and C_{OX2}.

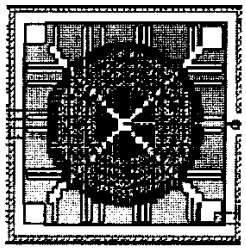


Fig 3 four-turn four-metal-layer inductor with patterned ground shields

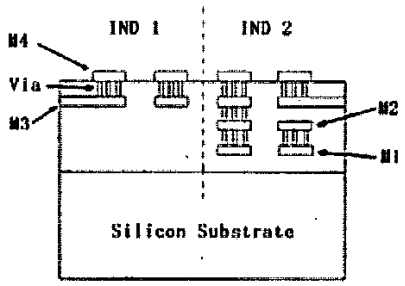


Fig 4 Cross-sectional view of the multi-level inductors

III. Model Verification

In order to verify proposed model in this article, two multi-level inductors were fabricated using standard 0.35 μm CMOS process, with four metal levels on silicon substrate of 8Ω-cm resistivity. Patterned ground shields (PGSs) were used to improve the performance of inductors by decoupling the inductor from the substrate [8], seen in fig 3. Spiral inductor IND 1 are formed using top metal layer (M4) and third metal layer (M3), while IND 2 are formed using all four metal layers supplied in the process. Shunt structures between layers are realized through vias. Fig 4 shows the sketch map of the both multi-level inductors. The structures of the inductors are summarized in Table I. Both inductors were measured by Agilent 8719ES from 50MHz to 8GHz.

TABLE I

Inductor	Number of turns	Metal width (μm)	Spacing (μm)	Metal Layers	Connection between layers
IND 1	5	15	1	M3 M4	Shunt
IND 2	4	15	1	M1 M2 M3 M4	Shunt-serial-shunt

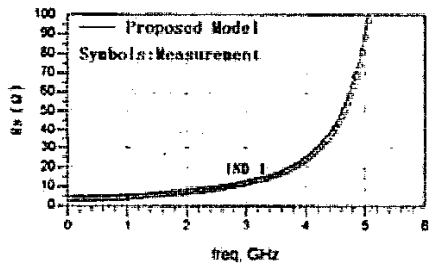
To characterize the intrinsic inductor, the pad parasitics were de-embedded from the measurement using open and short pad structures.

Key parameters L_0 and R_0 in the proposed model were calculated by ASITIC [9]. Other parameters were extracted by fitting the proposed model to the measured S-parameters.

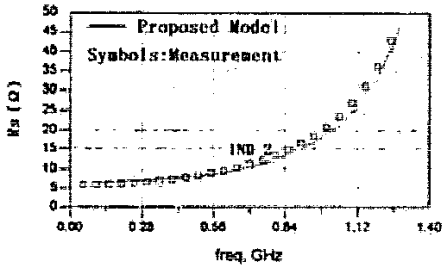
To verify the model validity, frequency dependent parameters L_S, R_S used in the traditional model are calculated by (1) and (2).

$$L_S = -\frac{\mathrm{Im}ag(\frac{1}{Y_{21}})}{2\pi f} \qquad (1)$$

$$R_S = -\mathrm{Re}al(\frac{1}{Y_{21}}) \qquad (2)$$



(a)



(b)

Fig5 Frequency dependent series inductance based on traditional model

Frequency dependent R_S and L_S curves are shown in Fig 5 and Fig 6. As can be seen from the figure, the proposed model predicts the change in inductance and resistance as a function of frequency.

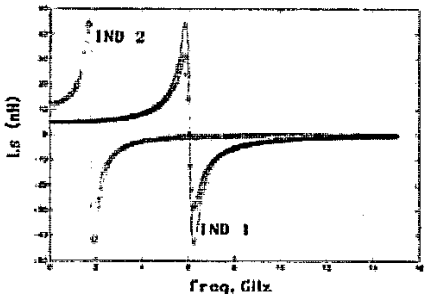
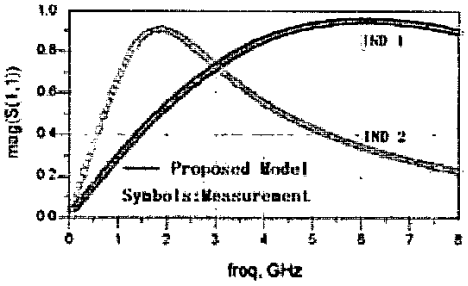
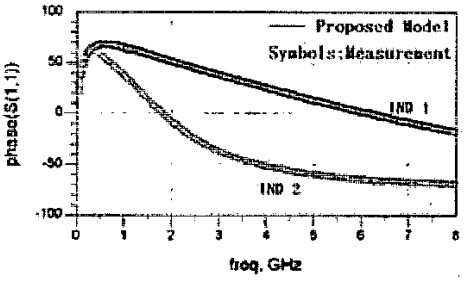


Fig6 Frequency dependent series inductance based on traditional model

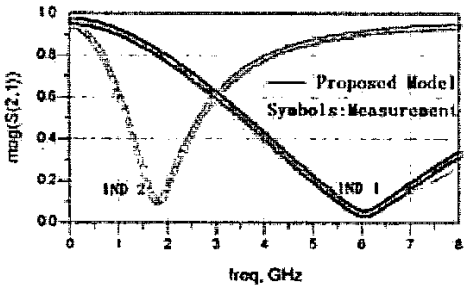
Fig 7 shows the measured and modeled S-parameters of IND 1 and IND 2. As shown from the figure, the S-parameter of the proposed model match the measured data well in the frequency band before resonance. However, the character from 50MHz to 8GHz is presented.



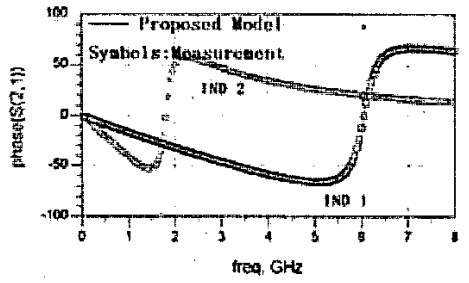
(a) S11 magnitude



(b) S11 phase



(c) S21 magnitude



(d) S21 phase

Fig 7 Comparison between measured and modeled S-parameter

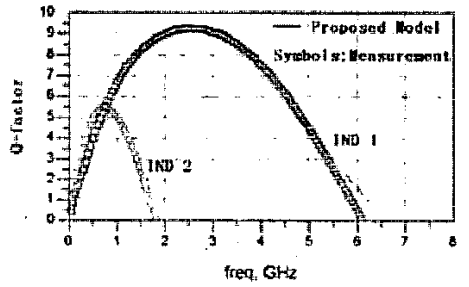


Fig 8 Quality factor comparison of the proposed model with measurement data

Quality factor can be calculated as

$$Q = -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \qquad (3)$$

The rapid degradation of Q at high frequencies is a combined effect of the substrate loss and the self-resonance. Fig 8 verifies Q for different structures mentioned above. The new lumped element equivalent circuit accurately models the peak value and frequency response of the quality factor. The frequency relative departure for the peak value of Q is no more than 5%.

IV. Conclusions

A new lumped element equivalent circuit model for on chip multi-level spiral inductors has been developed. Verification with measurement data from two different test structures has demonstrated the validity of the proposed model. Since all elements are frequency independent, it is compatible with harmonic balance analysis, transient analysis and wide-band design. This new model can be implemented in SPICE-compatible simulators to improve accuracy in circuit simulation.

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