A 12th Order Active-RC Filter with Automatic Frequency Tuning for DVB Tuner Applications

Liang Zou[1], Kefeng Han[1], Youchun Liao[2], Hao Min[1] and Zhangwen Tang[1]*

[1]ASIC & System State Key Laboratory, Fudan University, Shanghai 201203, China

[2]Ratio Microelectronics Technology Co., Ltd, Shanghai 200433, China

***Abstract*—A 12th order active-RC filter for DVB Tuner applications with automatic frequency tuning (AFT) is presented in this paper. The filter is implemented in Butterworth biquad structure. The AFT circuit is introduced to compensate the frequency variation by a 7-bits switched-capacitor array. The measurement results indicate that the precision of tuning circuit can be controlled less than ±2.3%, the in-band group delay variation is 70ns, and the in-band IM3 achieves -60dB with -27dbm input power. This proposed filter circuit, fabricated in a SMIC 0.18μm CMOS process, consumes 6mA current with 1.8V power supply.**

I. INTRODUCTION

The main purpose of the analog channel filter in RF receiver is to select the desired signal, and provides anti-aliasing for the following ADC. Channel selection can be implemented in either analog or digital domain. The implement in analog domain increases the requirement of analog filter's dynamic range, but lower the ADC's resolution. The implement in digital domain can conquer the variation of components, the phase and gain error in analog filter, but requires increased resolution and dynamic range of ADC. The power of ADC will swiftly increase as the increased resolution requirement, which can be shown as (1),

$$P_{ADC} = E_{conv} \cdot 2^N \cdot f_S \text{ (Nyquist-Rate ADC)} \quad (1)$$

where E_{conv} is the required power for one bit, 2^N is the number of bits, and f_S is the sample rate [1].

In RF tuner system, wide bandwidth and high linearity requirements make the ADC difficult to implement. To lower the power of ADC and obtain a good adjacent channel rejection (ACR) before ADC, here the high orders analog filter is adopted to achieve good attenuation, and the active-RC architecture is selected to achieve high linearity. The cut-off frequency of integrated active-RC filter is determined by on-chip resistor and capacitor which may vary much with process and temperature. So automatic frequency tuning (AFT) circuit should be engaged to calibrate the frequency variation. The total tuner receiver architecture is shown in Fig. 1.

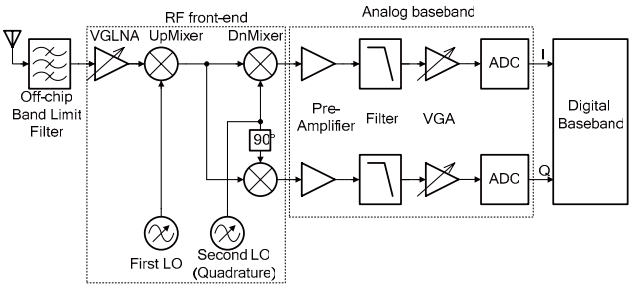

Figure 1 Architecture of RF Tuner Receiver

Section II illustrates the design of filter core circuit. Section III shows the implement of tuning circuit in detail, and proposed critical design insights to minimize the non-ideal factors which will affect the precision of tuning. Section IV gives some measurement results, such as frequency response, group delay and in-band IM3.

II. FILTER CORE CIRCUIT DESIGN

In our tuner receiver, system design specifies the cut-off frequency 11MHz, and requires the filter to achieve 60dB ACR@ 22MHz. A 12th order Butterworth filter is chosen here for the flat pass-band and sharp transition-band frequency response. The Two-Thomas biquad is adopted to implement the Butterworth function as shown in Fig. 2.

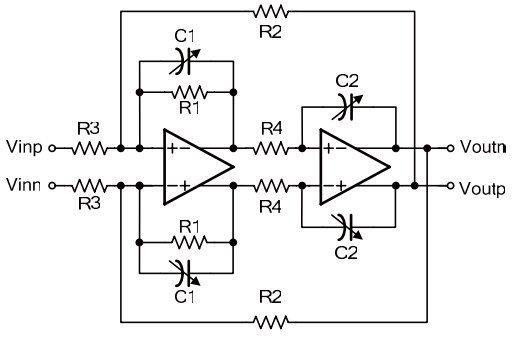

Figure 2 Biquad Integrator

*Corresponding author. Email: zwtang@fudan.edu.cn

There are some equations in Two-Thomas biquad, which can be shown as follows,

$$\omega_0^2 = \frac{1}{R_2 R_4 C_1 C_2},\ Q = \frac{R_1}{\sqrt{R_2 R_4}}\sqrt{\frac{C_1}{C_2}},\ A_0 = \frac{R_2}{R_3} \quad (2)$$

where A_o is the DC gain of integrator, ω_o is the cut-off frequency, Q is the quality of integrator.

Assume R_2=R_4, C_1=C_2, Equ. (2) can be rewritten as,

$$\omega_0^2 = \frac{1}{R_2 C_1},\ Q = \frac{R_1}{R_2},\ A_0 = \frac{R_2}{R_3} \quad (3)$$

From (3), Q and A_0 are determined by the ratio of resistors, and both Q and ω can be tuned independently [2].

This 12th order Butterworth filter consists of six cascaded biquads, the high Q biquad is placed in the end of filter chain to maximize linearity performance. Here, the capacitor is designed to be a programmable switched-capacitor array with binary-weighted to obtain adjustable RC constant, which is controlled by 7-bits digital signals, as shown in Fig. 3.

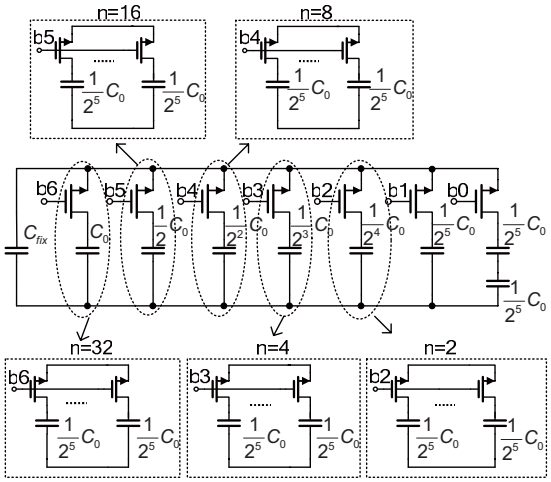

Figure 3 7-bits Digital Controlled Switched-capacitor Array

Sources of MOS-Switches are connected with the input nodes of the OTAs to reduce the nonlinearity of switches, but the parasitic capacitor at input nodes increased, which cause the phase lag [3]. Layout of switched-capacitor array should be considered carefully to assure the monotony.

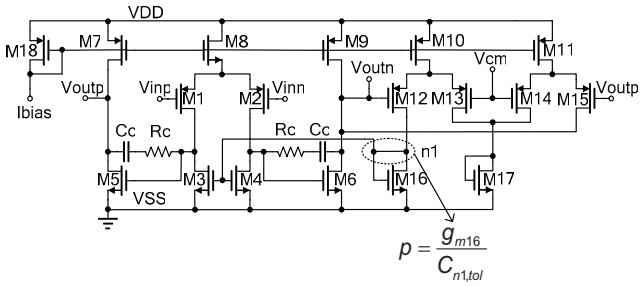

Figure 4 Fully Differential Two-stage Amplifier

Amplifier in Tow-Thomas biquad is shown in Fig. 4. It's a fully differential two-stage amplifier, two-stage structure is used to improve the differential gain. R_C and C_C acts as miller compensation to achieve 75 degree phase margin. Common-mode feedback circuit is designed to stable the common-mode operation point of output, a pole which located at $p=g_{m16}/C_{n1,tol}$ is additionally introduced to the common-mode loop as shown in Fig. 4. The gain of common-mode circuit can not be set too large to affect the stability of common-mode loop. The GBW of amplifier should be wide enough to conquer gain peaking around cut-off frequency. Requirement of GBW can be shown as [4]:

$$GBW \geq \left|\frac{A_C(j\omega_L)}{\delta} - 1\right| \left|[1 + A_C(j\omega_L)]\omega_L\right| \quad (4)$$

where the $A_C(j\omega_L)$ is the open loop gain of amplifier, ω_L is the cut-off frequency of filter, δ is the error between ideal transform function and non-ideal transform function. Another, the Slew Rate, equivalent input noise and THD should be considered in amplifier design.

III. TUNING CIRCUIT DESIGN

A. Tuning Circuit

Accurate cut-off frequency is necessary in filter to satisfy both the channel selection and adjacent channel rejection. To meet ±3% frequency variation of system requirement, a Master-Slave tuning circuit is introduced here to adjust the absolute precision by relative precision. Every tuning circuit needs an absolute reference. Commonly, there are only two absolute references which are Bandgap voltage and crystal frequency. Here the frequency of crystal oscillator is chosen to keep the same dimension with the RC constant. The mean to realize the RC tuning is carried out by adjusting the switched-capacitor array [5]. The overall schematic of proposed tuning circuit is illustrated in Fig. 5.

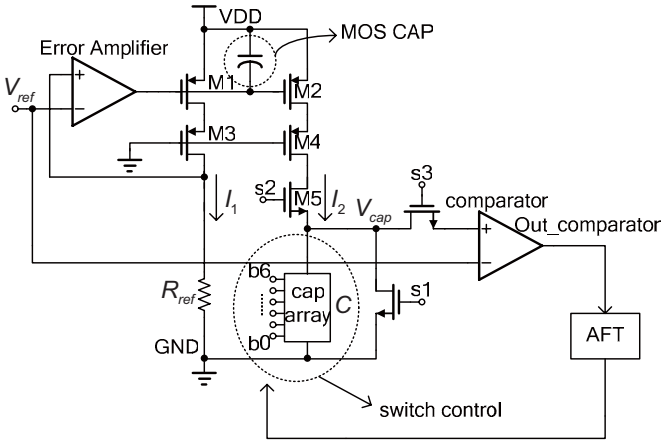

Figure 5 Tuning Circuit

First, a voltage reference is obtained from Bandgap output after voltage dividing, separately connects with the inputs of error amplifier and comparator. A current reference can be got as I_1=V_{ref}/R_{ref} through the feedback of error amplifier, and then a mirror current can be generated to charge the switched-capacitor array to get a voltage V_{cap}. V_{cap} and V_{ref} can be compared by a comparator, the comparison result enter into the AFT algorithm to form a feedback loop. By controlling the digital input signal of switched-capacitor, V_{cap} will equal to the V_{ref} after tuning. The process can be shown as follows,

$$V_{cap} = \frac{\Delta Q}{C} = \frac{I_2 \Delta t}{C} = \frac{I_1 \Delta t}{C} = \frac{V_{ref}}{R_{ref} C} \Delta t \quad (5)$$

$$\Rightarrow \frac{V_{cap}}{V_{ref}} = \frac{\Delta t}{R_{ref} C} \quad (6)$$

After tuning, V_{cap} is equal to V_{ref}, namely,

$$\frac{V_{cap}}{V_{ref}} = 1 \quad (7)$$

Substituting (7) into (6),

$$\Delta t = R_{ref} C \quad (8)$$

where Δt is the multiples of crystal oscillator's period, R_{ref} is the on-chip poly resistor, which keeps the relative precision with the resistors in filter core circuit, and the capacitor C in tuning circuit is equal to the capacitor in filter core. So the constant time $R_{ref}C$ is determined by Δt after tuning, and the $R_{ref}C$ keeps the relative precision with the constant time of filter core circuit. In another word, the cut-off frequency is tuned to keeps the relative precision with the frequency of crystal oscillator. The tuning control logic is implemented by binary search algorithm to save calibration time. Here the crystal frequency is chosen to be 25MHz, and the detailed timing plan in one comparison step is illustrated in Fig. 6. The whole calibration needs seven comparison steps, consumes only 8.96μs.

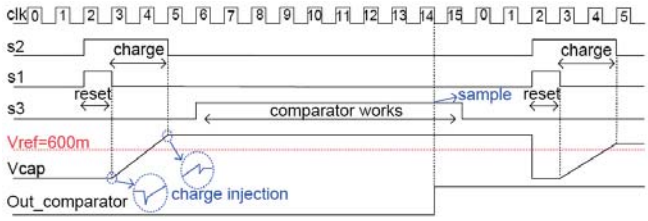

Figure 6 Timing Plan

B. Tuning Error

Error factors which affect the precision of tuning can be summarized as follows: quantization error of switched-capacitor array, resistor and capacitor mismatch between master and slave circuit, current mismatch, offset voltage of amplifier, charge injection of MOS switches, and clock feed-through, etc.

The programmable switched-capacitor array in Fig. 3 is considered as a capacitor DAC whose input is digital and output is capacitance.

$$C_{\max} = C_{fix} + (2 - \frac{1}{2^6}) C_0 \quad (9)$$

$$C_{\min} = C_{fix} \quad (10)$$

$$C_{center} = \sqrt{C_{\max} \bullet C_{\min}} \quad (11)$$

To cover the ±20% variation of resistors and capacitors over different process corners, here we choose C_{max}/C_{min}=2.25/1, the quantization error of CAP-DAC is,

$$E_q = \frac{C_0 / 2^{n-1}}{C_{center}} \quad (12)$$

where n is the number of digital control bits.

To satisfy 3% tuning precision, here n=7 is chosen to achieve 0.65% quantization error. Commonly, in the same chip, resistor mismatch between master and slave circuit can be controlled within 0.5% with suitable size and excellent layout, and the capacitor mismatch can be controlled under 0.2%. Besides RC mismatch, current mismatch is another important contribution, which can be designed to below 0.5%. All the other contributions should be controlled within 1%, thus the total tuning error can be controlled under 3%. To minimize these tuning errors, some useful design considerations are proposed as follows.

Amplifier offset, including random offset and systematic offset, affects the comparison result. The random offset can be minimized by engaging big size and small overdrive voltage of input transistors [6]. In Fig. 5, if comparator is implemented by the same with the error amplifier, symmetrically layout, the systematic offset voltage will be cancelled. Assuming ΔV is the offset voltage of amplifier between positive input and negative input in Fig. 5, the following equation can be got by (6),

$$\frac{V'_{cap}}{V'_{ref}} = \frac{\Delta t}{R_{ref} C} \quad (13)$$

After tuning, $V'_{cap} = V_{ref} + \Delta V = V'_{ref}$,

$$\Rightarrow \Delta t = R_{ref} C \quad (14)$$

From (14), the systematic offset voltage can be cancelled

The main consideration of current bias design is to minimize the difference between current I_2 and I_1 during the whole charging process. Here, the cascode transistors are applied to improve the output resistance for a good DC match. Also, the lengths of current mirrors are chosen to be 6μm and the overdrive voltages of M1 and M2 are designed to be large as 600mV to improve the match. While there is still trade-off when sizing M1 and M2, because large transistors may deteriorate clock feed-through effects, and then worsen dynamic current mismatch. MOS CAP in Fig. 5 is engaged to reduce clock feed-through. When switched-capacitor array is charging, V_{cap} increases as the time, and current I_2 will vary nonlinearity. So, the value of V_{ref} can't be set too high. Also the value of charging current should be designed carefully to get a reasonable charging time.

In tuning circuit as shown in Fig. 5, three MOS switches are introduced. The sizes of all the switches are chosen to be as small as possible to decrease charge injection which is shown in Fig. 6. When S1 turns on, V_{cap} is pulled down to GND, the lager W/L of S1 will help to lower the turn-on resistor but increase charge injection, it's also a trade-off. When S2 turns on, the bias current I_2 starts to charge the switched-capacitor array. There usually needs an initial time for current bias settling, which will cause dynamic current mismatch. In our timing design, the initial settling current is avoided to charge the capacitor array as shown in Fig. 6.

IV. Experimental Results

The proposed filter circuit was implemented in SMIC 0.18μm technology. The chip micrograph is shown in Fig.7, and the active area of filter including both I and Q channel is 1.4mm×0.9mm. As shown in Fig.8, flat pass-band response is obtained with less than 0.5dB in-band ripple, and 60dB ACR is achieved at 22MHz.

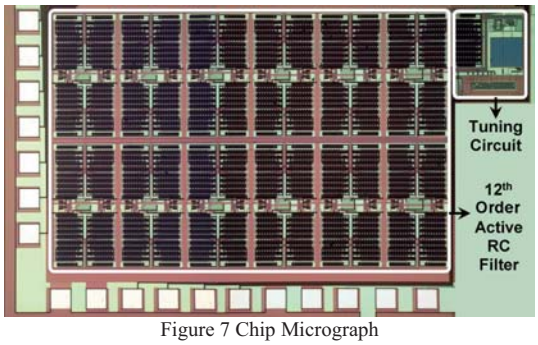

Figure 7 Chip Micrograph

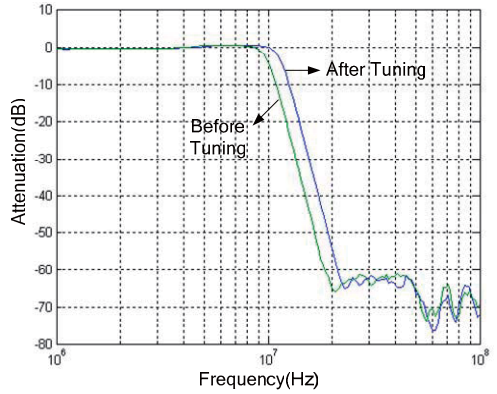

Figure 8 Frequency Response

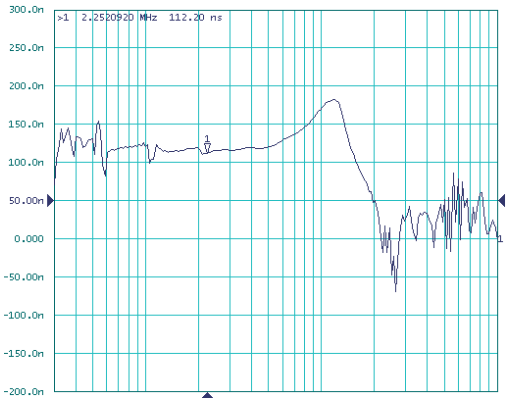
Figure 9 Measured Group Delay

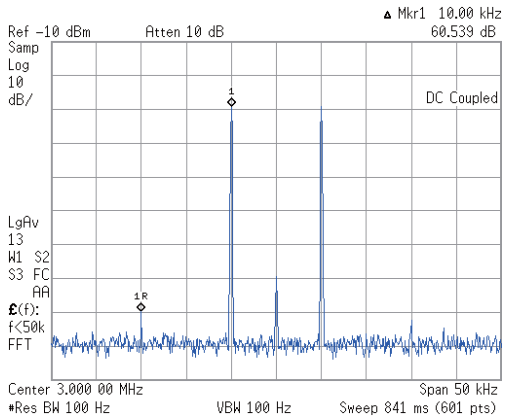

Figure 10 Measured IM3

Lots of measurement results show the cut-off frequency can be calibrated to less than 2.3%. As shown in Fig. 9, 70ns in-band group delay is achieved. Two-tone test is given in Fig. 10, which indicates that the in-band IM3 achieves -60.5dB with -27dBm input power. The performance of proposed filter is summarized at Table 1.

Table 1 Summary of the Measurement Results

Technology	CMOS 0.18 μm
Supply Voltage	1.8 V
Power Consumption	6mA×1.8V=10.8mW
Area	1.4 mm×0.9 mm (for both I&Q)
-3dB Frequency	11 MHz
Pass-band Ripple	< 0.5 dB
ACR@22 MHz	> 60 dB
In-band Group Delay Variation	70 ns
In-band IM3@input power -27dBm	-60.5 dB
Tuning Error	± 2.3%
Tuning Time	8.96 μs

V. CONCLUSION

A 12th order active-RC filter with automatic frequency tuning is proposed in this paper. The tuning circuit is analyzed in detail, and the measurement result indicates the tuning error can be controlled under ± 2.3%. This LPF is applied to a TV tuner receiver to implement channel selection and ACR. The result of two-tone test is given, which shows -60.5dB in-band IM3 with -27dBm input power. In-band group delay variation is 70ns, which is acceptable in tuner system specification. The proposed filter circuit, fabricates in a SMIC 0.18μm CMOS process, consumes only 6mA current with 1.8V power supply.

ACKNOWLEDGMENTS

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REFERENCES

[1] Jarkko Jussila, Kari Halonen, "Minimization of power dissipation of analog channel-select filter and Nyquist-rate AD converter in UTRA FDD," *IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 940-943, May 2004.

[2] Rolf Schaumann, Mac E. Van Valkenburg, "Design of Analog Filters", *Oxford University Press*, 2001.

[3] Jarkko Jussila, "Analog Baseband Circuits for WCDMA Direct-Conversion Receivers", P.H.D Dissertation, *Helsinki University of Technology*, 2003.

[4] DingKun Du, Yongming Li, Zhihua Wang, "An Active-RC Complex Filter with Mixed Signal Tuning System for Low-IF Receiver," *IEEE Asia Pacific Conference on Circuits and Systems*, pp. 1031-1034, December 2006.

[5] Seyeob Kim, Bonkee Kim, Min-Su Jeong, Jung-Hwan Lee,Youngho Cho, Tae Wook Kim, Bo-Eun Kim, "A 43dB ACR low-pass filter with automatic tuning for low-IF conversion DAB T-DMB tuner IC," *IEEE European Solid-State Circuits Conference*, pp. 319-322, September 2005

[6] Willy M.C. Sansen, "Analog Design Essentials", *Springer*, 2006.