Switch-embedded opamp-sharing MDAC with dual-input OTA in pipelined ADC

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A switch-embedded opamp-sharing multiplying digital-to-analogue converter (MDAC) with dual-input-differential-pair operational transconductance amplifier (OTA) is proposed to eliminate the non-resetting and successive-stage crosstalk problems in the conventional opamp-sharing technique. A 10-bit 80 MS/s pipelined analogue-to-digital converter (ADC) is implemented in a 0.18 μm CMOS process by using the proposed MDAC. Compared with a traditional opamp-sharing ADC, the measured signal-to-noise ratio is improved from 55.9 to 60.1 dB and the spurious free dynamic range is improved from 66 to 76 dB without any additional power or area consumption or clock phase.

Introduction: Applications used in many electronic systems, such as video decoder and wireless communication, require high-resolution low-power analogue-to-digital converters (ADCs). One of the most efficient ways to save power is opamp-sharing between successive pipelined stages. However, that is achieved at the cost of resolution reduction, since the opamp-sharing ADC has two serious problems. First, because the opamp input summing node is never reset, every input sample will be affected by the error voltage stored on the input capacitor due to the previous sample. Thus it suffers from the memory effect, which can be considered as a kind of offset [1]. Secondly, there is a potential crosstalk path between two successive stages caused by the parasitic capacitors of switches that are used to implement opamp sharing. The signals in the current and successive stages, which appear at input nodes of the shared opamp, will influence each other through the crosstalk path. In addition, the opamp-sharing switches also introduce charge injection and input-dependent resistances. These factors deteriorate both the signal-to-noise ratio (SNR) and the linearity. To alleviate the non-resetting problem, feedback signal polarity inverting (FSPI) is used to alternate the signal polarity, but it can only reduce the opamp offset by 2/3 [2]. To break the crosstalk path, isolation switches are added to tie the parasitic capacitor to ground, and the signal-to-noise-and-distortion ratio (SNDR) is improved by 1–2 dB, but the added switches increase the series resistances and the charge injection [3]. Although opamp current reuse can solve the problems of non-resetting and the crosstalk path by using both NMOS and PMOS input differential pairs in shared opamps, the capacitive level shifter increases the design complexity and the PMOS input differential pair decreases the power efficiency [4].

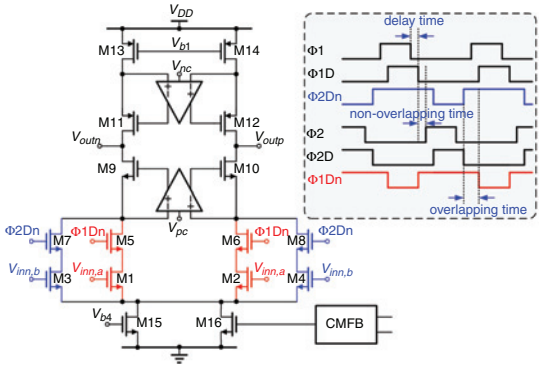

Fig. 1 *Proposed dual-input-differential-pair gain-boosting telescopic amplifier with clock timing*

Proposed switch-embedded opamp-sharing MDAC: To get rid of the problems of non-resetting and successive-stage crosstalk, a gain-boosting telescopic operational transconductance amplifier (OTA) with a dual-input-differential-pair is proposed, as shown in Fig. 1. Each input transistor (M1–M4) is connected with a MOS switch (M5–M8) in series, respectively. The switch is on when its corresponding control signal (i.e. Φ1Dn and Φ2Dn) is high, and is off when the control signal is low. By careful biasing, the switches with small invariable resistances will not affect the performance of the shared opamp. A 1.5-bit opamp-sharing multiplying DAC (MDAC) using the proposed OTA is shown in Fig. 2. When Φ1 is high, both $V_{inp,a}$ and $V_{inn,a}$ are connected to the common-mode input voltage V_{icm}, while $V_{inp,b}$ and $V_{inn,b}$ are the active differential inputs of the shared opamp. In the meantime, the shared opamp works in holding mode for the S-B stage. Similarly, when Φ2 is high, both $V_{inp,b}$ and $V_{inn,b}$ are tied to V_{icm}, while $V_{inp,a}$ and $V_{inn,a}$ are the active differential inputs of the shared opamp. The shared opamp works in holding mode for the S-A stage. Since both input pairs are reset to a common-mode input voltage alternately, the memory effect is completely eliminated without any additional clock phase. Furthermore, the opamp-sharing switches are embedded into the opamp instead of in series between the capacitor and the opamp input, therefore the crosstalk path is avoided. In addition, the charge injection and the input-dependent resistance do not exist for the same reason.

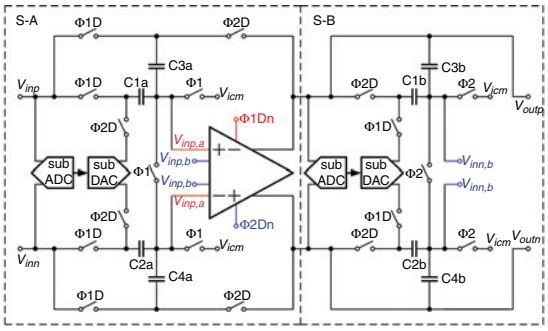

Fig. 2 *Schematic of opamp-sharing MDAC*

Timing considerations: The two-phase non-overlapping clock is always used in a pipelined ADC, but is not suitable for controlling the opamp-sharing switches in the proposed OTA. Because two input differential pairs will be disabled in the non-overlapping period, there is no current path to ground for the above PMOS transistor branches (M11–M14). The output voltage of the shared opamp will shift to a much higher level above the common output voltage during the non-overlapping period. In the worst case, the above PMOS transistors may enter into the linear region and the holding phase of MDAC stages would waste some time in the large-signal slew-rate. Therefore, the proposed opamp uses two-phase overlapping clocks (Φ1Dn and Φ2Dn) to avoid this problem. Since Φ1Dn and Φ2Dn are already used for the CMOS switches, no additional clock phase is needed. The overlapping working will not affect either the fidelity of signal transfer or settling or the quantisation process. On the one hand, during the overlapping period, the shared opamp has not been working for signal settling until Φ1D/Φ2D is high. Signal transfer and settling will not be affected because there is no charge leakage path and the two input differential pairs will not affect each other. On the other hand, the comparing operation has already been achieved at a moment between the falling edges of Φ1 and Φ1D, so the overlapping working has no adverse effect on the quantisation process either.

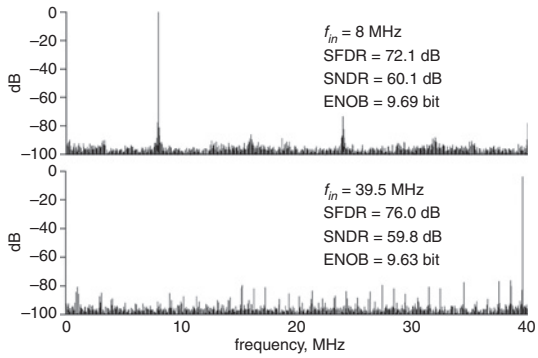

Fig. 3 *Measured FFT plot at sample frequency of 80 MHz with input signals of 8 and 39.5 MHz*

Experimental results: A common pipelined ADC is implemented by using the proposed MDAC. The ADC is composed of an S/H circuit, eight 1.5-bit MDACs using four shared opamps, and a 2-bit flash ADC as the last stage. The ADC is fabricated in a 0.18 μm CMOS process. The chip consumes 28 mW from a 1.8 V power supply at

80 MS/s. Fig. 3 shows the FFT plot for the input frequencies of 8 and 39.5 MHz at 80 MHz sample rate. The ADC achieves a peak SNDR of 60.1 dB and a peak spurious free dynamic range (SFDR) of 76 dB, while the effective number of bits (ENOB) is maintaining more than 9.6 bit for the full Nyquist input bandwidth. When the input frequency is close to the sample rate, the ADC still maintains 9.47 ENOB. Fig. 4 shows the measured SNDR and SFDR compared between this work and a traditional ADC with the additional isolated switches as in [3], and the two ADCs are the same except the shared method of opamp. A performance summary is shown in Table 1.

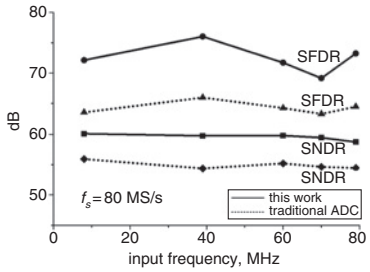

Fig. 4 *Measured SNDR and SFDR compared between this work and traditional opamp-sharing ADC*

Table 1: Performance comparisons of traditional and proposed ADC

	Traditional ADC	This work
Opamp-sharing method	Adding isolated switches	Switch-embedded
Resolution	10 bits	
Sample rate	80 MS/s	
Process	0.18 μm CMOS (MIM cap)	
Input range	1.6 V_{pp}	
SNDR	55.9 dB	60.1 dB
SFDR	66 dB	76 dB
DNL	+0.75/ − 0.63 LSB	+0.37/ − 0.23 LSB
INL	+0.84/ − 1.12 LSB	+0.53/ − 0.87 LSB
Power consumption	28 mW	
Active die area	1.1 mm^2	

Conclusions: This Letter describes a switch-embedded opamp-sharing MDAC based on a dual-input-differential-pair opamp. A 10-bit 80 MS/s pipelined ADC was implemented by using the proposed MDAC. Compared with a traditional opamp-sharing ADC, the proposed opamp-sharing method eliminates the memory effect and crosstalk path without any additional power or area consumption or clock phase. The measured SNDR and SFDR are improved from 55.9 to 60.1 dB and from 66 to 76 dB, respectively.

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One or more of the Figures in this Letter are available in colour online.

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