A Sub-0.75° RMS-Phase-Error Differentially-Tuned Fractional-N Synthesizer with On-Chip LDO Regulator and Analog-Enhanced AFC Technique

Lei Lu, Lingbu Meng, Liang Zou, Hao Min and Zhangwen Tang

Fudan University, Shanghai, China
Outline

• Motivation
• System Architecture
• Level Shifter for Symmetrical Tuning Curves
• High-PSR LDO Regulator
• Digital AFC with Monitor
• Measured Results
• Conclusions
Motivation

• Symmetrical tuning curves
  – Level Shifters eliminate threshold voltage

• Large noise from power supply deteriorates VCO severely
  – High-PSR LDO Regulator

• Frequency drift due to temperature variation
  – Control Voltage monitor to restart AFC
Single-Ended Tuned Synthesizer

- Advantage: Single-ended CP and VCO
- Disadvantage: Susceptible to CM noise, large LPF area
Differentially Tuned Synthesizer

- Advantage: Immune to CM noise, small LPF area (differential LPF)
- Disadvantage: differential CP and VCO
Simplified differential $LC$-tank

- Differential tuning of VCO
  - Inversion MOS transistors as varactors

![Diagram of differential LC-tank](image)
Conventional Differentially Tuned Techniques

\[ V_{ccm} = \frac{(V_{cp} + V_{cn})}{2} \]

\[ V_{ocm} = \frac{(V_{op} + V_{on})}{2} \]

\[ C_n \]

\[ V_{thn} \]

\[ V_{ocm} = \frac{(V_{op} + V_{on})}{2} \]

\[ C_p \]

\[ V_{thp} \]
Asymmetrical Tuning Curves

• Inversion MOS varactors have both p-type and n-type
  – Better choice in differentially tuned VCO than accumulation transistors
• Lead to asymmetrical tuning curves even if $V_{ccm}$ is equal to $V_{ocm}$ [See Soltanian, et al., CICC’06]
• The middle point of tuning curves deviates from $V_{ocm}$ by $V_{thn} + |V_{thp}|$
Proposed Differentially Tuned Techniques with Level Shifters

\[ V_{ocm} - V_{thn} + V_{gsn} = V_{ccm} \]

\[ V_{ocm} + |V_{thp}| - |V_{gsp}| = V_{ccm} \]
High-PSR LDO Regulator

- $V_{in}=1.5V$
- Add one zero to improve stability
- Sense $V_{DD}$ variation to improve PSRR
- Pass Transistor
- Cancelled
- VCO load with buffer
- $15mA$
- $C_L$
Simulated Noise and PSR of LDO
AFC and Voltage Monitor (1)

- Flow chart
  - 80 μs is enough for locking

Digital AFC start

- Count VCO clock and compare
  - $|\varepsilon| \leq 2$?

Shift VCO band

- >8th Comp?
  - Y
  - AFC finished
  - N
  - Shift VCO band

Wait 80 μs

- $V_{cl} < V_{cp}$, $V_{cn} < V_{ch}$?
  - Y
  - Shift VCO band
  - N

Digital AFC Voltage Monitor
AFC and Voltage Monitor (2)

- Set two boundary for control voltages
  - Ensure control voltages fall between them

\[ V_{cl} < V_c < V_{ch} \]

\[ \Delta f = \text{Linear Range} (\Delta V_c) \]
Other Circuits Details

- **VCO**
  - Complementary cross-coupled transistors
  - Two tail inductors to lower the phase noise

- **Charge Pump**
  - Differentially configured
  - Rail-to-rail CMFB

- **Loop Filter**
  - On-chip MIM capacitor and high-res poly resistor

- **Delta sigma modulator & P/S Counter**
  - Programmed using Verilog language
Die Micrograph

1.47mm

0.18μm CMOS process 1P6M

Prescaler

LC VCO

AFC&DSM

LDO

LPF

PFD & CP

1mm
Measured Tuning Curves

- Tuning range: 1.2 ~ 2.1 GHz
- Coarse tuning: 8-bit control, 256 sub-bands
Measured Phase Noise

- Typical fractional-\(N\) case: 1.6135 GHz
Phase Noise With and Without LDO
Loop Bandwidth and Phase Error

- Phase error: Integrated from 100 Hz to 40 MHz
Measured Locking Process

- Locking time: 20 μs (6.4 μs for AFC)
## Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18-µm CMOS</td>
</tr>
<tr>
<td>Die Area</td>
<td>1.47 mm × 1 mm</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.8 V (VCO with 1.5 V)</td>
</tr>
<tr>
<td>Current</td>
<td>16 mA</td>
</tr>
<tr>
<td>Ref. Clock</td>
<td>25 MHz</td>
</tr>
<tr>
<td>Output Freq.</td>
<td>1.2 GHz ~ 2.1 GHz</td>
</tr>
<tr>
<td>Phase Noise (dBc/Hz)</td>
<td>Integer-N: -100@10kHz</td>
</tr>
<tr>
<td></td>
<td>Fractional-N: -96@10kHz</td>
</tr>
<tr>
<td>Phase Error</td>
<td>Integer-N: &lt;0.5°_RMS</td>
</tr>
<tr>
<td></td>
<td>Fractional-N: &lt;0.75°_RMS</td>
</tr>
<tr>
<td>Locking Time</td>
<td>20 µs</td>
</tr>
</tbody>
</table>
Conclusions

• Have proposed level shifters to ensure symmetrical tuning curves
• Have demonstrated high-PSR LDO regulator
• Have introduced voltage monitor to overcome frequency drift
• Have achieved superior phase noise and phase error performance across the whole wideband tuning range