A Sub-0.75°RMS-Phase-Error Differentially-Tuned Fractional-*N* Synthesizer with On-Chip LDO Regulator and Analog-Enhanced AFC Technique

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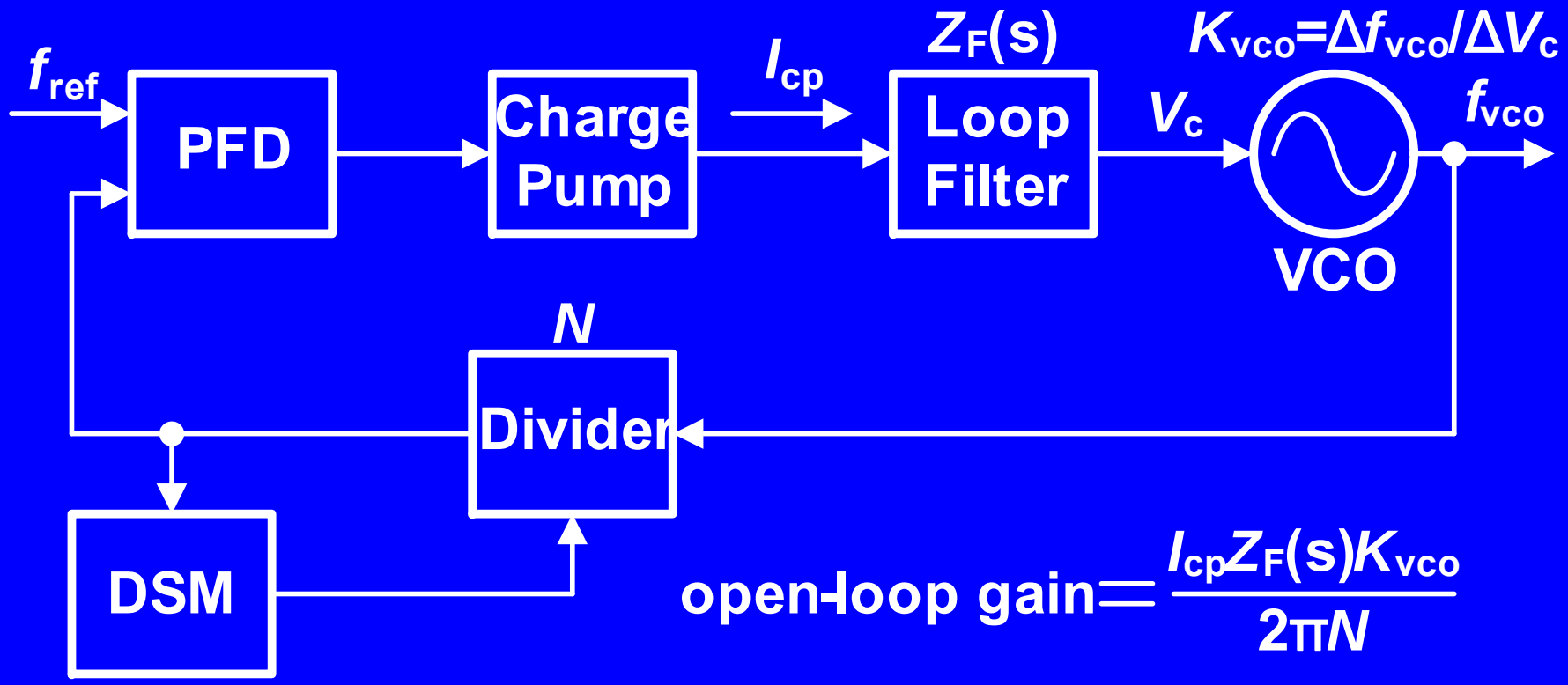
Outline

- Motivation
- System Architecture
- Level Shifter for Symmetrical Tuning Curves
- High-PSR LDO Regulator
- Digital AFC with Monitor
- Measured Results
- Conclusions

Motivation

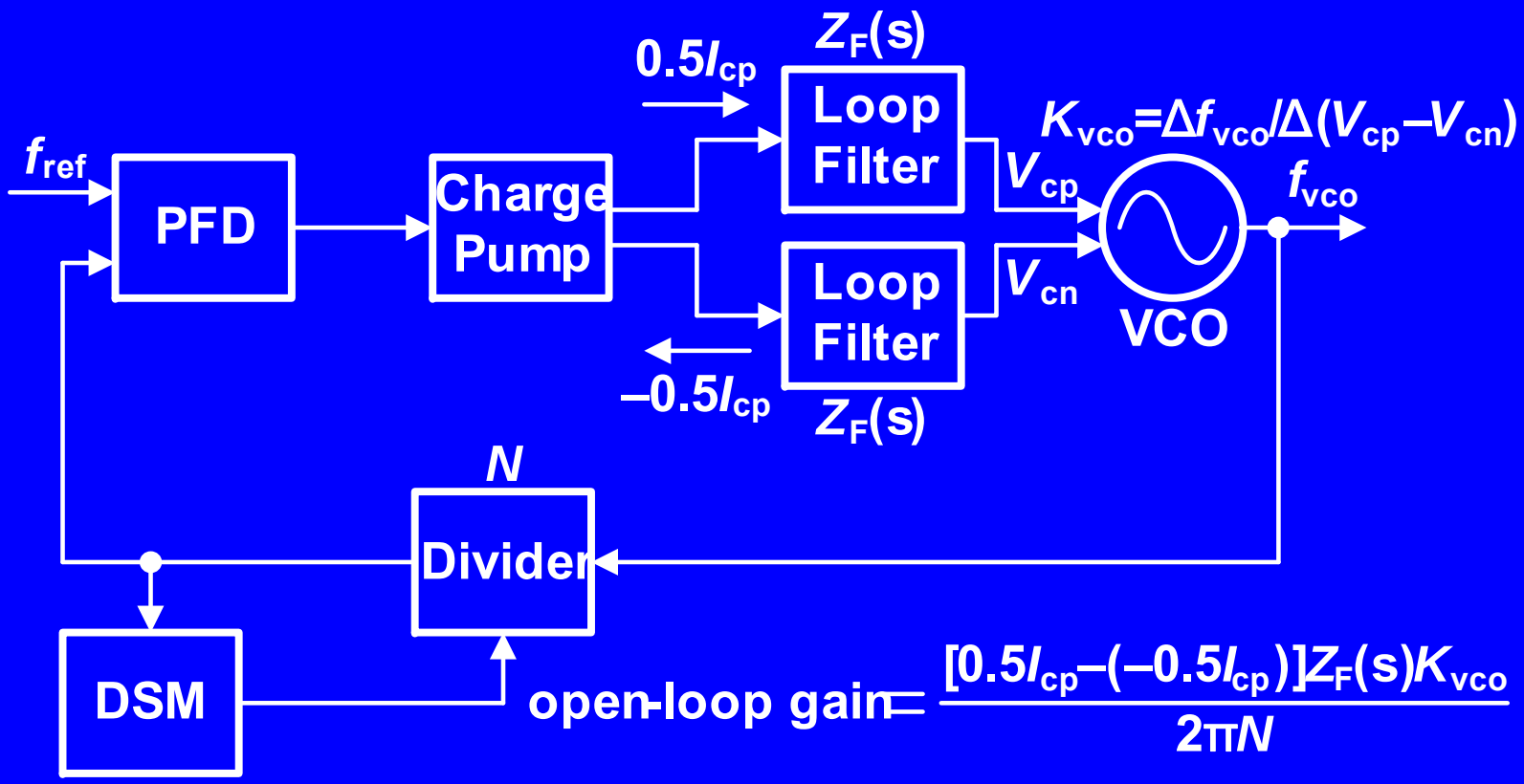
- Symmetrical tuning curves
  - Level Shifters eliminate threshold voltage
- Large noise from power supply deteriorates VCO severely
  - High-PSR LDO Regulator
- Frequency drift due to temperature variation
  - Control Voltage monitor to restart AFC

Single-Ended Tuned Synthesizer



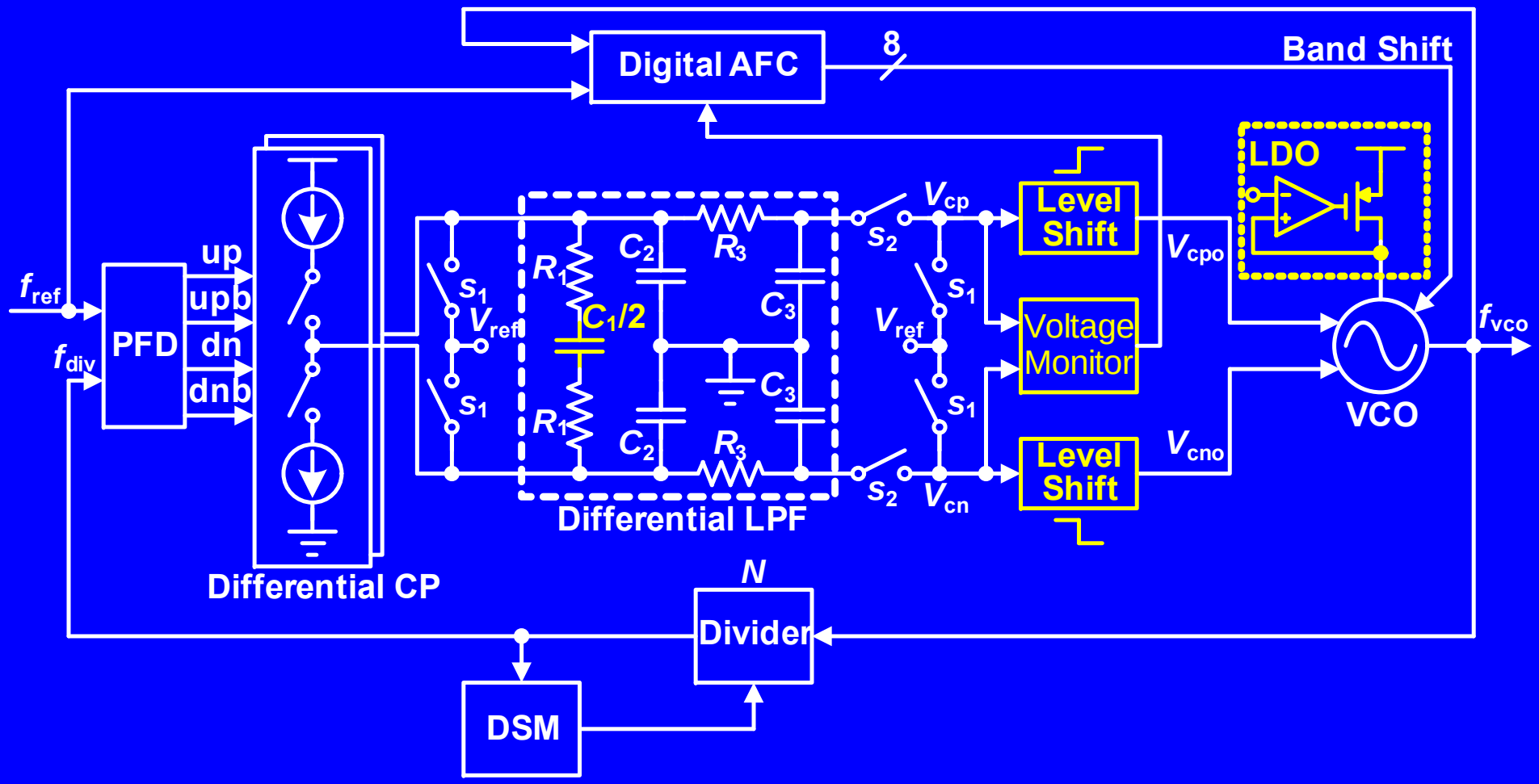
- Advantage: Single-ended CP and VCO
- Disadvantage: Susceptible to CM noise, large LPF area

Differentially Tuned Synthesizer



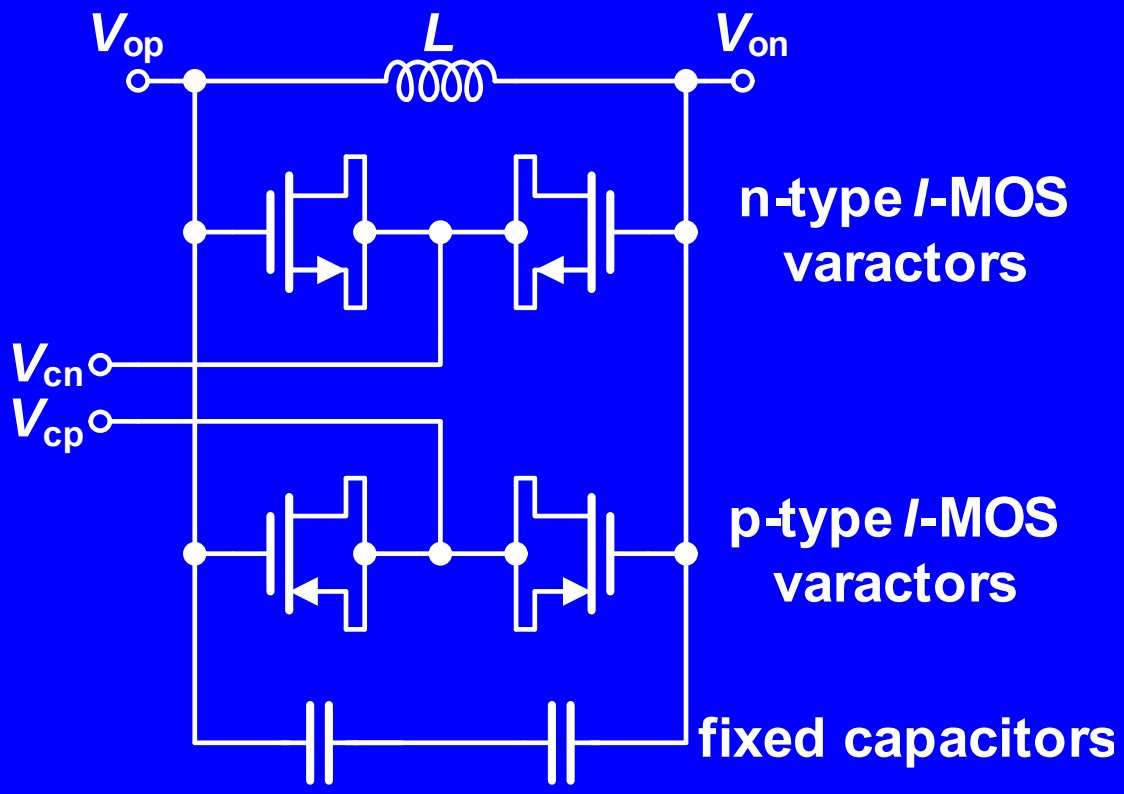
- Advantage: Immune to CM noise, small LPF area (differential LPF)
- Disadvantage: differential CP and VCO

Synthesizer Block Diagram

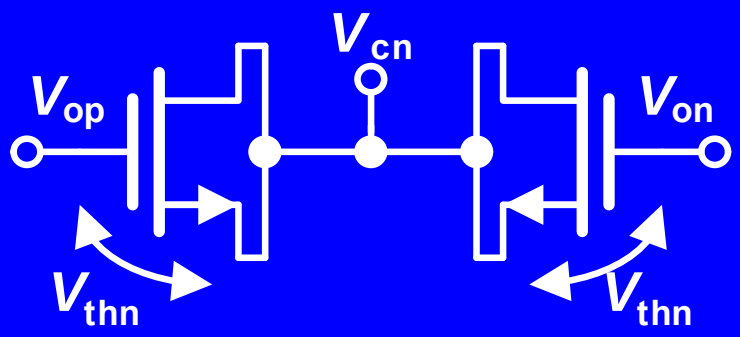


Simplified differential *LC*-tank

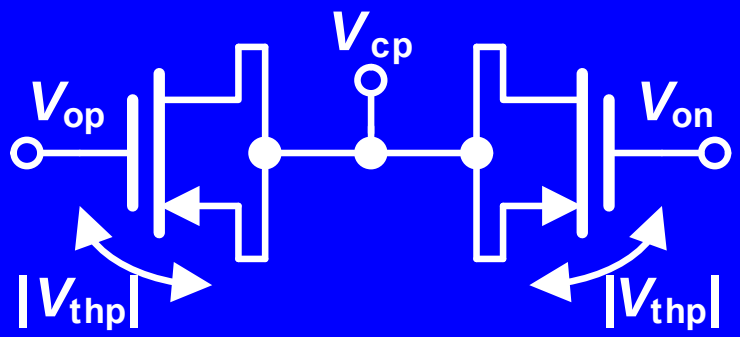
- **Differential tuning of VCO**
  - **Inversion MOS transistors as varactors**

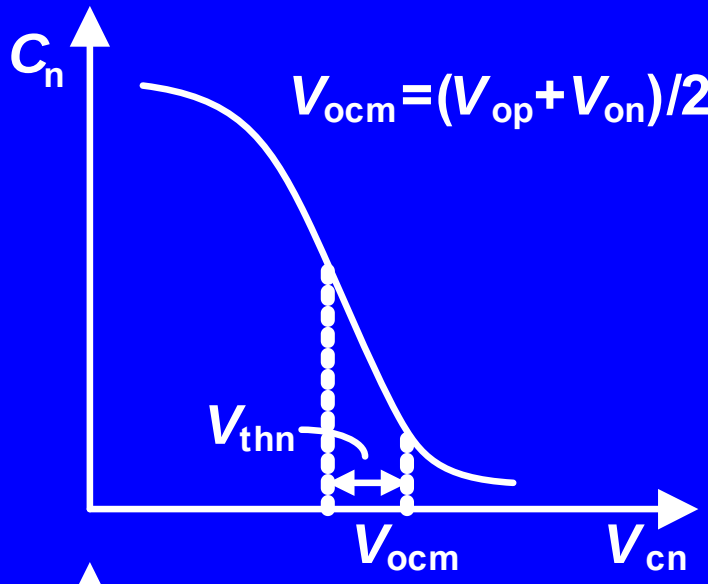


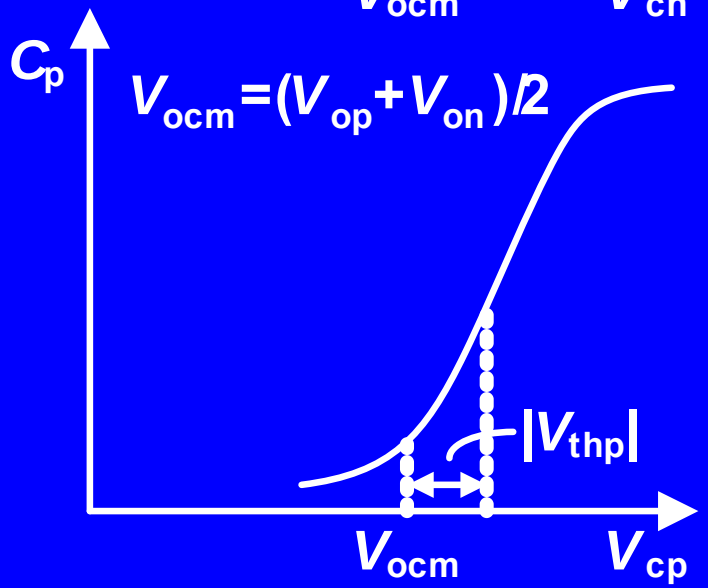
Conventional Differentially Tuned Techniques



$$V_{ccm}=(V_{cp}+V_{cn})/2$$



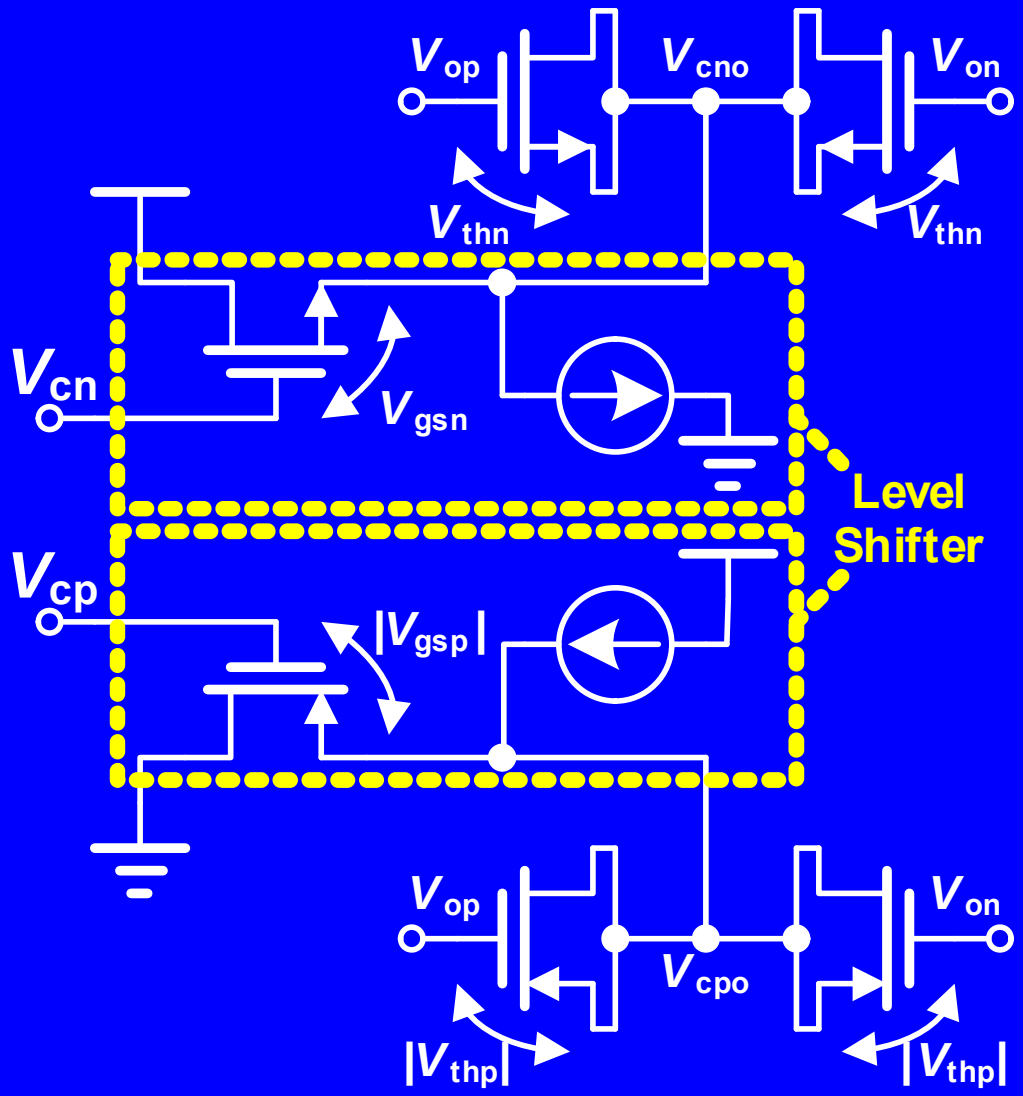


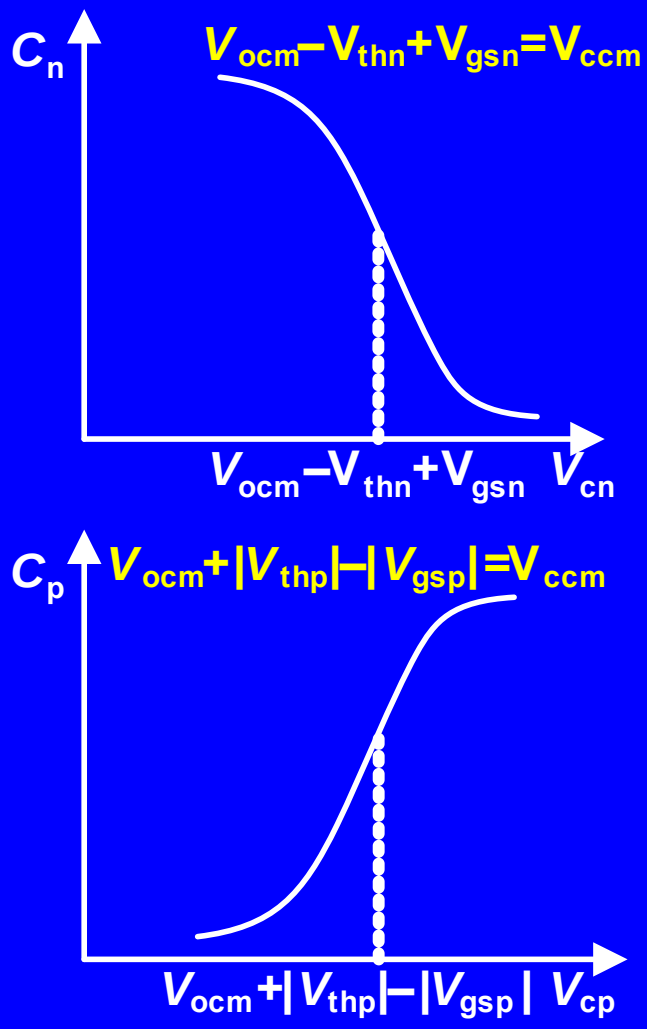


Asymmetrical Tuning Curves

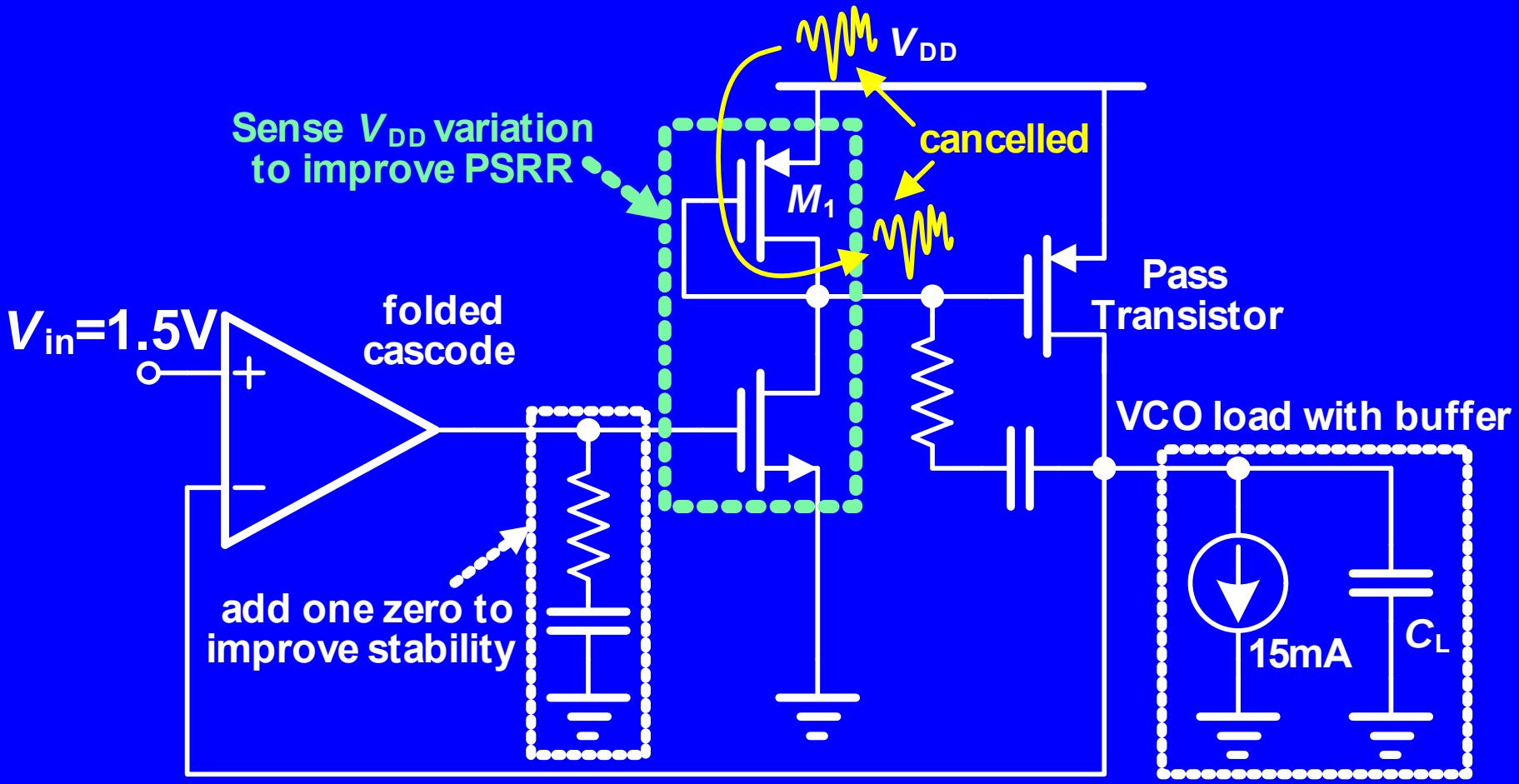
- Inversion MOS varactors have both p-type and n-type
  - Better choice in differentially tuned VCO than accumulation transistors
- Lead to asymmetrical tuning curves even if V_{ccm} is equal to V_{ocm} [See Soltanian, et al., CICC'06]
- The middle point of tuning curves deviates from V_{ocm} by $V_{thn}+|V_{thp}|$

Proposed Differentially Tuned Techniques with Level Shifters

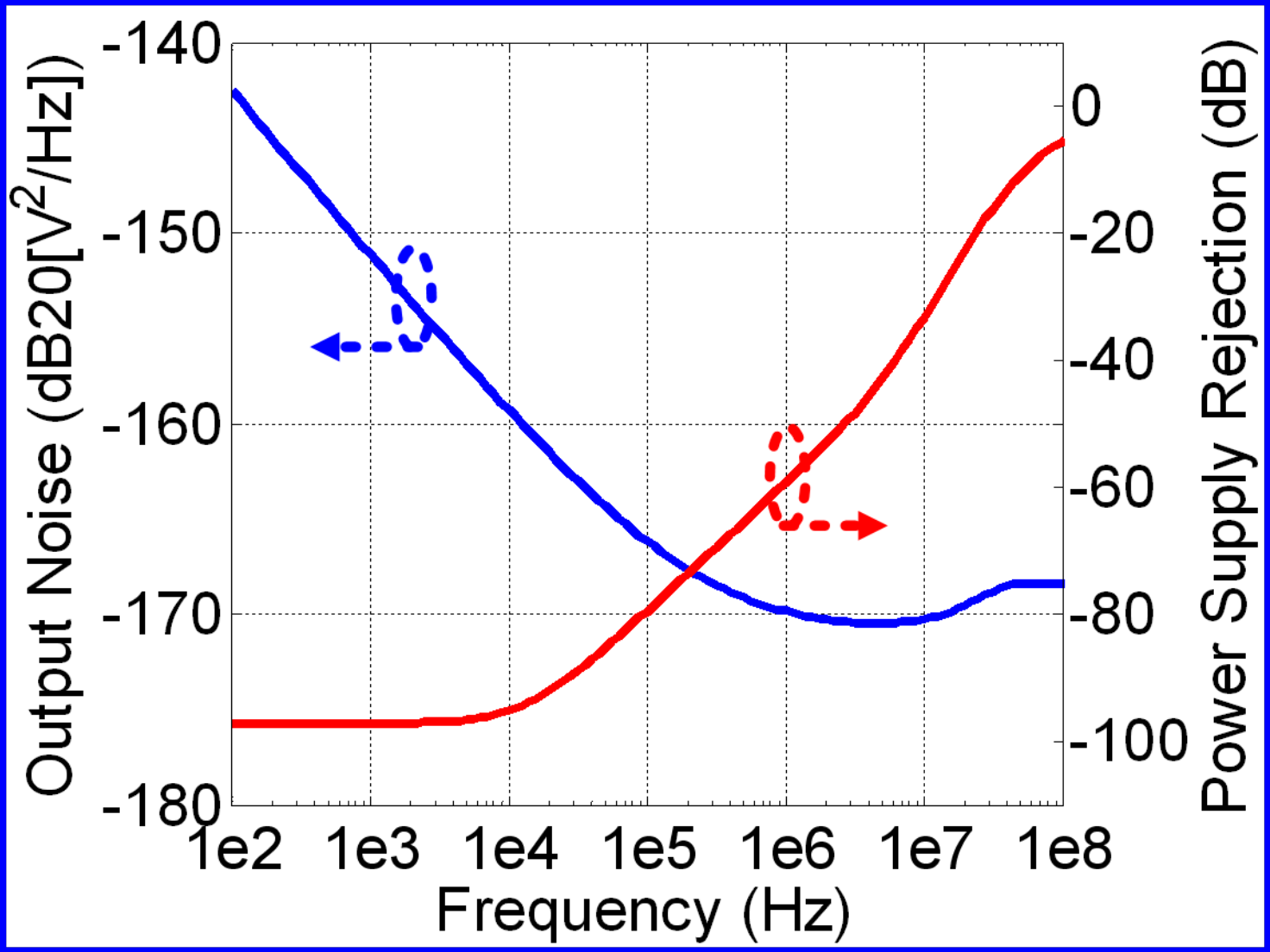




High-PSR LDO Regulator

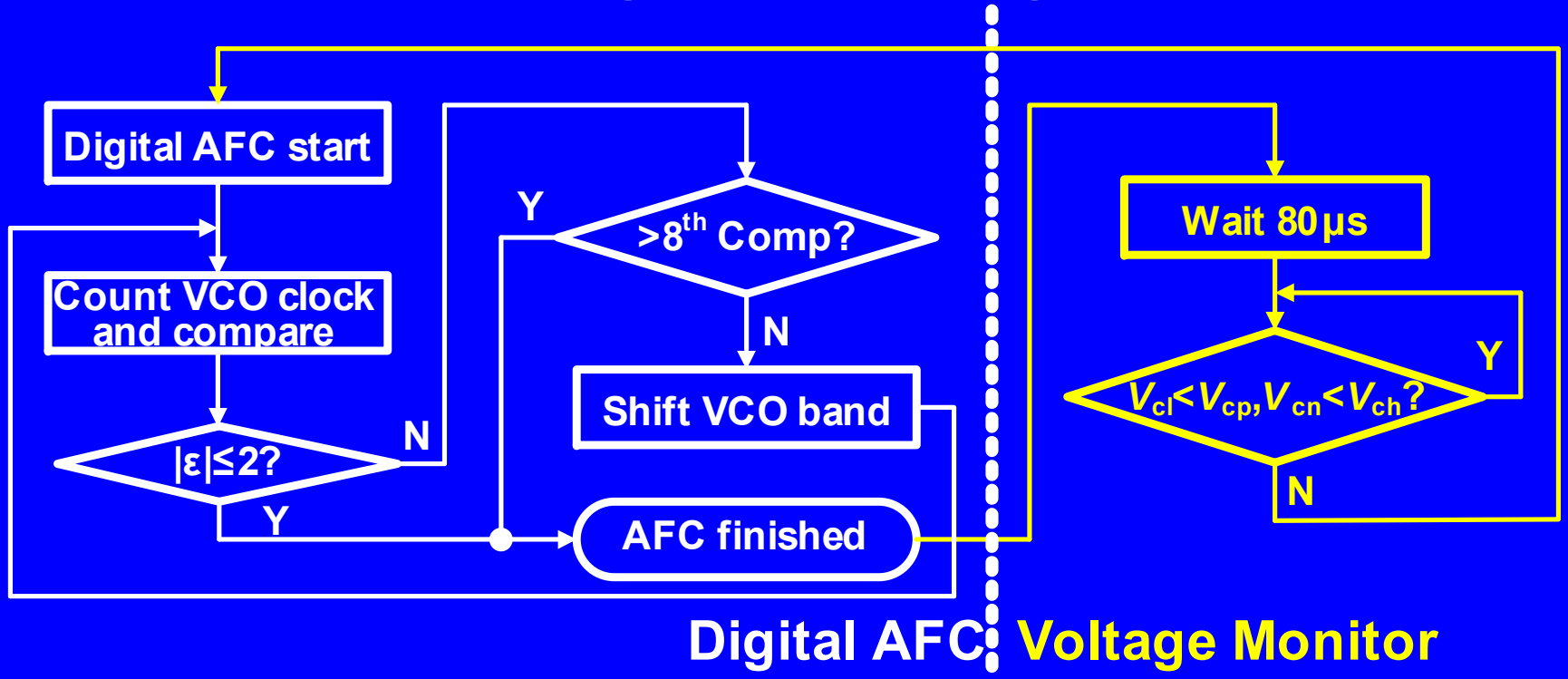


Simulated Noise and PSR of LDO



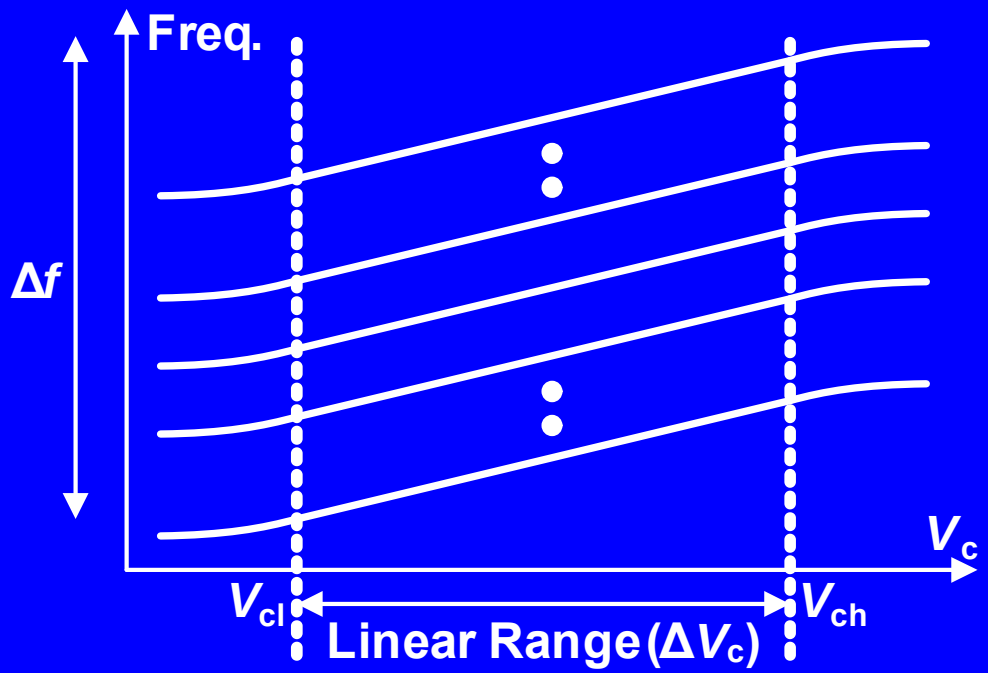
AFC and Voltage Monitor (1)

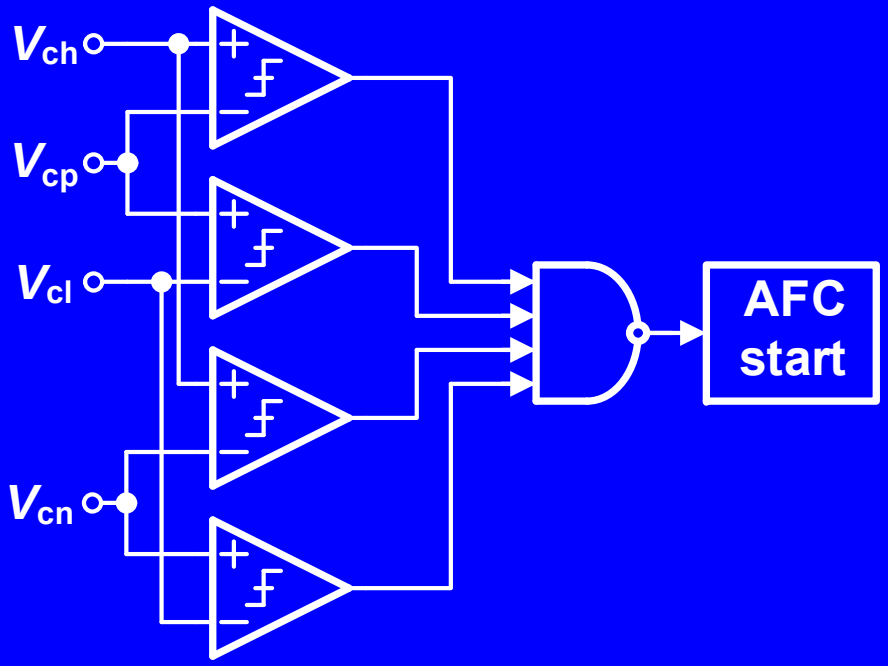
- **Flow chart**
  - 80 μs is enough for locking



AFC and Voltage Monitor (2)

- Set two boundary for control voltages
  - Ensure control voltages fall between them

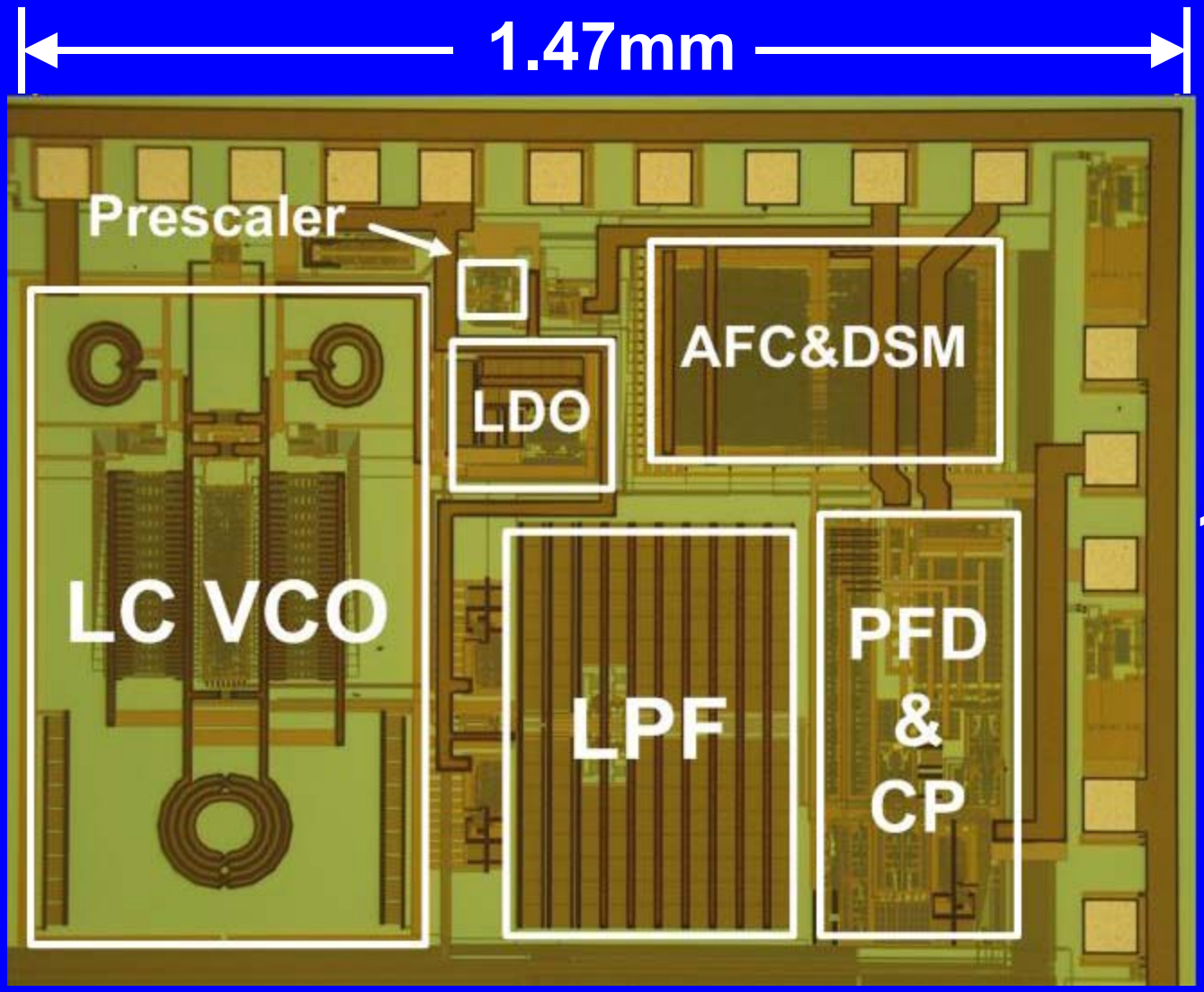




Other Circuits Details

- VCO
  - Complementary cross-coupled transistors
  - Two tail inductors to lower the phase noise
- Charge Pump
  - Differentially configured
  - Rail-to-rail CMFB
- Loop Filter
  - On-chip MIM capacitor and high-res poly resistor
- Delta sigma modulator & P/S Counter
  - Programmed using Verilog language

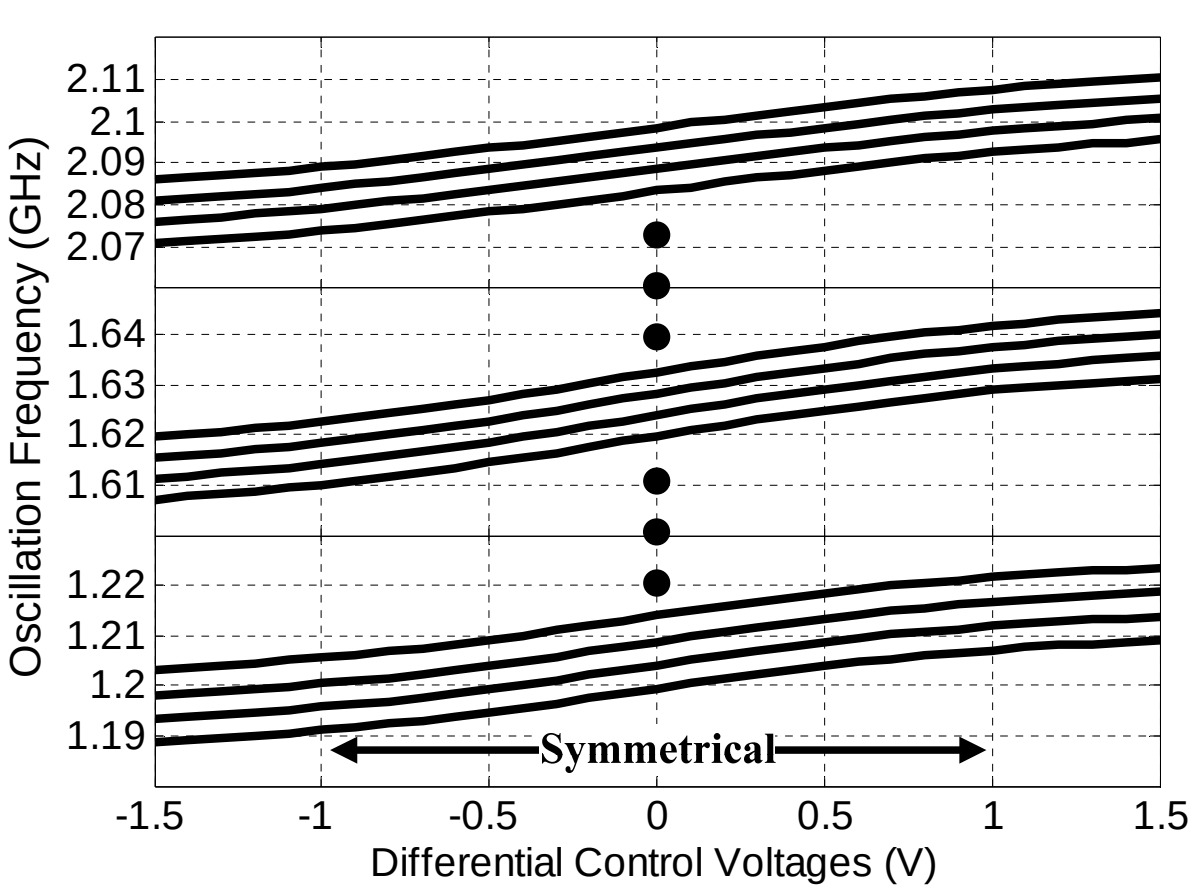
Die Micrograph



0.18µm CMOS process 1P6M

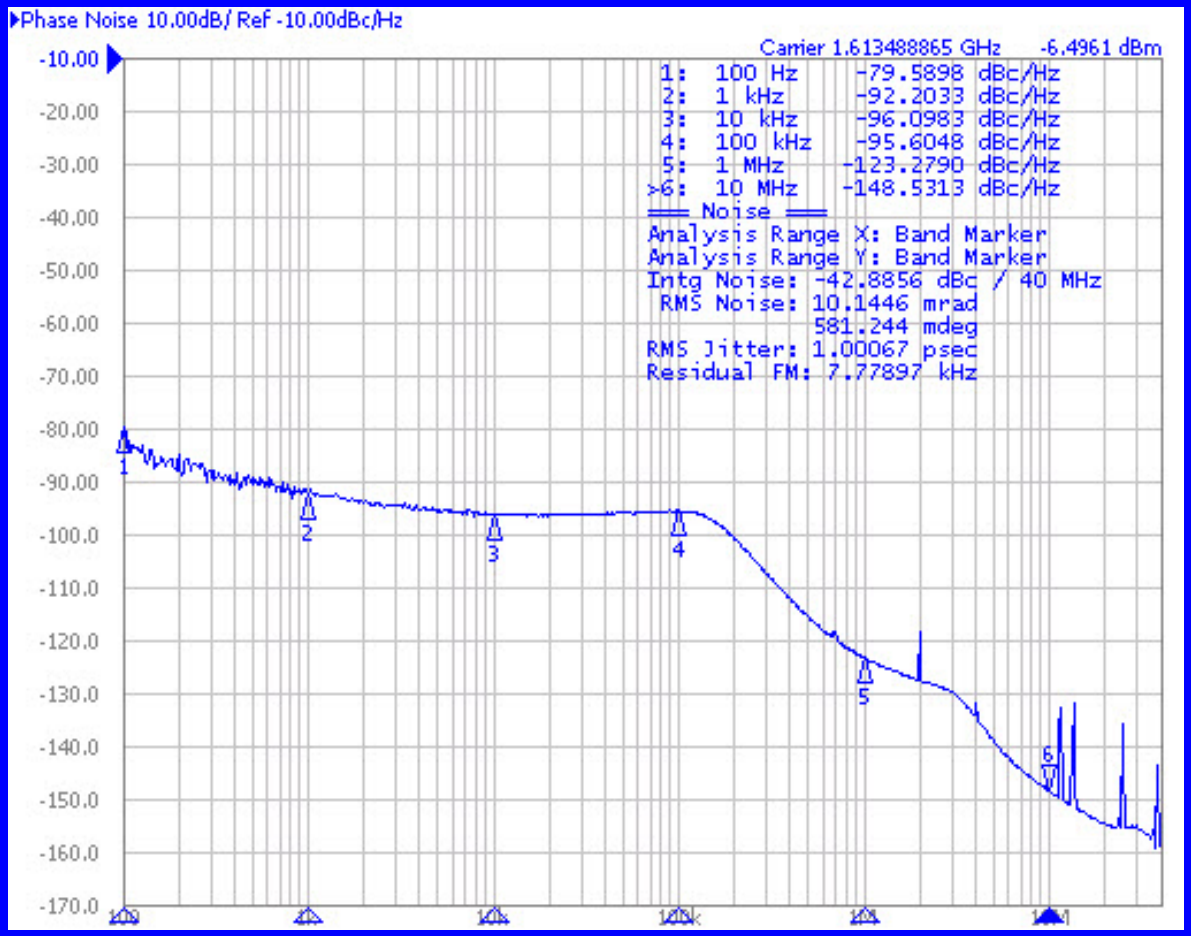
Measured Tuning Curves

- Tuning range: 1.2 ~ 2.1 GHz
- Coarse tuning: 8-bit control, 256 sub-bands

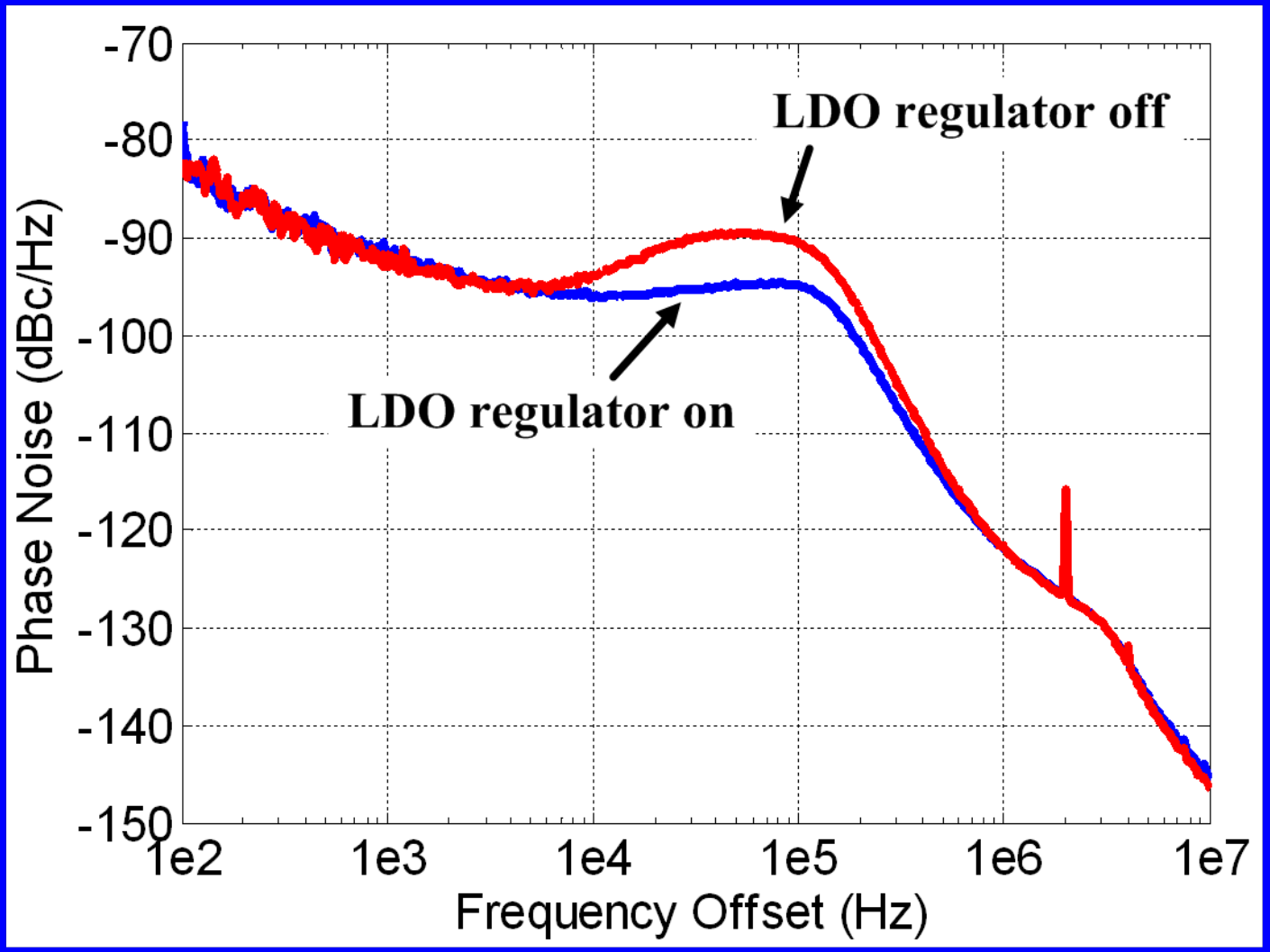


Measured Phase Noise

- **Typical fractional-*N* case: 1.6135 GHz**

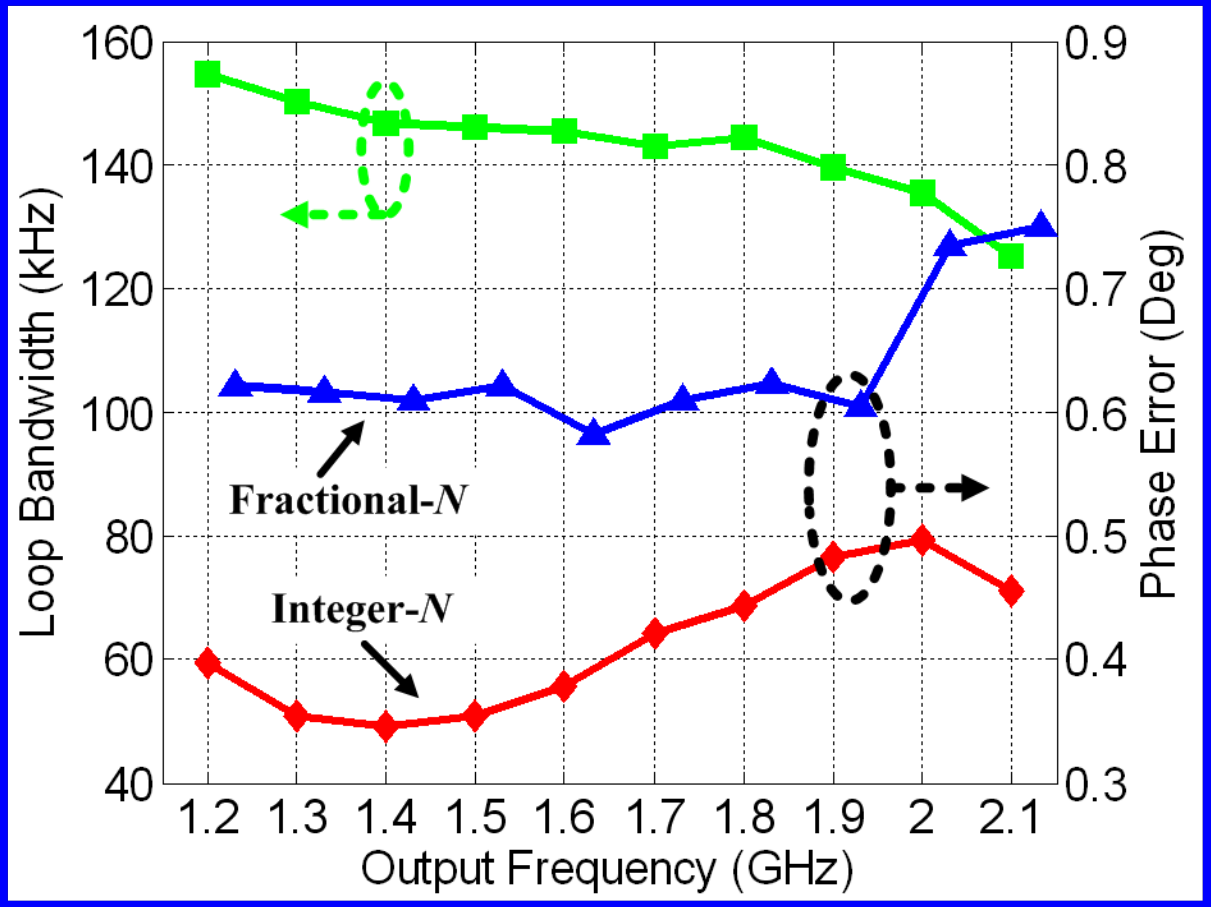


Phase Noise With and Without LDO



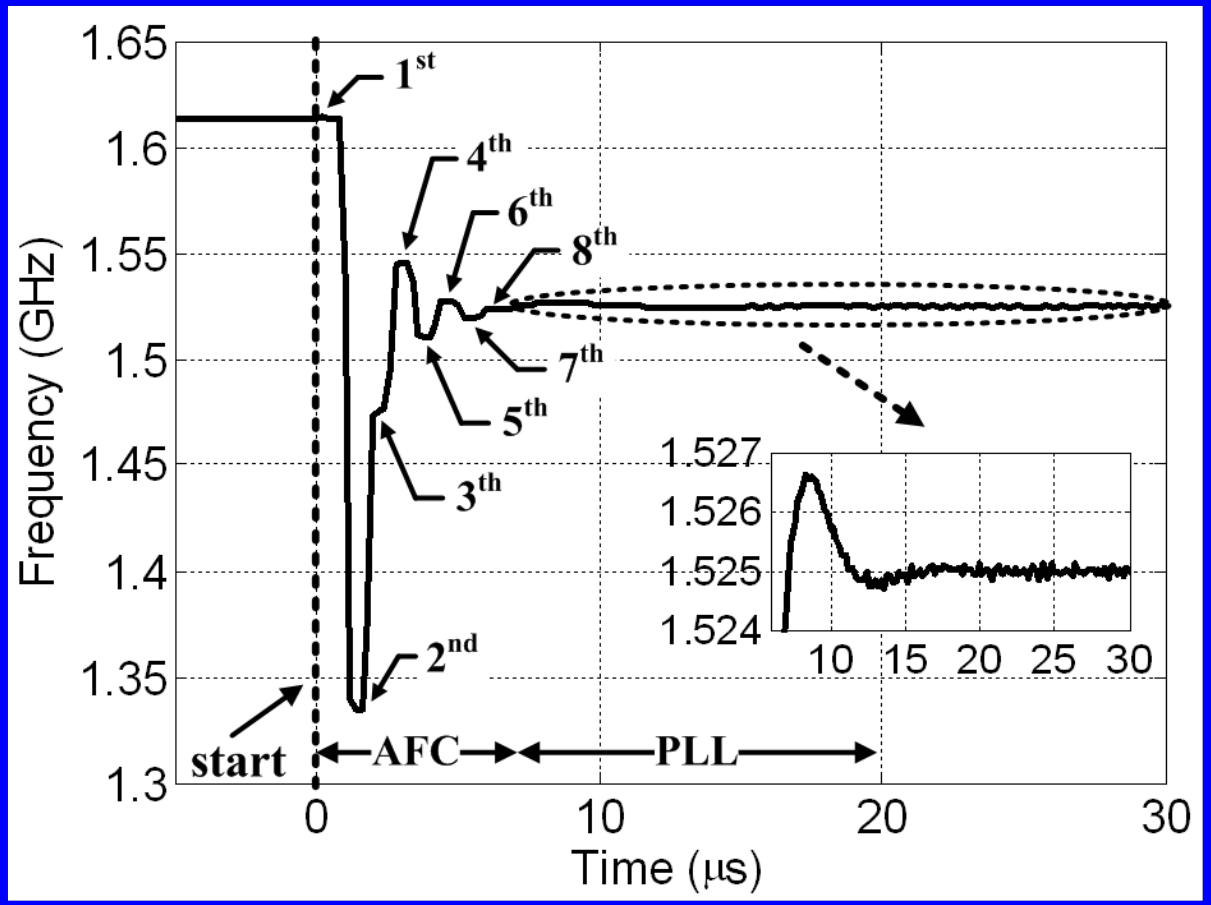
Loop Bandwidth and Phase Error

- **Phase error: Integrated from 100 Hz to 40 MHz**



Measured Locking Process

- Locking time: 20 μs (6.4 μs for AFC)



Performance Summary

Technology	0.18-μm CMOS	
Die Area	1.47 mm × 1 mm	
Supply Voltage	1.8 V (VCO with 1.5 V)	
Current	16 mA	
Ref. Clock	25 MHz	
Output Freq.	1.2 GHz ~ 2.1 GHz	
Phase Noise (dBc/Hz)	Integer-*N*	–100@10kHz
	Fractional-*N*	–96@10kHz
Phase Error	Integer-*N*	<0.5°$_{RMS}$
	Fractional-*N*	<0.75°$_{RMS}$
Locking Time	20 μs	

Conclusions

- Have proposed level shifters to ensure symmetrical tuning curves
- Have demonstrated high-PSR LDO regulator
- Have introduced voltage monitor to overcome frequency drift
- Have achieved superior phase noise and phase error performance across the whole wideband tuning range