A Sub-0.75°$_{RMS}$-Phase-Error Differentially-Tuned Fractional-*N* Synthesizer with On-Chip LDO Regulator and Analog-Enhanced AFC Technique

Lei Lu, Lingbu Meng, Liang Zou, Hao Min and Zhangwen Tang*
ASIC & System State Key Laboratory, Fudan University, Shanghai 201203, China

***Abstract*—This paper presents a low-phase-error wideband fractional-*N* frequency synthesizer. Differential tuning is described and a level shift circuit is proposed to obtain symmetrical tuning range. On-chip LDO regulator is designed to improve the power supply rejection for VCO. A voltage monitor is used to enhance the digital AFC technique to overcome the temperature variation. The synthesizer was implemented in a 0.18-µm CMOS process with a 16-mA supply current and a 1.47-mm^2 die area. The measured in-band phase noise is less than –97 dBc/Hz at a 10-kHz frequency offset and the integrated phase error is less than 0.75°$_{RMS}$. The measured reference spur is less than –71 dBc and the locking time is smaller than 20 µs.**

I. Introduction

Fractional-*N* frequency synthesizers with wide tuning range are essential for digital TV tuners. To meet the requirements of the tuners, synthesizer should also have low phase noise, low phase error, constant loop bandwidth as well as automatic frequency calibration (AFC) techniques [1].

For the synthesizer loops, either single-ended or differential architectures can be adopted. Fig. 1 shows the block diagram of a typical ΔΣ fractional-*N* frequency synthesizer. The differences in circuit blocks between single-ended and differential configurations are that differential charge pumps with common-mode feedback, two loop filters and differentially-uned VCOs are used in the latter. To obtain the same loop characteristics as the single-ended form, half the charge pump current I_{cp} should be assigned to each side in the differential form. Besides that, twice area of the loop filter and differentially-tuned varactors in LC VCO are needed. Compared with the single-ended form, the differential form has other advantages. The loop filter area can be reduced to a half when two big capacitors in series are combined into one. Differential tuning characteristics can suppress the common-mode noise from power supply, substrate and control lines. Differential charge pump can obtain better linearity, which may effectively avoid the degradation of in-band phase noise generated from quantization noise of ΔΣ modulator going through analog blocks with large nonlinearity.

To achieve a symmetrical tuning range in the differential form, the common-mode voltage of VCO outputs is sensed to decide the common-mode voltage of charge pump differential outputs [2]. However, non-symmetrical accumulation mode MOS varactors (A-MOS) are used. In addition, the common-mode voltage of charge pump outputs also varies, which may lead to current mismatch in most cases when common-mode voltage is not $V_{DD}/2$. This paper proposes a level shift circuit to acquire a symmetrical tuning range using symmetrical inversion mode MOS varactors (I-MOS). A low-noise high power-supply-rejection (PSR) low-dropout (LDO) regulator is designed to bias VCO power supply. Due to the temperature drift, the frequency variation may exceed 30 MHz for the multi-band VCO of this synthesizer, so a voltage monitor is adopted to guarantee the robustness of the AFC technique.

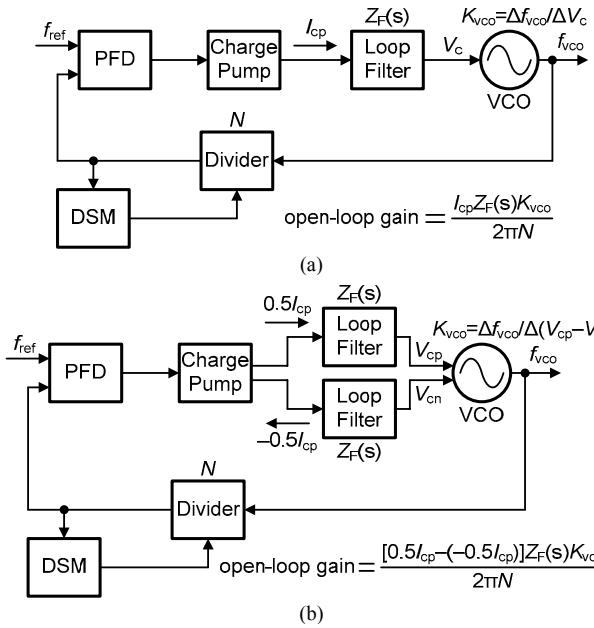

Fig. 1. Block diagram of a typical ΔΣ fractional-*N* frequency synthesizer. (a) Single-ended configuration. (b) Differentially-tuned configuration.

II. Synthesizer Architecture

The detail block diagram of the presented 1.2–2.1-GHz differentially-tuned ΔΣ fractional-*N* frequency synthesizer is shown in Fig. 2. The big capacitor C_1 is reduced to a half compared with the single-ended form and the loop filter is fully integrated. The phase-frequency detector (PFD) uses a conventional tri-state deadzone free circuit. The charge pump has rail-to-rail outputs and common-mode feedback with excellent current match. Level shift circuits are added before the control voltages of the VCO to compensate the difference between common-mode of charge pump outputs and VCO outputs as well as the threshold voltage of the I-MOS varactors.

* Corresponding author. Email: zwtang@fudan.edu.cn.

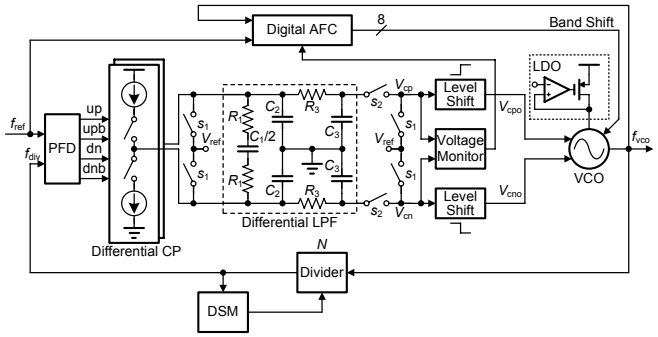

Fig. 2. Detail block-level diagram of the 1.2–2.1-GHz differentially tuned ΔΣ fractional-*N* frequency synthesizer with level shift of differential control voltages.

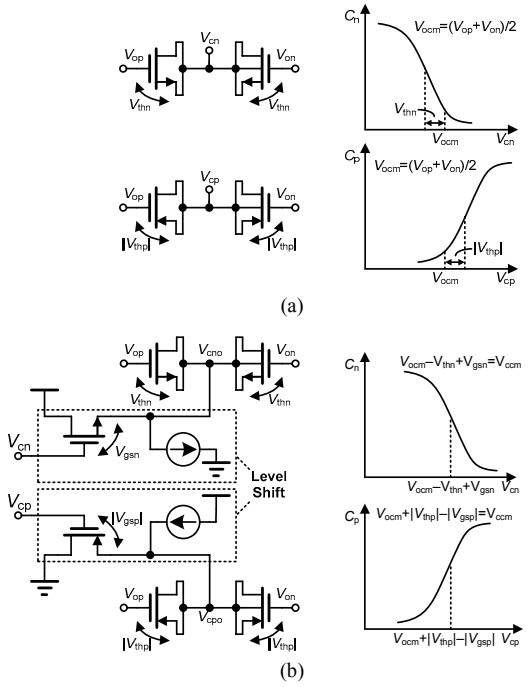

Fig. 3. *C–V* curves of I-MOS varactors. (a) Conversional circuit which has asymmetrical tuning curves. (b) Proposed method to obtain symmetrical tuning curves where $V_{ccm}=(V_{cp}+V_{cn})/2$.

Digital AFC counts the VCO clock directly and selects one of the 256 sub-bands of VCO whose center frequency is closest to the target frequency. After AFC finishes, a voltage monitor will always detect control voltages and ensure the robustness of the loop. Multi-modulus divider adopts programmed P/S counters and 4/4.5 prescaler to obtain the wide division ratio and reduce the quantization noise from ΔΣ modulator by 6 dB. Adaptive bandwidth control is used to obtain constant loop bandwidth across the whole frequency range [3].

III. Circuit Implementation

A. Level Shift

I-MOS varactors have p-type and n-type in process, so they are the best choice in differentially-tuned LC VCOs. Fig. 3 shows the *C–V* curves of *I*-MOS varactors. The point with

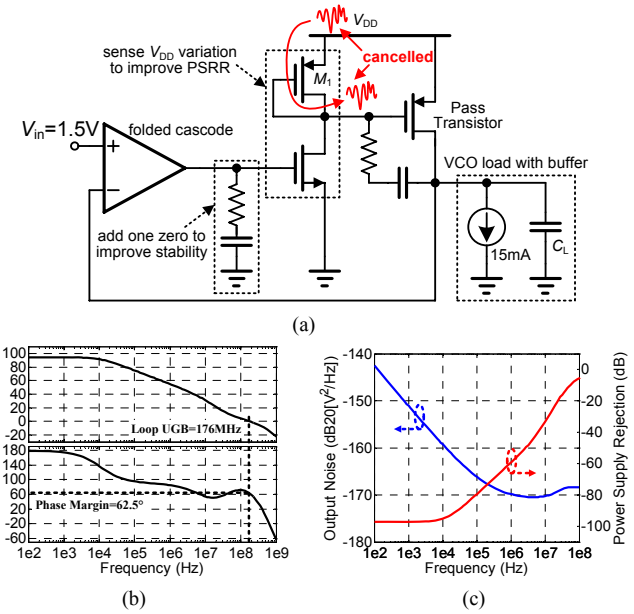

Fig. 4. Schematic of the low-noise high-PSR LDO regulator for VCO power supply. (a) Bode diagram. (b) Simulated output noise and power supply rejection.

maximal tuning gain in the tuning curve is the point with maximal slope in the *C–V* curve. A symmetrical tuning range means the point when V_{cp}–V_{cn}=0 has the maximal tuning gain. For A-MOS varactors, if the common-mode voltage V_{ocm} of VCO outputs is equal to the common-mode voltage V_{ccm} of control voltages, the tuning range could be symmetrical [2]. However, for I-MOS varactors, even if the two common-mode voltages are the same, the tuning range is still not symmetrical since V_{thn} and $|V_{thp}|$ do not have the same values.

To compensate both the common-mode difference and threshold voltage, level shift circuits are added before the control voltages directly connected to VCO. Control voltage V_{cn} goes through a voltage drop of V_{gsn} firstly, and then sees a threshold voltage rise to V_{ocm}. If after the two voltage level shifts, V_{cn} is equal to V_{ocm}, then the C–V curve shifts toward the right and becomes symmetrical. It is also like that for V_{cp}. Therefore, we can obtain V_{gsn} and $|V_{gsp}|$ as following

$$\begin{cases} V_{gsn} = V_{thn} + (V_{ccm} - V_{ocm}) \\ |V_{gsp}| = |V_{thp}| - (V_{ccm} - V_{ocm}) \end{cases}. \quad (1)$$

By adjusting the sizes of the level shift transistors with certain bias current, the gate-source voltage can be changed to meet the relationship in (1). The extra current consumption is very small compared to the VCO circuit. But the bias current can not be too small, since noise issues should be considered.

B. On-Chip LDO Regulator

On-chip LDO regulator for VCO should have low output noise and high PSR. The schematic of the regulator is shown in Fig. 4. Diode-connected transistor M_1 is inserted to sense the supply variation and conduct it to the gate of the pass transistor, thus the gate-source voltage can be constant due to

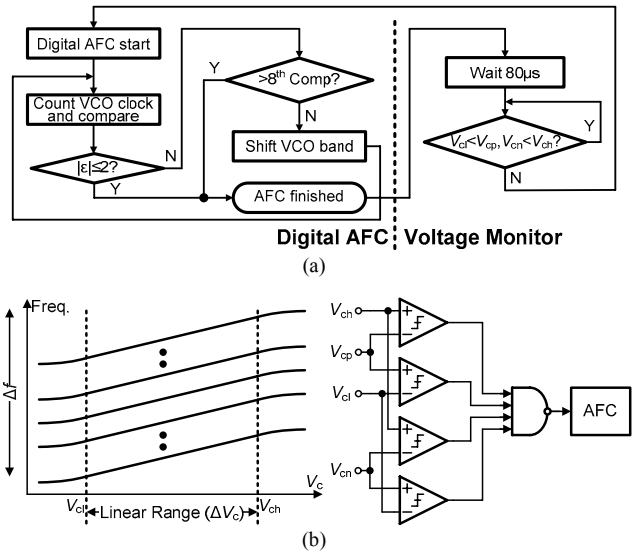

Fig. 5. Diagram of the analog-enhanced AFC technique. (a) Flow chart. (b) The voltage monitor to detect the control voltages.

the cancellation [4]. The RC connection after the folded-cascode amplifier is to introduce a zero within the GBW to improve the loop stability. The unit-gain bandwidth is 176 MHz and the phase margin is 62.5°. The input voltage 1.5 V is generated from a low noise bandgap output. The simulated output noise at 100 Hz frequency is less than –140 dB20[V^2/Hz] and reaches –170 dB20[V^2/Hz] at 1 MHz frequency. This will have no effect on VCO phase noise. The simulated PSR is –97 dB at DC, –80 dB at 100 kHz frequency and –60 dB at 1 MHz frequency. This will effectively suppress the noise from power supply lines.

C. Analog-Enhanced Digital AFC Technique

Division-ratio-based digital AFC technique is used to select the sub-band of VCO [3]. However, the temperature drift of 70℃ may lead to the oscillation frequency variation of 30 MHz, which exceeds the linear tuning range of one tuning curve. The analog-enhanced AFC technique is shown in Fig. 5. A voltage monitor including four comparators and one NAND gate is introduced to detect the differential control voltages. After 80 μs when AFC finishes, the voltage monitor starts working. 80 μs is to ensure the synthesizer has been locked. When the synthesizer looses lock due to the temperature drift, the control voltages exceed V_{ch} or V_{cl}, then NAND gate outputs "1" to restart digital AFC. This method is similar to [5], but different from that. This voltage monitor restarts AFC and does not adjust the sub-band directly. Because the AFC time is very short, restarting AFC can always ensure the operation of VCO closest to the center frequency of the sub-band with adding only a little more time.

IV. Experimental Results

The differentially-tuned ΔΣ fractional-*N* frequency synthesizer was implemented in a 0.18-μm CMOS process with a current consumption of 16 mA from a 1.8-V supply. The die micrograph is shown in Fig. 6. The die area is 1.47 mm^2, including loop filter and PADs.

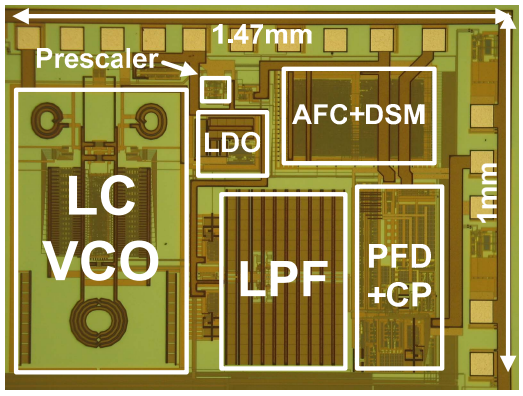

Fig. 6. Die micrograph.

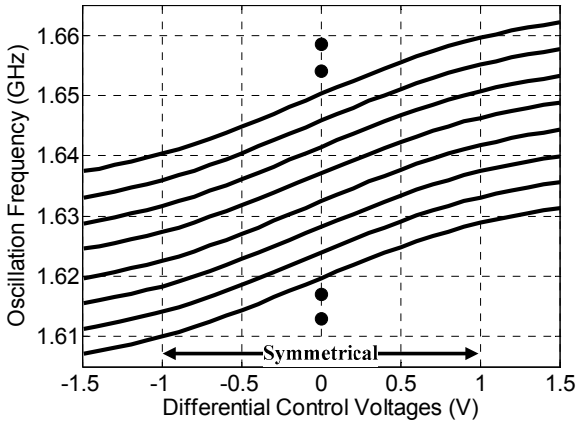

Fig. 7. Measured VCO tuning curves in part.

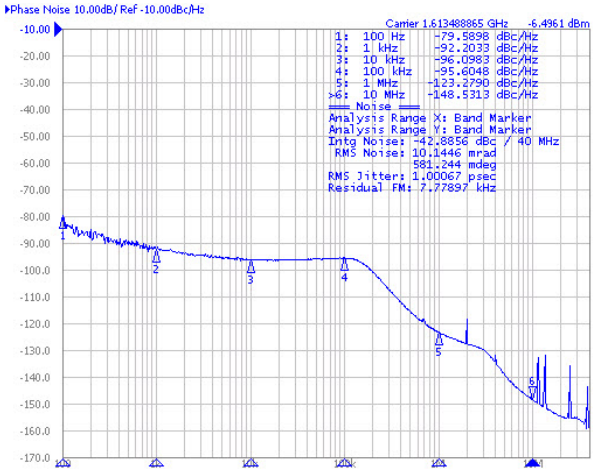

Fig. 8. Measured phase noise at the oscillation frequency of 1.6135GHz.

The measured tuning range is from 1.2 GHz to 2.1 GHz. Fig. 7 shows some measured VCO tuning curves. The measured fractional-*N* phase noise at the oscillation frequency of 1.6135 GHz is shown in Fig. 8. The in-band phase noise is less than –96 dBc/Hz and the out-of-band phase noise at a 1-MHz frequency offset is less than –123 dBc/Hz, which is

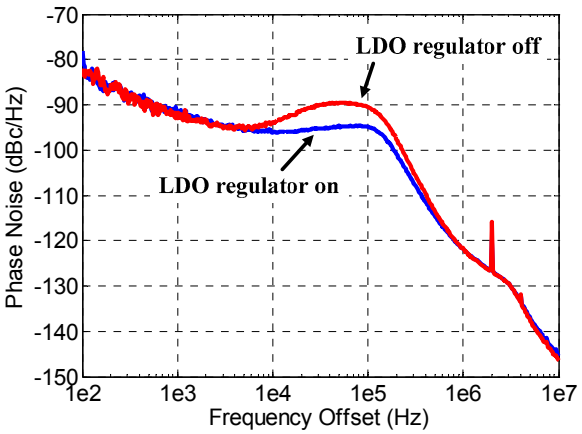

Fig. 9. Comparisons of measured phase noise with and without LDO regulator at the output frequency of 1813.5 MHz.

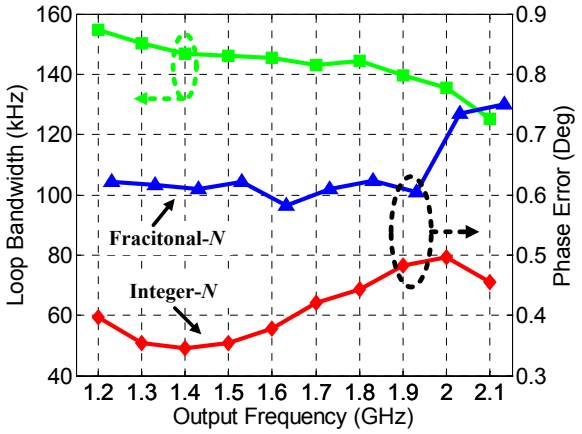

Fig. 10. Measured 3-dB closed-loop bandwidth and integrated RMS phase error from 100 Hz to 40 MHz in integer-*N* and fractional-*N* mode.

deteriorated by high-pass quantization noise of ΔΣ modulator. The measured phase noise with and without on-chip LDO is shown in Fig. 9. Compared with using on-chip LDO regulator, the phase noise is worsened by 5 dB at a 60-kHz frequency offset when using off-chip power supply.

Fig. 10 shows the measured loop bandwidth and integrated phase error. The measured loop bandwidth is from 125 kHz to 155 kHz with the variation less than 10.7%. The integrated phase error from 100 Hz to 40 MHz is less than 0.75°$_{RMS}$ in fractional-*N* mode and less than 0.5°$_{RMS}$ in integer-*N* mode. The measured reference spur at 25 MHz frequency offset is less than –71 dBc across the whole frequency range. The locking time is shown in Fig. 11. The total locking time is less than 20 μs, with 6.4 μs for AFC time. Table I shows a performance summary of the measured results.

V. Conclusion

A 1.2–2.1-GHz differentially-tuned ΔΣ fractional-*N* frequency synthesizer was implemented in a 0.18-μm CMOS process. Level shift circuits are proposed to obtain symmetrical tuning range. On-chip LDO regulators are employed to effectively suppress the noise from off-chip

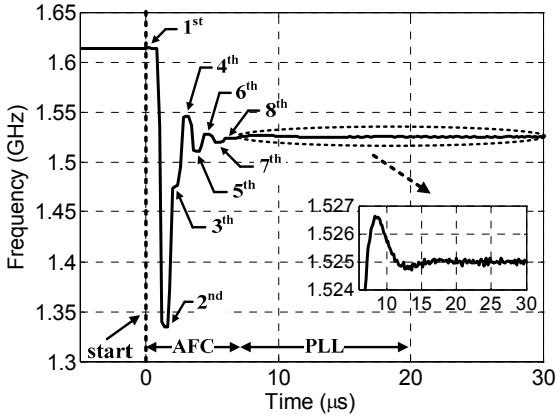

Fig. 11. Measured total locking time with AFC time of 6.4 μs.

Table I. Performance Summary

Technology	0.18-μm CMOS	
Die Area	1.47 mm^2	
Supply Voltage	1.8 V (VCO with 1.5 V)	
Current	16 mA	
Reference Clock	25 MHz	
Output Frequency	1.2 GHz ~ 2.1 GHz	
Phase Noise (dBc/Hz)	Integer-*N*	–100 @ 10 kHz; –127 @ 1MHz
	Fractional-*N*	–96 @ 10 kHz; –123 @ 1MHz
Phase Error (100 Hz ~ 40 MHz)	Integer-*N*	< 0.5°$_{RMS}$
	Fractional-*N*	< 0.75°$_{RMS}$
Reference Spur	< -71 dBc	
Locking Time	20 μs	

power supply. A voltage monitor is introduced to detect control voltages to guarantee the robustness of the digital AFC technique. The measured integrated phase error is less than 0.75°$_{RMS}$ and the in-band phase noise is less than –96 dBc/Hz in fractional-*N* mode. The measured reference spur is less than –71 dBc and the locking time is less than 20 μs. The chip consumes a 16-mA current with a die area of 1.47 mm^2.

Acknowledgment

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References

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