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A CMOS Wide-Band Low-Noise Amplifier With Balun-Based Noise-Canceling Technique

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***Abstract*— A differential high linearity low-noise amplifier (LNA) based on a capacitor-cross-coupled topology is presented in this paper. An off-chip balun is used for providing DC-bias and canceling the channel thermal noise of the transconductance MOS transistors. The LNA uses NMOS load and provides an extra signal feed-forward and noise-canceling path. Analysis shows that the noise contribution of the transconductance MOST is only $\gamma/20$ and the noise figure (NF) of the proposed LNA is $1+0.2\gamma$. The chip is implemented in a 0.18-μm MMRF CMOS process. Measured results show that in 50M-860MHz frequency range, the LNA achieved 15 dB gain, 2.5 dB NF, 8.3 dBm IIP3 and consumes only 4 mA current from a 1.8-V supply.**

I. Introduction

The world-wide spread of high-definition digital television (HDTV) promotes the research of the RF tuners and their building blocks. Among all the DTV standards, the Digital Video Broadcasting for Cable (DVB-C, 50M-860MHz) is regarded as the most difficult one for single-chip integration because of its low center-frequency and high bandwidth-to-center-frequency ratio (BW/f_c).

The low-noise amplifier (LNA) design is a challenge in CMOS tuners. Besides the basic requirements on gain and noise figure (NF), it needs to be fully differential to obtain high common-mode restrain ratio (CMRR) and high even-order harmonic restrain ability (IIP2). The fully differential capacitor-cross-coupled (CCC) topology [1] is a good candidate for its high linearity and low power dissipation. However, it suffers from high NF. The LNA exploiting a noise-canceling technique [2] achieves very low NF over wide frequency band but consumes too much power, e.g., for a differential topology, the total current is greater than 20 mA [3].

Fig. 1 shows a double-conversion low-IF (DLIF) DVB-C tuner RF architecture. An off-chip balun is used to transform the single-ended signal received by the antenna to balanced one for the differential-input LNA. In the traditional LNA design, the balun is AC-coupled to the tuner chip and acts only as a single-ended to differential (S-D) transformer. In this paper, the balun and the LNA are DC-coupled, and a balun-based noise-canceling technique is proposed. Analysis shows that the proposed balun+LNA topology achieves the lowest NF in all published CCC LNAs, and maintains the inherent advantage of high linearity and low power.

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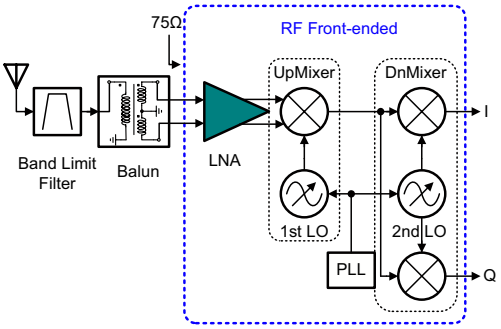


Fig. 1. A DZIF tuner architecture.

This paper is organized as follows: the balun+LNA topology and the balun-based noise-canceling technique are introduced in Section II. The balun impedance analysis and NF calculation are given in Section III. The chip implementation and measurement results are given in Section IV, and Section V concludes this work.

II. CCC LNA With Off-Chip Balun

A traditional wide-band CCC common-gate (CG) LNA is shown in Fig. 2. The differential signal from the off-chip balun is AC-coupled to the source of the transconductance MOS transistors, and then cross-coupled to the gate of the opposite MOSTs through coupling capacitor $C_{1,2}$, therefore the effective transconductor is doubled without consuming extra current. The source resistor $R_{S1,2}$ (or current mirror) provides the DC-bias. Only considering the channel thermal noise of the transconductance MOSTs and assuming input impedance is matched, the minimum NF of this LNA is [1]

$$F = 1 + \gamma/2 \tag{1}$$

Comparing to the basic CG topology without $C_{1,2}$ whose NF is $1+\gamma$, the noise contribution of $M_{1,2}$ is half reduced. This can be explained in the noise-canceling point of view: The channel thermal noise i_n flows through the small signal impedance at OP and IP, causes two noise voltage $v_{n,op}$ and $v_{n,ip}$ with opposite sign. Then $v_{n,ip}$ is coupled to the gate of M_2 by C_1-R_1 and amplified by the CS stage M_2 to $v_{n,on}$. The inphase noise $v_{n,on}$ and $v_{n,op}$ reduced the output differential mode noise voltage and thus reduced the NF. However, the

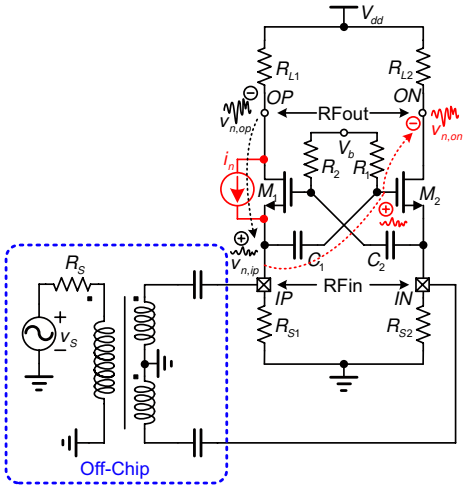


Fig. 2. Traditional CCC LNA.

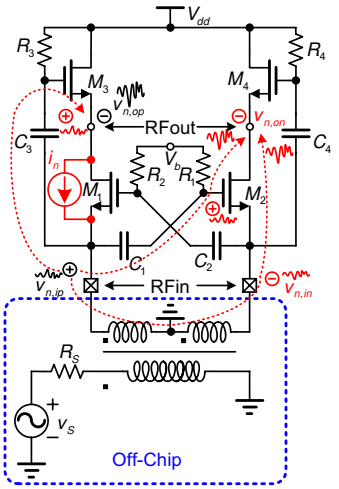


Fig. 3. Proposed LNA schematic.

actual NF of Fig. 2 is still higher than 3 dB for a typical $\gamma = 4/3$ because of the noise contribution of $R_{S1,2}$ and $R_{L1,2}$. The other drawback is that $R_{S1,2}$ reduced the voltage headroom and therefore reduced the linearity.

A DC-coupled balun+LNA topology is proposed to overcome these problems, as shown in Fig. 3. The two balanced ports of a transformer-type balun are directly connected to the source of M_1 and M_2 respectively, with the center-tapped port grounded providing DC-bias for the LNA. The first advantage of this topology is that the source resistor $R_{S1,2}$ and the off-chip AC-coupled capacitors can be removed, while the S-D transform function still remains. The load resistor $R_{L1,2}$ is replaced by NMOST $M_{3,4}$ for two reasons: 1) The linearity can be improved due to a "post-correction" approach [4]; 2) NMOS loading with extra AC paths C_3-R_3 and C_4-R_4 can improve the voltage gain and provide an extra noise-canceling path [5]. From Fig. 3, it can be shown that there are now three noise-canceling paths (in dot lines) which are:

1) The CCC path C_1-R_1 and CS stage M_2. $v_{n,ip}$ is AC-coupled to the gate of M_2 by C_1-R_1, and then amplified to $v_{n,on}$ by CS stage M_2.

2) The balanced ports of the balun and CG stage M_2. $v_{n,ip}$ is transformer-coupled to $v_{n,in}$ by the balun, and then amplified to $v_{n,on}$ by CG stage M_2.

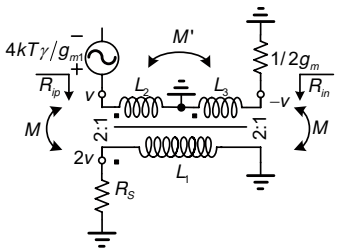
3) The extra feed-forward path C_3-R_3 and source follow stage M_3. $v_{n,ip}$ is AC-coupled to the gate of M_3 by C_3-R_3, and then followed to $v_{n,op}$ by source follow stage M_3.

With these noise-canceling paths, the output differential-mode noise of $M_{1,2}$ is remarkable reduced, therefore the NF can be very low.

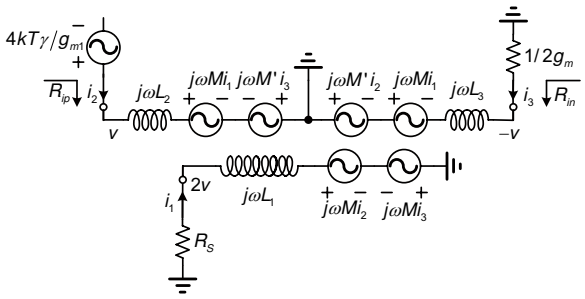
III. Parameter Calculation

In this design, we choose a balun with the impedance ratio 1:1. The differential input impedance of the LNA is $1/g_m$, so the input impedance matching condition is

$$g_m = 1/R_S \tag{2}$$



(a)



(b)

Fig. 4. A 1:1 balun model. (a) Original model. (b) De-coupled equivalent circuit.

The voltage gain is

$$A_V = 1 + 2g_{m1}/g_{m3} \tag{3}$$

where the term "1" comes from the feed-forward paths C_3-R_3-M_3 and C_4-R_4-M_4.

In order to calculate the noise contribution of M_1, the balun impedance characteristic should be analyzed firstly.

A. Balun Model

When the noise voltage of M_1 adds to one of the balanced ports, the balun model can be shown in Fig. 4(a). For the 1:1 balun, the coil ratio is 2:1 and three inductors $L_1 \sim L_3$ satisfy

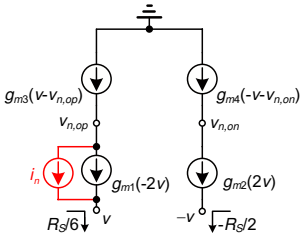


Fig. 5. Small signal circuit for NF calculation.

$L_1 = 4L_2 = 4L_3$. Then the voltage ratio of three ports is $2v : v : (-v)$. Under conservation of energy it has

$$\frac{v^2}{R_{ip}} = \frac{(2v)^2}{R_S} + \frac{(-v)^2}{1/2g_m} \tag{4}$$

So that

$$R_{ip} = \frac{1}{4/R_S + 2g_m} = \frac{R_S}{6} \tag{5}$$

Assuming $L_1 \sim L_3$ are fully coupled, i.e., coupling coefficient of each two inductors is $k = 1$. The mutual inductance of which are $M = \sqrt{L_1 L_2} = \sqrt{L_1 L_3} = 2L_2$ and $M' = \sqrt{L_2 L3} = L_2$. We can obtain the de-coupled balun model in Fig. 4(b), and three current loop formulas are

$$\begin{cases} j\omega L_1 i_1 + j\omega M i_2 - j\omega M i_3 = 2v \\ j\omega M i_1 + j\omega L_2 i_2 - j\omega M' i_3 = v \\ -j\omega M i_1 - j\omega M' i_2 + j\omega L_3 i_3 = -v \end{cases} \tag{6}$$

Substituting $i_1 = -2v/R_S$ and assuming $L_1 \sim L_3$ to be infinite (comparing with R_S) yields

$$i_2 - i_3 = 4v/R_S \tag{7}$$

From (5) and (7) it can be calculated that

$$R_{in} = -v/i_3 = -R_S/2 \tag{8}$$

B. NF Calculation

From the small signal circuit as shown in Fig. 5, the noise contribution of $M_{1,2}$ can be calculated as

$$\overline{v_{n,M1,2}^2} = (v_{n,op} - v_{n,on})^2 = \left(\frac{R_S}{4} - \frac{1}{2g_{m3}}\right)^2 4kT\gamma g_{m1} \tag{9}$$

And the noise contribution of $M_{3,4}$ is

$$\overline{v_{n,M3,4}^2} = 4kT\gamma/g_{m3} \tag{10}$$

So the NF of the total circuit is

$$F = 1 + \frac{2 \cdot \overline{v_{n,M1,2}^2} + 2 \cdot \overline{v_{n,M3,4}^2}}{A_V^2 \cdot 4kTR_S} \tag{11}$$

Considering the input impedance matching condition (2), and substituting $g_{m3} = g_{m1}/2$ for 14 dB gain, the NF is

$$F_{min} = 1 + \frac{9}{200}\gamma + \frac{4}{25}\gamma \approx 1 + 0.2\gamma \tag{12}$$

It can be seen that the noise contribution of the transconductance MOST $M_{1,2}$ is less than $\gamma/20$ and is no longer the dominant noise source. For $\gamma = 4/3$, the minimum NF is about 1 dB.

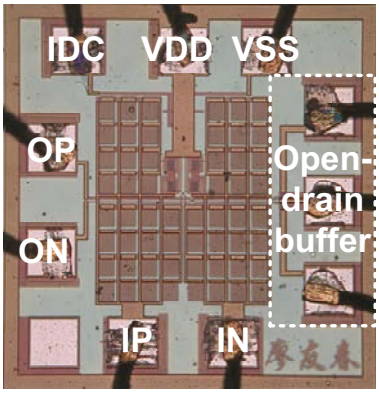


Fig. 6. Microphotograph of the chip.

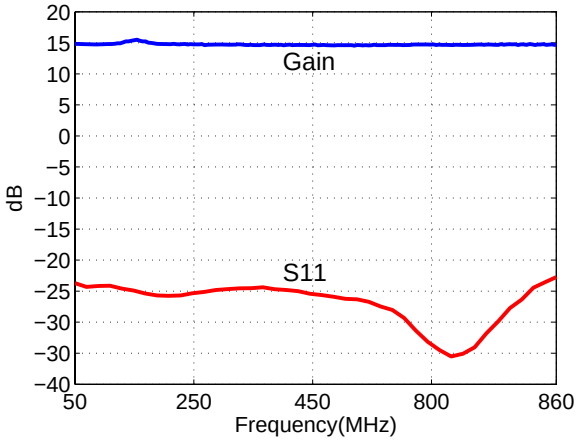


Fig. 7. Measured gain and $S11$.

IV. Chip Implementation and Measurement

The LNA chip is implemented in a 0.18-μm, 1P6M MMRF CMOS process, the chip microphotograph is shown in Fig. 6. The MIM capacitor is available for coupling capacitors $C_1 \sim C_4$. The core size of the LNA is $0.25 \times 0.3\text{mm}^2$ and the total chip size including the PADs and ESD MOSTs is $0.52 \times 0.54\text{mm}^2$. The chip consumes only 4 mA current from a 1.8-V supply.

The differential outputs are both directly connected and after an open drain NMOS pairs for measurement purpose. The former are combined to single-ended by an off-chip 1:4 balun for NF and linearity measurement while the latter are connected to two 50 Ω resistors and combined to a 1:2 balun for gain measurement.

The measured gain has a flat value of 15 dB and the $S11$ (referred to 75 Ω characteristic impedance) is below -24 dB during the 50M-860MHz frequency range, as shown in Fig. 7. The simulated and measured NFs are shown in Fig. 8. The measured NF is 2.2∼2.9 dB with an average value 2.5 dB, which is very close to the simulated value 2.3 dB. The measured input-referred third-order intercept point (IIP3) is shown in Fig. 9 with a value of 8.3 dBm at two-tone frequency

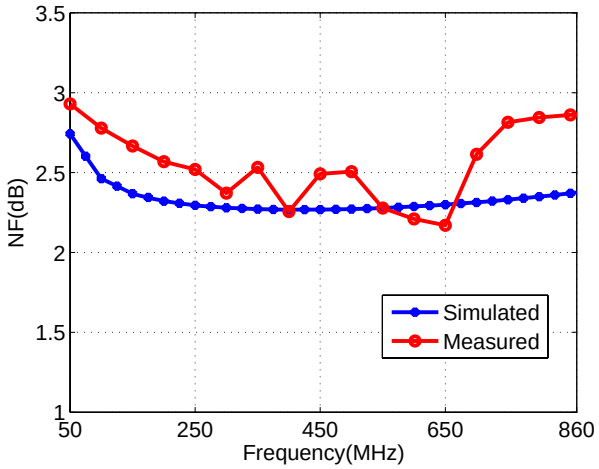


Fig. 8. Simulated and measured NF.

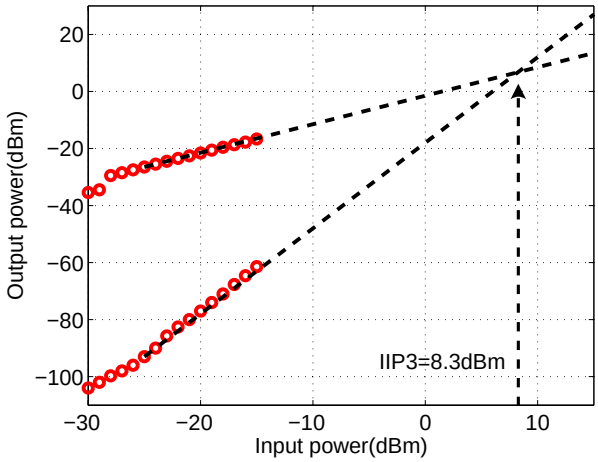


Fig. 9. Measured IIP3.

TABLE I
SUMMARY OF MEASUREMENT RESULTS AND PERFORMANCE COMPARISON

	[3]	[7]	[8]	[9]	This Work
CMOS Process	0.12-μm	0.18-μm	0.18-μm	0.18-μm	0.18-μm
Frequency	48-862MHz	470-860MHz	470-870MHz	1.2-11.9GHz	50-860MHz
Gain	17dB	10dB	16dB	9.7dB	15dB
S_{11}	N/A	N/A	-11dB	-11dB	-24dB
NF	3dB	5.7dB	4.3dB	4.8dB	2.5dB
IIP3	5.5dBm	10dBm	-1.5dBm	-6.2dBm	8.3dBm
Power	23mA×2.5V	5.2mA×1.8V	12mA×1.8V	11mA×1.8V	4mA×1.8V
FOM	0.79	0.73	0.072	0.03	12.08

500M & 502MHz. The 1st and 3rd order power are both attenuated by the output balun while the IIP3 value is same to the simulated result.

A figure of merit (FOM) is used to compare recent wide-band LNAs with this work, which is given by [6]

$$\text{FOM} = \frac{\text{Gain} \cdot \text{IIP3}}{P_{dc} \cdot (F-1)} \cdot \frac{\text{BW}}{f_c} \tag{13}$$

where the gain and F are in absolute values, IIP3 and P_{dc} are in milliwatts, and the bandwidth is replaced by BW/f_c. Summary of the measured results and performance comparison are shown in Table I. The proposed LNA shows a highest FOM in all published works.

V. CONCLUSION

In this paper, a differential capacitor-cross-coupled LNA with a balun-based noise-canceling technique is proposed. Analysis shows that the noise contribution of the transconductance MOST can be greatly reduced with three noise-canceling paths. Measured results shows that the proposed LNA achieves low NF, high linearity and consumes low power during the 50M-860MHz frequency bandwidth.

REFERENCES

[1] W. Zhuo, S. Embabi, J. Pineda de Gyvez, and E. Sanchez-Sinencio, "Using Capacitive Cross-Coupling Technique In RF Low Noise Amplifiers and Down-Conversion Mixer Design," in *Proc. 26th Eur. Solid-State Circuits Conf.*, pp.116-119, Sep. 2000.

[2] Youchun Liao, Zhangwen Tang, and Hao Min, "A Wide-band CMOS Low-Noise Amplifier for TV Tuner Application," in *Proc. of Asian Solid-State Circuit Conf. (A-SSCC)*, Nov. 2006, Hangzhou, China.

[3] D. Saias, et al., "A 0.12m CMOS DVB-T Tuner", in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2005, pp. 430-431.

[4] B. Razavi, *Design of Analog CMOS Integrated Circuits*, U.S.:McGraw-Hill, 2001.

[5] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Generating All 2-MOS Transistors Amplifiers Leads To New Wide-Band LNAs," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1032-1040, July 2001.

[6] A. Amer, E. Hegazi, and H. Ragai, "A Low-Power Wideband CMOS LNA for WiMAX", *IEEE Tran. on Circuit and Systems-II: Express Briefs*, vol. 54, pp. 4-8, Jan. 2007.

[7] T. W. Kim and B. Kim, "A 13-dB IIP3 Improved Low-Power CMOS RF Programmable Gain Amplifier Using Differential Circuit Transconductance Linearization For Various Terrestrial Mobile D-TV Applications," *IEEE J. Solid-State Circuits*, vol. 41, pp. 945-953, Apr. 2006.

[8] Jianghong Xiao, I. Mehr, and Jose Silva-Martinez, "A High Dynamic Range CMOS Variable Gain Amplifier for Mobile DTV Tuner", *IEEE J. Solid-State Circuits*, vol. 42, pp. 292-301, Feb. 2007.

[9] Chih-Fan Liao, and Shen-Iuan Liu, "A Broadband Noise-Canceling CMOS LNA for 3.1-10.6-GHz UWB Receivers", *IEEE J. Solid-State Circuits*, vol. 42, pp. 329-339, Feb. 2007.