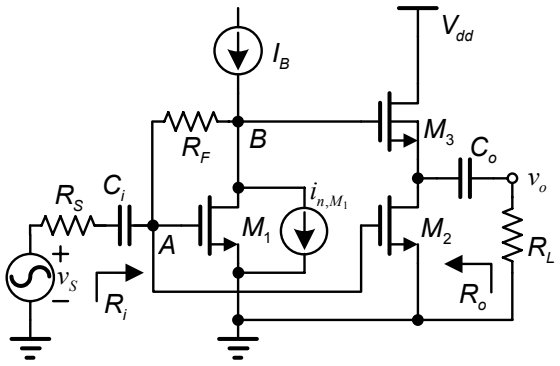


Fig. 2. Topology of a LNA exploiting noise-canceling technique.

teristics, gain greater than 12 dB, NF less than 4 dB and IIP3 greater than 3 dBm within 50-860 MHz frequency range.

III. Parameter Analysis and Circuit Design

A. Noise-canceling Under Input/output Impedance Matching

The LNA exploiting a noise-canceling technique [2] is shown in Fig. 2. The primary purpose of this circuit is to eliminate the noise contribution of M_1 channel thermal-noise $i_{n,M1}$, which is a dominating noise source. It flowing through R_F and R_S causes two instantaneous noise voltages at nodes B and A with the same phase. Then the voltage of node A is amplified by a common-source stage M_2 and node B is followed by a source-follow stage M_3. Consequently, the thermal noise of M_1 could be counteracted at the output due to the opposite voltage gain sign of M_2 and M_3.

The input and output impedances can be calculated as $R_i = 1/g_{m1}$ and $R_o = 1/g_{m3}$, respectively. And the load impedance is $R_L = R_S = 50\,\Omega$. Then the impedance matching condition is

$$g_{m1} = g_{m3} = 1/R_S \tag{1}$$

Considering the influence of load impedance R_L, the noise-canceling condition is

$$g_{m2} = (1 + R_F/R_S)/R_S \tag{2}$$

where R_F is the feedback resistor. Thus, under the impedance matching and noise-canceling condition, the voltage gain from node A to output is

$$A_V = v_o/v_A = -R_F/R_S \tag{3}$$

According to [4] , the noise figure (or noise factor) can be represented as

$$NF = 1 + \frac{\overline{v_{n,M1}^2} + \overline{v_{n,RF}^2} + \overline{v_{n,M2,M3}^2} + \overline{v_{n,RL}^2}}{A_V^2 \cdot 4kTR_S} \tag{4}$$

where $\overline{v_{n,M1}^2}$, $\overline{v_{n,RF}^2}$, $\overline{v_{n,M2,M3}^2}$ and $\overline{v_{n,RL}^2}$ are the noise contributions at the output of M_1, R_F, M_2-M_3 and R_L, respectively. Substituted with their expressions under the noise-canceling condition, (4) can be calculated as

$$\begin{aligned} NF &= 1 + \frac{R_F + \gamma(2R_S + R_F)/4 + R_L}{(R_F/R_S)^2 R_S} \\ &= 1 + \frac{R_S}{R_F} + \frac{\gamma}{4}\frac{R_S}{R_F}\left(\frac{2R_S}{R_F} + 1\right) + \left(\frac{R_S}{R_F}\right)^2 \end{aligned} \tag{5}$$

where γ is a parameter greater than 1 for submicron MOSFET.

B. Linearity Analysis

Considering only the first-order deviation of the transconductance from the square law and weakly nonlinear condition, the drain current of M_1 and M_2 can be given by

$$i_{d1} = g_{1,1}v_A + g_{1,2}v_A^2 + g_{1,3}v_A^3 \tag{6}$$

$$\begin{aligned} i_{d2} &= g_{2,1}v_A + g_{2,2}v_A^2 + g_{2,3}v_A^3 \\ &= n\left(g_{1,1}v_A + g_{1,2}v_A^2 + g_{1,3}v_A^3\right) \end{aligned} \tag{7}$$

where $g_{i,j}$ means the j^{th}-order distortion of the transconductance of MOSFET M_i (for $i = 1, 2$ and $j = 1, 2, 3$), and $n = g_{2,j}/g_{1,j} = 1 + R_F/R_S$. The voltage of node B can be calculated by small-signal analysis as

$$v_B = (1 - g_{1,1}R_F)v_A - g_{1,2}R_F v_A^2 - g_{1,3}R_F v_A^3 \tag{8}$$

Then the input IP3 of the first stage is

$$A_{IP3,fs} = \sqrt{\frac{4}{3}\left|\frac{1 - g_{1,1}R_F}{g_{1,3}R_F}\right|} = \sqrt{\frac{4}{3}\left|\frac{g_{1,1}}{g_{1,3}} - \frac{1}{g_{1,3}R_F}\right|} \tag{9}$$

Here, the first term is the non-linearity contribution of the common-source topology M_1 and the latter is that of the feedback resistor R_F. Normally $g_{1,3} < 0$ when M_1 is in saturation region, therefore the IP3 of the first stage is decreased due to R_F.

The third-order distortion of M_3 can be ignored owing to the over-driven voltage of M_3 is quite large ($V_{GS3} > 1$V). Therefore, the voltage at the output can be written as

$$\begin{aligned} v_o = &-\left[(ng_{1,1}R_S + g_{1,1}R_F - 1)v_A + g_{1,2}(nR_S + R_F)v_A^2\right. \\ &\left.+ g_{1,3}(nR_S + R_F)v_A^3\right]/2 \end{aligned} \tag{10}$$

And the input IP3 of the total circuit is

$$\begin{aligned} A_{IP3,total} &= \sqrt{\frac{4}{3}\left|\frac{ng_{1,1}R_S + g_{1,1}R_F - 1}{g_{1,3}(nR_S + R_F)}\right|} \\ &= \sqrt{\frac{4}{3}\left|\frac{g_{1,1}}{g_{1,3}} - \frac{1}{g_{1,3}(R_S + 2R_F)}\right|} \end{aligned} \tag{11}$$

From (3), (5) and (11), it can be seen that A_V, NF and IP3 are only depended on the feedback resistor R_F. High gain, low noise figure and high linearity can be achieved simultaneously when R_F is large enough. However, a large R_F needs a large g_{m2} to meet the noise-canceling condition (2), and this would lead much greater power consumption. The relationships of A_V, NF, IIP3, Idd (total current) versus the feedback resistor R_F are shown in Fig. 3.

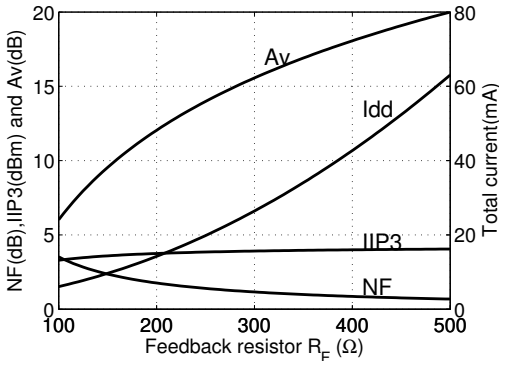


Fig. 3. Relationship of Av, NF, IIP, Idd vs. R_F.

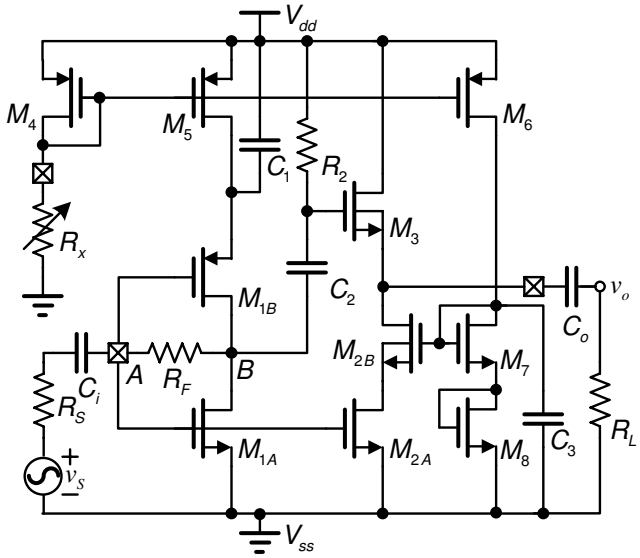
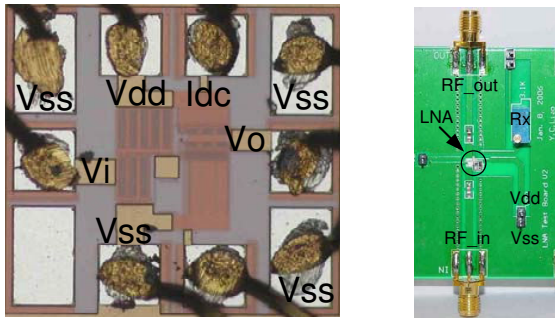


Fig. 4. Schematic of the designed noise-canceling LNA.

C. LNA Design

Figure 4 is the schematic of a noise-canceling LNA. A PMOS M_{1B} is exploited to increase the transconductance of input stage via a current-reuse technique. And a capacitor C_1 is used to reduce the influence of power supply fluctuating and to filter out the noise from current-mirror M_4-M_5. The second stage is AC-coupled to the first stage via a high-pass topology C_2-R_2. A cascode transistor M_{2B} is used to increase the inverse isolation (S_{12}). Its DC bias voltage is provided by the branch M_6-M_8. And C_3 is used to filter out the noise from this branch. M_3 and M_{2B} are deep n-well NMOS devices, whose substrates are connected to each source to eliminate body effect.

It is easy to obtain the devices parameters from the previous analysis. The transconductances of M_1 and M_3 are determined by the impedance matching condition (1), which is $g_{m1A} + g_{m1B} = g_{m3} = 0.02\,S$. The feedback resistor R_F is chosen to be 400 Ω considering the trade-offs between the gain, noise figure, linearity and power consumption. The transconductance



(a) (b)

Fig. 5. Photograph of (a) Chip (b) PCB.

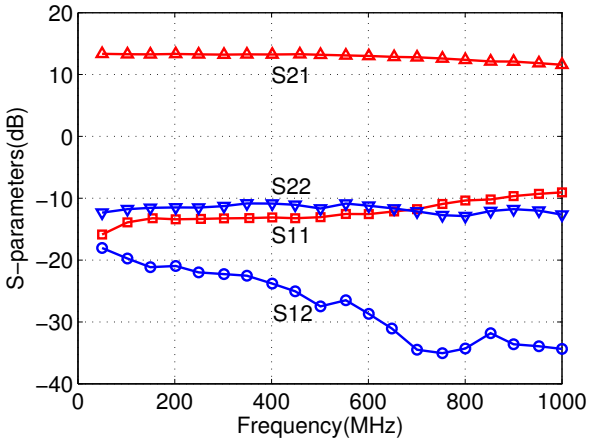


Fig. 6. Measured S-parameters.

of M_2 can be calculated from the noise-canceling condition (2), which is $g_{m2} = g_{m3}(1 + R_F/R_S) = 0.18\,S$. However, for the power dissipation restriction, g_{m2} is actually chosen to be 0.08 S in this design. Consequently, the voltage gain will decrease and the NF will deteriorate due to the deviation of the noise-canceling condition.

IV. Chip Implementation and Measurement

The chip is implemented in a 0.25-μm RF CMOS process. Figure 5 is the photograph of the chip and test PCB. The core size is only 0.15mm×0.18mm. And it draws 12 mA from a 2.5-V power supply. The ground V_{SS} is connected via four bonding-wires to reduce the parasitic inductance.

The measured S-parameters are shown in Fig. 6. In the frequency range of 50 MHz–1 GHz, the S_{21} (voltage gain) is about 13.4 dB with a 3-dB bandwidth of 1 MHz–1.3 GHz, the input matching S_{11} is from –16 dB to –9 dB, the output matching S_{22} is below –10 dB, and the inverse isolation S_{12} is less than –19 dB.

The simulated and measured NF are shown in Fig. 7. The measured NF is less than 3.5 dB from 50 MHz to 1 GHz, with a minimum NF of 2.4 dB at 350 MHz. The NF increases at low frequency because of the MOSFET flick noise, and degenerates at high frequency due to the input parasitic capacitances

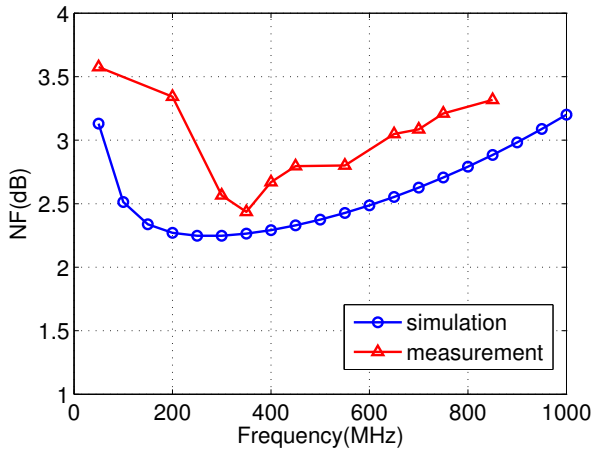


Fig. 7. Simulated and measured NF.

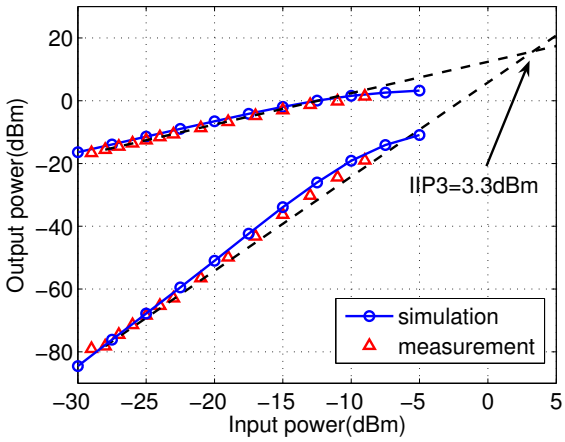


Fig. 8. Simulated and measured IIP3.

TABLE I
SUMMARY OF MEASUREMENT RESULTS AND PERFORMANCE COMPARISON

	[2]	[5]	[6]	[7]	This Work
Process	0.25μm CMOS	0.5μm CMOS	0.18μm CMOS	0.18μm CMOS	0.25μm CMOS
Frequency	150-2000 MHz	50-700 MHz	54-880 MHz	470-860 MHz	50-860 MHz
S_{11}(dB)	-8	N/A	-10	N/A	-9
S_{21}(dB)	13.7	14.8	10-22	10	13.4
S_{12}(dB)	-36	-41	N/A	N/A	-19
S_{22}(dB)	-12	N/A	N/A	N/A	-10
NF(dB)	1.8-2.2	2.3-3.3	4.2-6	5.7	2.4-3.5
1dBCP(dBm)	-9	N/A	N/A	N/A	-6.7
IIP3(dBm)	0	-4.7	4.3-5 @11dB	10	3.3
Power	14mA×2.5V	3.3mA×3V	23mA×1.8V	2.9mA×1.8V	12mA×2.5V
Chip size(mm^2)	0.3×0.25	1.0×1.2	1.19×0.59	N/A	0.15×0.18

which cause the noise-canceling condition deviating.

The third-order intercept point is measured with a two-tone test at 500 MHz and 502 MHz, as shown in Fig. 8. The measured IIP3 is 3.3 dBm and varies slightly with the two-tone frequencies. The input-referred 1dB compression point (1dBCP) measures to be –6.7 dBm at 500 MHz.

Table I gives the measurement results compared with recently published works. It can be seen that the S-parameters performance of this work are approaching to the others, and the IIP3 increases 3.3 dB and power consumption decreases 2 mA compared to [2]. Furthermore, the presented LNA occupies the smallest chip size.

V. CONCLUSION

In this paper, a wide-band CMOS LNA exploiting a noise-canceling technique is designed and measured, and the voltage gain, noise figure and linearity of the LNA is analyzed in detail. The circuit design process and parameter calculation method are also presented. Measurement results show that the presented LNA achieves good input/output 50 Ω impedance matching, high gain, low noise figure and high linearity in 50-860 MHz frequency range, and meets the requirements of the TV tuner applications.

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