A Low-phase-noise 1-GHz LC VCO Differentially Tuned by Switched Step Capacitors

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***Abstract*—This paper proposes a novel 1-GHz LC oscillator differentially tuned by switched step capacitors, which is implemented in a 0.25μm 1P5M CMOS process. A period calculation technique (PCT) is adopted to analyze the differential tuning characteristic of switched step capacitors. Due to the symmetric oscillation waveforms, the differentially tuned LC VCO has 7 dB phase noise reduction in the $1/f^3$ region compared to the single-ended tuned topology, and 23.6dB CMRR. It achieves phase noise –83 dBc/Hz, –107 dBc/Hz and –130 dBc/Hz respectively at 10-kHz, 100-kHz and 1-MHz offsets, while dissipating 3.3 mA current at 2.6 V power supply. Chip size is 0.82 mm×0.84 mm.**

I. INTRODUCTION

Due to the common-mode noise in LC oscillators, such as the noise at control voltages, power supply or in tail current, there exists large close-in phase noise up-converted by AM-to-PM mechanism from low-frequency flicker noise [1, 2]. The differentially tuned LC oscillators have an advantage of common-mode noise suppression as well as other differential circuits. However, the implementation of differentially tuned LC oscillators is not easy.

Two p-n diode varactors connected in anti-parallel configuration can implement differentially tuned topology [2]. But positive and negative tuning voltages have only $V_{DD}/2$ tuning range in order to prevent the varactors from being forward biased. It is evident that the differentially diode varactors suffer more severely from the AM-to-PM conversion. Accumulation MOS varactors in CMOS process cannot offer symmetric characteristics of anode and cathode compared to SOI technology [3]. AC coupling varactors is a viable way to mitigate their non-linearity and in turn the effects of AM noise. However, the reduction of the C-V nonlinearity is typically paid in terms of narrower tuning range [2,4].

A novel LC VCO is proposed in this paper, which is differentially tuned by a pair of positive and negative step capacitors [6]. The positive and negative tuning voltages can tune from V_{SS} to V_{DD}. And additional AC coupling capacitors are not required. Due to the symmetric oscillation waveforms, the phase noise in the $1/f^3$ region is improved.

This paper is organized as follows. In Section II, a period calculation technique (PCT) is proposed to analyze the differentially tuning characteristic, and explain in detail why the phase noise in the differentially tuned topology is better than that in the single-ended tuned topology. Section III describes the actual implementation of a novel 1-GHz CMOS LC VCO differentially tuned by switched step capacitors. Section IV presents the measured F-V curves, voltage-to-frequency gain K_{VCO} curves and phase noise. Finally, conclusions are drawn in Section V.

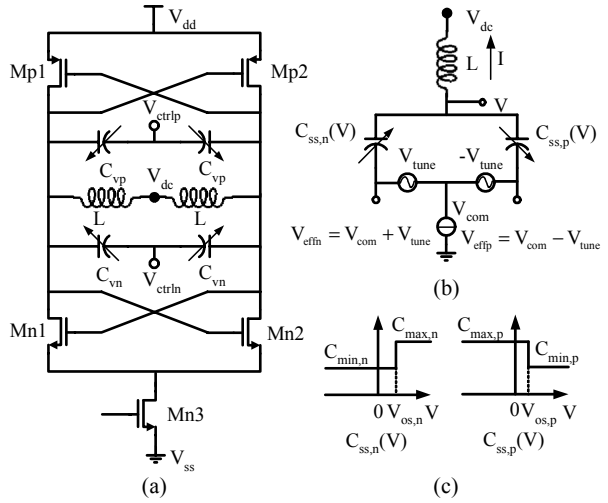

Fig. 1. CMOS differentially tuned LC-tank VCO, (a) LC-tank VCO, (b) Simplified half circuit, (c) Step C-V curves

II. FREQUENCY TUNING CHARACTERISTIC OF DIFFERENTIALLY TUNED LC OSCILATORS

A differentially tuned LC oscillator, shown in Fig. 1(a), consists of positive-step varactors and negative-step varactors. The presence of on-chip inductors in Fig. 1(a) imposes that the dc value of differential oscillation voltages must be a constant voltage V_{dc}. Neglecting the tank losses of on-chip inductors and varactors, the simplified half circuit of LC-tank VCO can be considered as a series or parallel LC tank [1, 6]. Without loss of generality, a series LC tank, shown in Fig. 1(b), is considered here. The small-signal capacitance of positive-step and negative-step varactors are respectively given by:

$$\text{Positive-step capacitor: } C_{ss,n}(V)=\begin{cases} C_{max,n} & V \ge V_{os,n} \\ C_{min,n} & V < V_{os,n} \end{cases},$$

$$\text{Negative-step capacitor: } C_{ss,p}(V)=\begin{cases} C_{min,p} & V \ge V_{os,p} \\ C_{max,p} & V < V_{os,p} \end{cases}. \quad (1)$$

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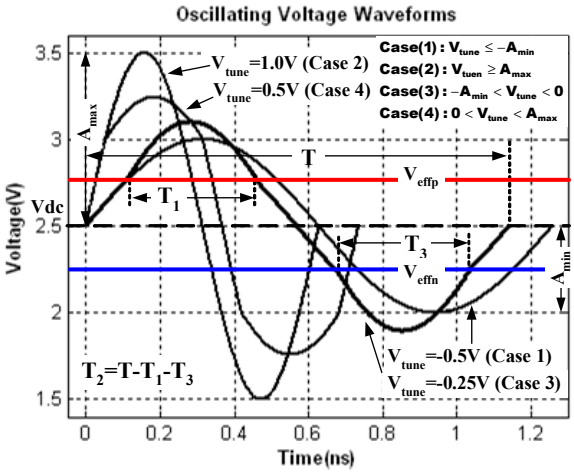

Fig. 2. Oscillation voltage waveforms

where $V_{os,n}$ and $V_{os,p}$ are C-V voltage offsets. V_{ctrln} and V_{ctrlp} are the control voltages, and we define $V_{effn}=V_{ctrln}+V_{os,n}$ and $V_{effp}=V_{ctrlp}+V_{os,p}$ *effective control voltages* (ECV) of positive-step and negative-step varactors. The common-mode tuning voltage is $V_{com}=(V_{effn}+V_{effp})/2$, and the differential tuning voltage is V_{tune}. Thus, the positive tuning ECV V_{effn} is $V_{com}+V_{tuen}$, and the negative tuning ECV V_{effp} is $V_{com}-V_{tune}$. For the sake of the symmetric tuning characteristics, V_{com} normally equals V_{dc}, and $C_{min,n}=C_{min,p}$, $C_{max,n}=C_{max,p}$.

A. *Period Calculation Technique*

In [6], a period calculation technique was first introduced to analyze a single-ended tuned LC oscillator. Here, it is adopted to calculate the oscillation period of a differentially tuned LC oscillator.

Fig. 2 shows oscillation voltage waveforms of a series LC tank. The ECV voltages V_{effn} and V_{effp} control the small-signal capacitance $C_{ss,n}$ and $C_{ss,p}$ to be a minimum or maximum. Therefore, each waveform consists of three segmental sinusoids of different sizes, which join at ECVs. With the differential tuning voltage V_{tune} changes from low to high, there exist four cases.

For example, Case(3) is $-A_{min}<V_{tune}<0$, $V_{dc}-A_{min}<V_{effn}<V_{dc}$, and $V_{dc}+A_{min}>V_{effp}>V_{dc}$, where A_{min} is the minimum oscillation amplitude. When the oscillation voltage is above V_{effp}, the equivalent capacitance of the LC tank is $C_{mid}=C_{max,n}+C_{min,p}$; when the oscillation voltage is below V_{effp} and above V_{effn}, the equivalent capacitor is $C_{max}=C_{max,n}+C_{max,p}$; when the oscillation voltage is below V_{effp}, the equivalent capacitor is $C_{mid}=C_{min,n}+C_{max,p}$. Thus the oscillation waveform comprises three segmental sinusoids joined at V_{effn} and V_{effp} ECVs. One is over V_{effp} with amplitude θA_{mid} (θ is an *ellipse similar factor, ESF* [6]) and frequency ω_{mid}; the second is below V_{effp} and above V_{effn} with amplitude A_{min} and frequency ω_{min}; the third is below V_{effn} with amplitude θA_{mid} and frequency ω_{mid}. The I-V locus of three segmental sinusoids holds

$$\left(\frac{V-V_{dc}}{A_{mid}}\right)^2+\left(\frac{I}{\omega_{mid}C_{mid}A_{mid}}\right)^2=\theta^2,\ V\ge V_{effp}$$
$$\left(\frac{V-V_{dc}}{A_{min}}\right)^2+\left(\frac{I}{\omega_{min}C_{max}A_{min}}\right)^2=1,\ V_{effp}>V>V_{effn}$$
$$\left(\frac{V-V_{dc}}{A_{mid}}\right)^2+\left(\frac{I}{\omega_{mid}C_{mid}A_{mid}}\right)^2=\theta^2,\ V_{effn}\ge V \quad (2)$$

where θ satisfies $A_{min}/A_{mid}\le\theta\le 1$. When $V_t=0$, $\theta=1$, and $V=V_{dc}$, three equations of (2) satisfy

$$I_{max}=\omega_{mid}C_{mid}A_{mid}=\omega_{min}C_{max}A_{min} \quad (3)$$

where I_{max} is the maximum current in the inductor.

The oscillation period is a sum of three intervals $T=T_1+T_2+T_3$, shown in Fig. 2. T1, T2 and T3 are respectively a time interval of the first, second and third segmental sinusoids. From (3), we obtain the amplitude ratio

$$\frac{A_{min}}{A_{mid}}=\sqrt{\frac{C_{mid}}{C_{max}}} \quad (4)$$

When the oscillation voltage equals V_{effp} (or V_{effn}), we define the inductor current $I=I_{effp}$ (or I_{effn}). Substituting (4) in the first (or last) two equations of (2) and eliminating I_{effp} (or I_{effn}) lead to the ESF θ

$$\theta=\sqrt{1-\left(\frac{V_{tune}}{A_{min}}\right)^2+\left(\frac{V_{tune}}{A_{mid}}\right)^2} \quad (5)$$

Thus, the oscillation period is

$$T=T_1+T_2+T_3=\frac{\pi-2sin^{-1}\left(\frac{-V_{tune}}{\theta A_{mid}}\right)}{\pi}T_{mid}+\frac{2sin^{-1}\left(\frac{-V_{tune}}{A_{min}}\right)}{\pi}T_{max} \quad (6)$$

where $T_{mid}=2\pi\sqrt{LC_{mid}}$ and $T_{max}=2\pi\sqrt{LC_{max}}$.

B. *Advantage of Suppressing AM-PM Conversion*

At any control voltage, in Fig. 2, the first segmental sinusoid is symmetric to the third one. The oscillation voltage waveform in a differentially tuned LC VCO always remains symmetric. However, a single-ended tuned LC VCO has asymmetric waveform in the whole tuning range [6]. Therefore, the differentially tuned application has an advantage of suppressing the up-conversion by AM-to-PM mechanism from low-frequency flicker noise at power supply and tail current [7].

In a single-ended tuned LC VCO, the oscillation frequency sensitivity to the common-mode noise is the same as the voltage-to-frequency gain K_{VCO}. So the low-frequency phase noise converted by the AM-FM conversion from the common-mode noise can only be filtered by the low-bandwidth PLL closed loop. From (6), we can conclude that the oscillation period is insensitive to the common-mode voltage. So the sensitivity is $K_{VCO,COM}=\partial\omega_0/\partial V_{COM}=0$. Therefore, a differentially tuned LC VCO itself has an advantage of suppressing the common-mode noise from control voltages, power supply, and tail current.

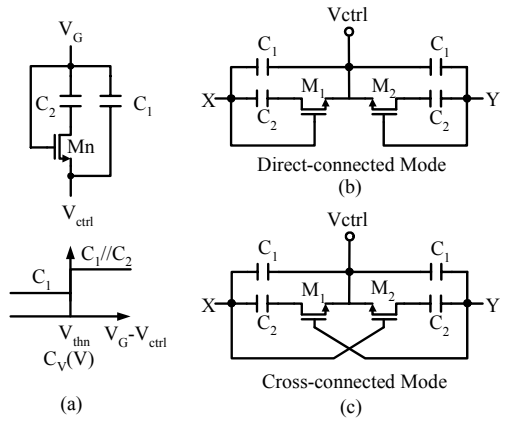

Fig. 3. Equivalent circuit of a step MOS capacitor

III. CIRCUIT IMPLEMENTAION

From the frequency tuning analyses in [6], we can conclude that any capacitor with a step C-V characteristic can be used to implement a LC VCO with a linear F-V curve. In this section, a novel equivalent circuit with a step C-V curve is proposed to implement a LC VCO.

A. Switched Step Capacitors

An equivalent circuit of a step MOS capacitor is shown in Fig. 3(a), which comprises two Metal-Insulator-Metal (MIM) capacitors and a switching NMOS transistor. Neglecting the body effect and parasitic capacitors of MOS transistor, if the voltage between V_G and V_{ctrl} satisfies V_G-V_{ctrl}<V_{thn}, the capacitance of an equivalent circuit is a minimum, C_{min}=C_1; and otherwise it is a maximum, C_{max}=C_1+C_2. On selection of capacitors C_1 and C_2, any capacitance ratio can be obtained. There exist two kinds of differential topologies with two back-to-back switched step varactors. One structure is the direct-connected mode, as shown in Fig. 3(b), in which the oscillation voltages (X and Y) control the varactors in the same side. The other is the cross-connected mode, as shown in Fig. 3(c), in which the oscillation voltages control the opposite varactors. Noticing that the oscillation voltages V_X and V_Y are differential, the SpectraRF simulation shows that the cross-connected topology is better than the direct-connected topology in differential LC VCOs in terms of phase noise.

B. Differentially Tuned LC Oscillator

A differentially tuned LC-VCO is shown in Figure 4, in which the tank consists of an on-chip differential inductor L and switched step capacitors. The NMOS transistors Mn3-Mn4 and MIM capacitors C_{n1}-C_{n2} form a positive-step capacitor, and PMOS transistors Mp3-Mp4 and MIM capacitors C_{p1}-C_{p2} generate a negative-step capacitor. In order to reduce common-mode voltage-to-frequency gain, positive-step capacitors (C_{n1}-C_{n2}) must completely equal negative-step ones (C_{p1}-C_{p2}). The zero threshold transistors, NMOS Mn3-Mn4 and PMOS Mp3-Mp4, are used to eliminate the offset of F-V tuning curve, and to improve the Common-Mode Rejection Ratio (CMRR) of voltage-to-frequency gain K_{VCO}. Two additional inductors, L_1 & L_2 (28nH each), resonate at double frequency with the parasitic capacitors (C_3 & C_4) at each common-source node, avoiding Q-degradation by triode region MOS transistors in the stacked differential pairs. The current mirrors, Mp5 and Mp6, provide enough current to generate a large voltage swing in the current-limited mode. MIM capacitors C_1 and C_2 are added to adjust the center frequency.

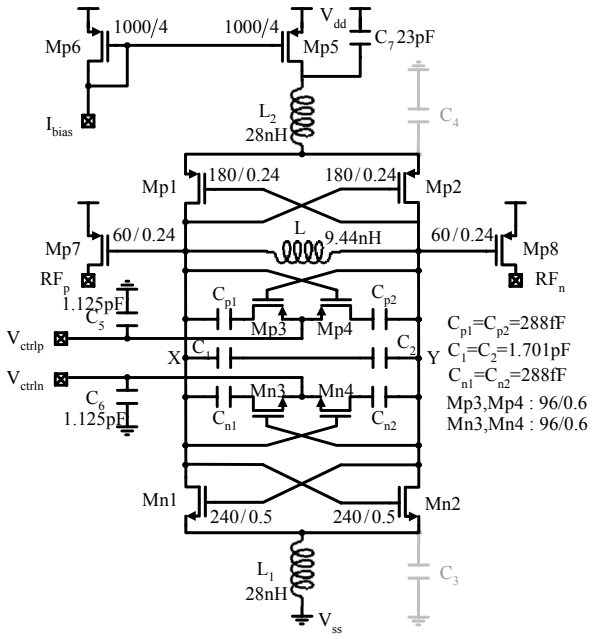

Fig. 4. LC oscillator differentially tuned by switched step capacitors

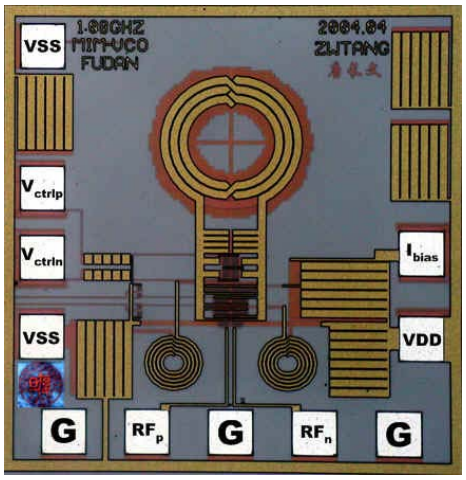

Fig. 5. Microphotograph of differentially tuned LC VCO

IV. MEASUREMENT VALIDATIONS

The prototype circuit was manufactured in a 0.25μm 1P5M CMOS process, and its microphotograph is shown in Fig. 5. The oscillator IC operates from 2.6 V and biases at 3.3mA. Chip-On-Board (COB) packaged chips are measured on an Agilent E4440A (3Hz~26.5GHz) PSA Serial Spectrum Analyzer with Phase Noise Module.

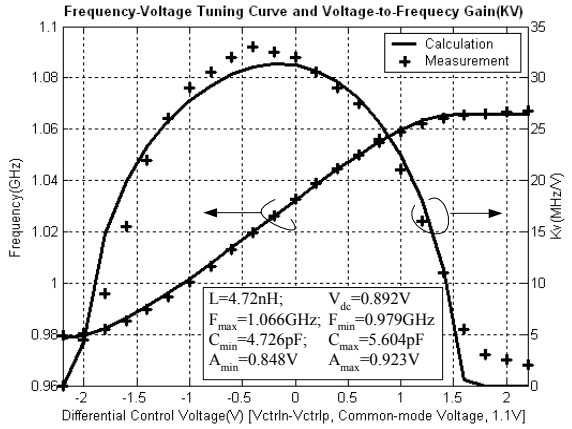

Fig. 6. Differentially tuned F-V curve and K_{VCO} gain

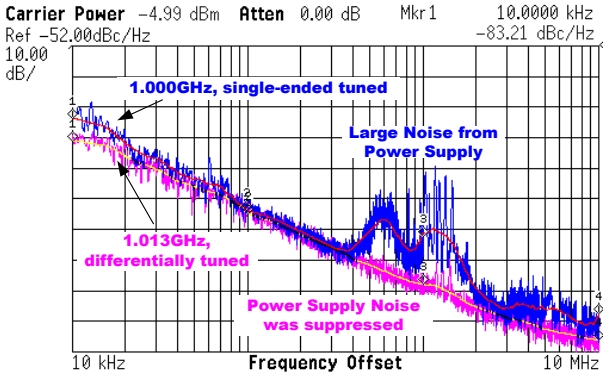

Fig. 7. Measured phase noise

A. F-V Tuning Curve Measurements

At the common-mode voltage (V_{ctrlp}+V_{ctrln})/2=1.1 V, the differentially tuned F-V curve and voltage-to-frequency gain K_{VCO} are plotted in Fig. 6. The solid line is calculated by the theoretic analysis in Section II. And the cross line is the measured result, which is in good agreement with the theoretic prediction. When the differential control voltage $2V_{tune}$ tunes from –2.2 V to 2.2 V, the oscillation frequency ranges from 0.979 GHz to 1.066 GHz. The linear tuning range covers from –1.6 V to 1.1 V with >20MHz/V differentially tuned voltage-to-frequency gain, which is 77% of the tuning range from -2.0 V to 1.5 V.

There exists only 2-MHz difference between common-mode control voltages 0 V and 2.6 V. A large frequency deviation of 8.5-MHz occurs at the middle of 0~2.5 V. The maximum differentially tuned K_{VCO} gain is about 33MHz/V, and according to the publication [3], Common-Mode Rejection Ratio (CMRR) of K_{VCO} gain is about 23.6 dB.

B. Phase Noise Measurements

The phase noises at about 1.0 GHz, both in the single-ended and differentially tuned applications, are plotted in Fig. 7. The single-ended tuned VCO is biased at V_{ctrlp}=0 V and V_{ctrln}=0.9 V. Only V_{ctrln} is tuning effective. It measures –75.97 dBc/Hz, –105.82 dBc/Hz respectively at 10-kHz and 100-kHz offsets from the carrier. Due to the large switching noise from DC-DC converter power supply, there exists worst phase noise at about 500-kHz and 1.5-MHz offsets. The differentially tuned VCO at 1.013GHz is biased at V_{ctrln} =0.8V and V_{ctrlp}=1.4V. It measures –83.21 dBc/Hz, –106.93 dBc/Hz and –129.76 dBc/Hz respectively at 10-kHz, 100-kHz and 1-MHz offsets.

The $1/f^3$ phase noise (at 10-kHz offset) in the differentially tuned application has 7 dB reduction compared to the single-ended tuned topology. The differentially tuned application also has much advantage of suppressing the up-conversion by AM-to-FM mechanism from low-frequency flicker noise at power supply.

V. CONCLUSIONS

A period calculation technique (PCT) is adopted to analyze the frequency-tuning characteristic of a differentially tuned LC VCO. According to PCT, we can conclude that a differentially tuned topology has two advantages: the symmetric oscillation waveform and suppressing AM-FM conversion from the common-mode noise at control voltages, power supply, and tail current. A novel LC oscillator, which is differentially tuned by switched step capacitors, is implemented in a 0.25μm 1P5M CMOS process. In the $1/f^3$ region, the differentially tuned topology has 7dB phase noise reduction compared to the single-ended tuned topology.

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