A Wideband CMOS Variable-Gain Low Noise Amplifier with Novel Attenuator

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Abstract
This paper presents a wideband variable-gain low noise amplifier (VGLNA) which is used in mobile TV tuner covering VHF band (50 to 250 MHz) and UHF band (470 to 860MHz). The proposed VGLNA includes three gain paths for different input signal strengths: high gain path, attenuation path, medium gain path. The high gain path is realized by an active AC feedback LNA, whose DC current is set by a constant-G_m biasing; the novel attenuator used in attenuation path has constant input impedance which guarantees a good *S*11 with the variety of gain; the medium gain path is the combination of one active AC feedback LNA and one attenuator. The chip is implemented in 0.18 μm CMOS process and achieves a gain range over 42 dB (2dB/step), a minimum noise figure of 2 dB at maximum gain, an IIP3 of 27.9 dBm at minimum gain. The die consumes 8 mA from 1.8 V supply voltage at maximum gain.

1. Introduction

Although a lot of efforts have been devoted to the research of TV tuners and important achievements have been made [1] [2], designing a distinguished TV tuner supporting multi-standard multi-band is still full of challenges. As the first active stage of TV tuner, VGLNA plays a vital role in the overall performance.

A mobile TV tuner may receive a signal level as high as -10 dBm or as low as -110 dBm. Low noise figure and high gain are needed for low level input, which is critical especially for LNA. As the input level increasing, the corresponding gain should be reduced so that the subsequent stages remain sufficiently linear with the large input signal. An attenuator is often used with even higher input level.

A novel attenuator with high linearity, small gain step and better noise performance is proposed in this paper. The high gain path is realized by an active feedback LNA which is similar to the one in [3], but the feedback is only AC coupling. The gain step in the high gain path is realized by changing the g_m of amplifying MOS. In the next section, the detail implementation of the proposed VGLNA will be described. The measurement results will be given at last.

2. Circuit realization

The target is to design a CMOS wideband VGLNA suitable for TV tuner whose gain range is -22 ~ 20 dB with 2 dB/step and covering both VHF and UHF band. It has two different inputs, one for VHF and the other for UHF, to isolate each other. Figure 1 shows the overall topology of the wideband VGLNA. When only S3 is on, -22 dB ~ -6 dB is achieved by a novel attenuator (ATT) for VHF or UHF; when only S0 and S2 are on, -4 dB ~ 14 dB can be realized by combining one ATT and one active AC feedback LNA which constitute medium gain path (MGP), and 14 dB ~ 20 dB for VHF or UHF can be acquired by the other active AC feedback LNA when only S1 or S4 is on which is high gain path (HGP). The capacitor C_0 in figure 1 is used to insulate the DC signal of LNA for MGP. All switches are controlled by a simple digital control unit.

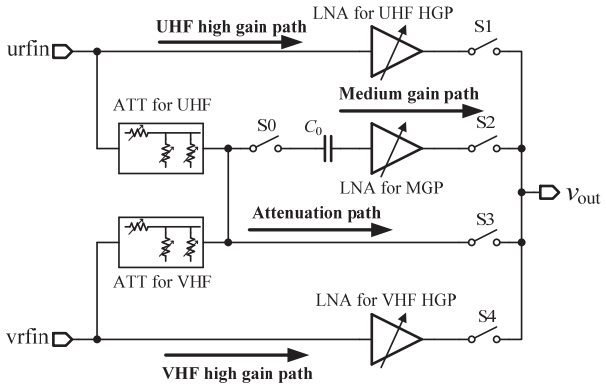

Figure 1. The overall topology of the VGLNA

2.1 High gain path (HGP)

Figure 2 shows the circuit topology in high gain path. The active AC feedback LNA presented in this paper separates DC signal from its signal paths so the feedback is just an AC feedback achieved by R_1, C_1 and R_F, C_F, and DC current can be set independently. A constant-G_m biasing circuit [4] is used to bias the amplifying MOSs MA1 ~ MA4 and the cascode MOSs MC1 ~ MC4. The inductor L is employed to extend output bandwidth which is not needed in VHF high gain path. So VHF and UHF high gain path have a little difference.

A. Input matching and gain analysis

To implement a gain step of 2 dB, four switches are used to change the g_m of amplifying MOS. When all switches are connected up, maximum gain is achieved.

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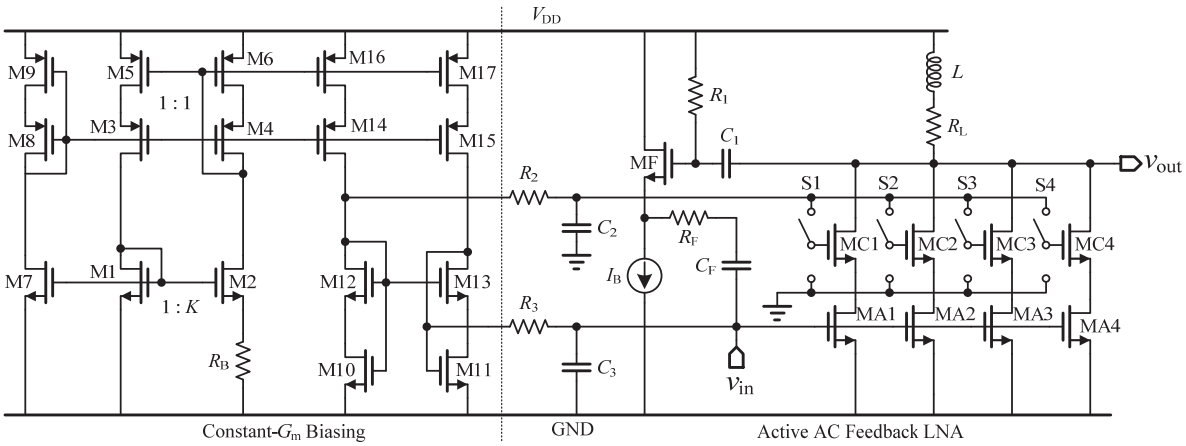


Figure 2. The circuit topology in high gain path

Minimum gain can be obtained when only S1 is connected up. A simplified circuit as shown in figure 3 can be used to analysis the performance of the circuit when the parasitic resistance of L is neglected.

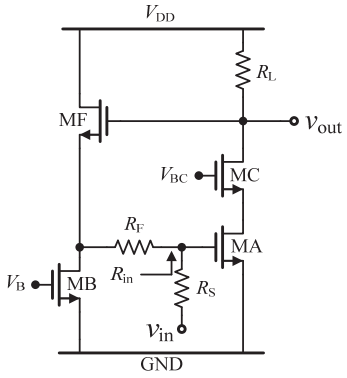


Figure 3. Simplified circuit for analysis

The input impedance R_{in} can be calculated as

$$R_{in} = \frac{1 + g_{mF} R_F}{(1 + g_{mA} R_L)\, g_{mF}} \tag{1}$$

where g_{mA} is the transconductance of the device MA, and g_{mF} is the transconductance of the device MF. If input is matched, then $R_{in} = R_S$, so the input matching can be achieved when

$$1 + g_{mF} R_F = (1 + g_{mA} R_L)\, g_{mF} R_S . \tag{2}$$

It is obvious that the value of R_F should follow the variety of g_{mA} i.e. the variety of gain when the value of g_{mF} is constant. To achieve a good input matching performance with the variety of gain, R_F is chosen to be increasing as gain increase.

Ignoring the second order effect, the small signal AC gain can be expressed as

$$\frac{v_{out}}{v_{in}} = -\frac{(1 + g_{mF} R_F) g_{mA} R_L}{1 + (1 + g_{mA} R_L) g_{mF} R_S + g_{mF} R_F} . \tag{3}$$

When the condition of input matching is applied, i.e. substitute equation (2) into (3)

$$\frac{v_{out}}{v_{in}} = -\frac{1}{2} g_{mA} R_L . \tag{4}$$

So changing g_{mA} can directly change the gain. With the constant-G_m biasing, equation (4) can be further derived

$$\frac{v_{out}}{v_{in}} = -\sqrt{\alpha}\, \frac{R_L}{R_B} \left(1 - \frac{1}{\sqrt{K}}\right) \tag{5}$$

where α is scale factor of the current mirror. The above expression is immune to the variations of process, voltage and temperature (PVT). It is just impacted by the proportion of two resistances, which can be relatively accurate by taking good care of layout.

B. Noise and nonlinearity consideration

Since the small signal AC gain has been calculated, every noise source can be equivalent to the output in a similar way by simply calculating the transform function from the noise source to the output. If the flicker noise is not considered, the noise figure (*NF*) is [3]

$$\begin{aligned} NF = 1 &+ \frac{\gamma_A}{g_{mA} \cdot R_S} \left(\frac{2 + A_v}{1 + A_v}\right)^2 + \frac{R_F}{R_S (1 + A_v)^2} \\ &+ \frac{\gamma_F}{1 + A_v} \left[1 - \frac{R_F}{R_S (1 + A_v)}\right] + \frac{1}{g_{mA} \cdot R_S A_v} \left(\frac{2 + A_v}{1 + A_v}\right)^2 \\ &+ \gamma_B \cdot g_{mB} \cdot R_S \left[1 - \frac{R_F}{R_S (1 + A_v)}\right]^2 \end{aligned} \tag{6}$$

where γ is a coefficient which equals to 2/3 for long channel transistors and may be replaced by a larger value for submicron MOSFETs. A_V equals to $g_{mA}\, R_L$. Since $A_V >> 1$, above expression becomes

$$NF \approx 1 + \frac{\gamma_A}{g_{mA} \cdot R_S} + \gamma_B \cdot g_{mB} \cdot R_S . \tag{7}$$

If a long channel MOS is used for the device MB and its overdrive voltage is set as large as possible, the contribution of the bias device MB can also be neglected.

So the main contribution of noise figure is from the noise of amplifying MOSs. A larger g_{mA} obviously yields a lower noise figure and also pays the price for larger parasitic capacitance lowering the noise figure at high frequency. Since the target frequency is much larger than the 1/f corner, excluding 1/f noise will not influence the result too much.

As the output signal is a large signal compared to the input signal. When a large signal is applied to the gate of the device MF, the dominate contribution of nonlinearity will come from the nonlinearity of the device MF which degrades substantially IIP3 value. Additionally, the feedback can combine the second-order distortion with the fundamentals of the output signal, generating third-order distortion at the output, which further worsens the IIP3 value. Decreasing gain, increasing the overdrive voltage of the device MF and increasing the value of R_F will improve IIP3 [3], but there are always trade-offs among noise, IIP3, voltage headroom, input matching, etc.

2.2 Proposed attenuator (ATT)

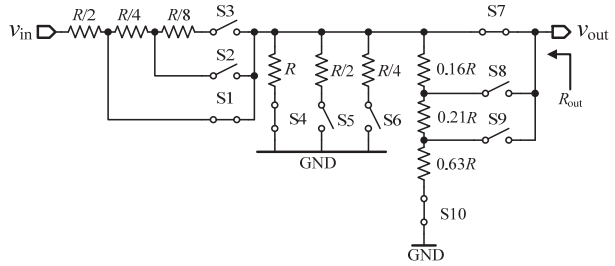


Figure 4. The schematic of attenuator

Figure 4 shows the schematic of attenuator, in which R equals to 50 ohms. The proposed attenuator has constant input impedance over all different gain modes, which grantees good input matching. For example, when only S1, S4, S10 and S7 are on, then

$$\frac{v_{out}}{v_{in}} = \frac{R \left\| (0.16R + 0.21R + 0.63R) \right.}{R \left\| (0.16R + 0.21R + 0.63R) \right. + \frac{R}{2}} = \frac{1}{2} = -6 \text{ dB} . \quad (8)$$

In the meanwhile

$$R_{in} = \frac{R}{2} + R \left\| (0.16R + 0.21R + 0.63R) \right. = R = R_S . \quad (9)$$

To acquire a step of 2 dB, S8 and S9 are introduced. If S7 is off and S8 is on in above situation, taking advantage of (8), then

$$\frac{v_{out}}{v_{in}} = \frac{1}{2} \cdot \frac{0.16R + 0.63R}{0.16R + 0.21R + 0.63R} \approx -8 \text{ dB} . \quad (10)$$

-10 dB can obtain by setting S9 on. Table 1 shows the detail control of switches and the corresponding gain.

The conventional R-2R topology in [5] has larger output impedance compared to the proposed one when the input is matched. Since larger output impedance introduces more output noise, the proposed one has better noise performance. As the minimum value of resistance is $R/8$, reducing the parasitic resistance of the switch is critical to ensure the accurate gain. Setting the size of S4, S5 and S6 inverse proportional to their relevant value of resistance can achieve better performance. The switch in [5] is selected for S1, S2, S3, and S7, S8 and S9, they have better linearity performance and good isolation characteristic when they are off. Those switches should also have their ratios.

Table 1. Switch control and the corresponding gain

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	Gain (dB)
1			1			1			1	-6
1			1				1		1	-8
1			1					1	1	-10
	1		1	1		1			1	-12
	1		1	1			1		1	-14
	1		1	1				1	1	-16
		1	1	1	1	1			1	-18
		1	1	1	1		1		1	-20
		1	1	1	1			1	1	-22

"1" denotes on, blank denotes off.

2.3 Medium gain path (MGP)

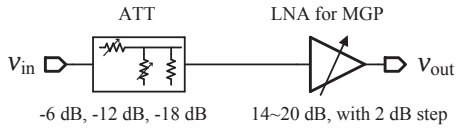


Figure 5. The block diagram of MGP

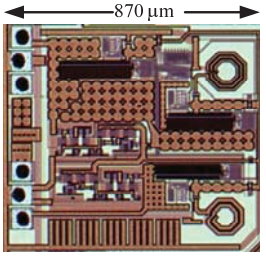
The block diagram of MGP is shown in figure 5. Just three gain modes are used in the attenuator, and the LNA employed here is similar to the LNA used in HGP. As VHF and UHF share the MGP, the bandwidth of MGP is different from the HGP, so the value of the inductor L and the resistance R_L. Another difference that should be noted is that the LNA for MGP do not need input matching anymore, which gives more freedom to optimize the noise and linearity performances. So the value of R_F is also different.

Since 14 dB have two different implementation ways which can be used to choose noise optimization or linearity optimization. For instance, choosing HGP to realize a 14 dB will have a better noise figure than choosing MGP, but the latter have better linearity performance. 8 dB gain and 2 dB gain have similar situations.

3. Measurement results

A prototype of this VGLNA which is fabricated in 0.18μm CMOS process occupies 870 μm x 760 μm area including pads. Figure 6 shows the die micrograph of the VGLNA and performance summary. Figure 7 shows the

measured noise figure at maximum gain, ranging from 2.0 dB to 2.4 dB for VHF band and 2.7 dB to 3.5 dB for UHF band. Figure 8 is the measured S11 at different gain, all of them below -9 dB no matter in VHF band or UHF band. Figure 9 depicts the gain step of the proposed attenuator. 2 dB gain step is realized well in VHF band. While in UHF band, the step is not consistent due to the parasitic effect in high frequencies. Figure 10 displays two tone IIP3 test result at minimum gain, in which two tone input frequencies are set 639.5MHz and 640.5MHz. The measured IIP3 is -7.6 dBm at maximum gain and +27.9 dBm at minimum gain which is just the IIP3 of the attenuator. The IIP3 tests in VHF band have similar results.



Technology	0.18 μm
Die Area	870 x 760 μm^2
Power	8mA @1.8 V
S11	< -9 dB
Gain Range	-22 ~ 20 dB
NF@20 dB	2.0 dB
IIP3@-22 dB	27.9 dBm
Frequency	50 ~ 250 MHz 470 ~ 860 MHz

Figure 6. Chip micrograph and performance summary

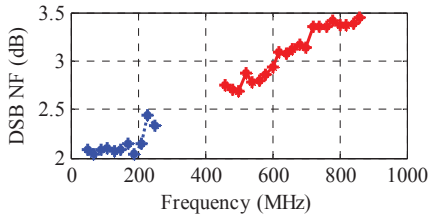


Figure 7. Measured noise figure @ maximum gain

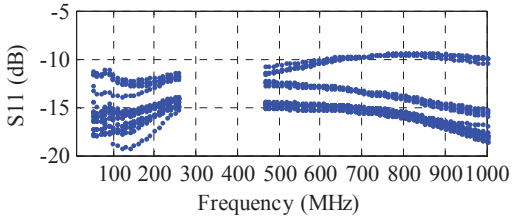


Figure 8. Measured S11 @ different gain

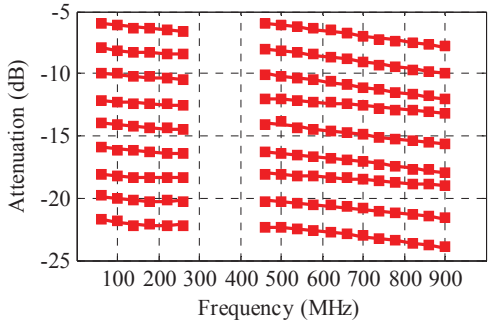


Figure 9. Measured gain step of attenuator

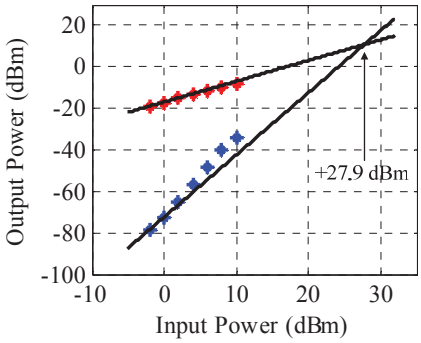


Figure 10. Measured IIP3 @ minimum gain

4. Conclusion

This paper demonstrates the design and implementation of a wideband CMOS VGLNA in 0.18 μm CMOS technology. Active AC feedback LNA has been used in high gain path, which has a good input matching performance over a wide frequency range and a low noise figure. A novel attenuator has been introduced in this paper. Its favorable matching feature, decent gain step coverage and nice linearity have been proved in the measurement results. The overall performance of this design is well suited for mobile TV tuner application.

Acknowledgments

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References

[1] Vassiliou I, Vavelidis K, Haralabidis N, et al. A 65 nm CMOS multistandard, multiband TV tuner for mobile and multimedia applications, Solid-State Circuits, IEEE Journal of, p.1522-1533 (2008).

[2] Shi Y, Dai F F, Yan J, et al. A fully integrated zero-IF mobile TV tuner RFIC for S-band CMMB application, Custom Integrated Circuits Conference, IEEE, p. 253-256, (2008).

[3] Borremans J, Wambacq P, Soens C, et al. Low-area active-feedback low-noise amplifier design in scaled digital CMOS, Solid-State Circuits, IEEE Journal of, p. 2422-2433 (2008).

[4] Razavi B, Design of Analog CMOS Integrated Circuits, p.392 (2003).

[5] Kefeng H, Xi T, Zhangwen T, et al. A wideband CMOS VGLNA based on single-to-differential stage and resistive attenuator for TV tuners. Journal of Semiconductors, p. 075003 (2011).