A Low Noise High Linearity CMOS Upconversion Mixer

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Abstract – In this paper, a low noise high linearity mixer is presented, exploiting a switched transconductor topology. Its noise figure (NF) and linearity are analyzed particularly. The mixer chip is implemented in 0.18-μm RF CMOS process. The measurement result shows that the conversion gain of the mixer is about 8dB, the SSB NF is about 11dB, and the input-referred third-order intercept point (IIP3) is about 10.5dBm. The chip consumes 10mA at 1.8V power supply and the size of the whole chip is 0.63mm×0.78mm.

I. INTRODUCTION

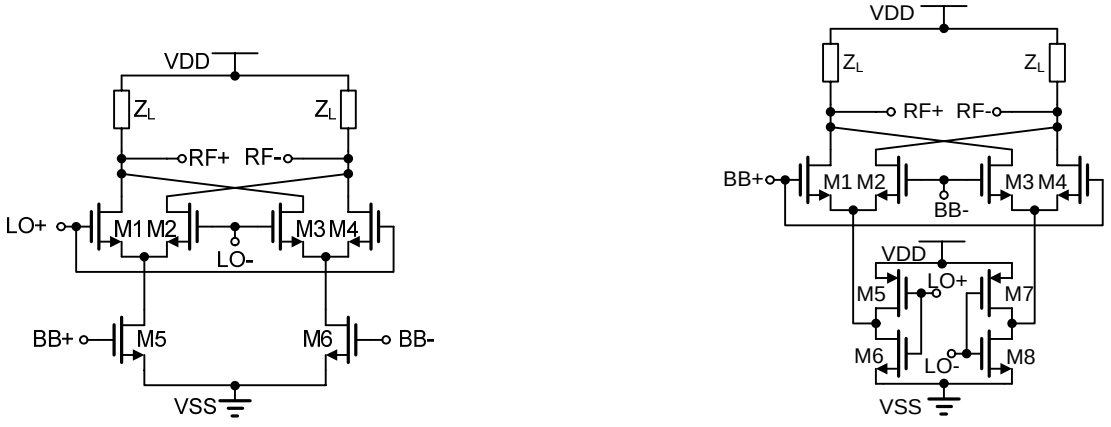
Upconversion mixers are important modules in RF transceivers, converting the low frequency baseband (BB) signal to RF band. The NF, which determines the sensitivity of the circuit, is a key performance of the upconversion mixer. The IIP3 determines the maximum signal level that the mixer can handle. A mixer with low NF and high IIP3 has larger dynamic range. This paper is organized as follows. In Section II, advantages of the switched transconductor mixer topology are analyzed compared with the conventional one. In Section III, the schematic of an upconversion mixer is introduced. Simulation and measurement results of the designed mixer are presented in Section IV. Finally, the conclusions are given in Section V.

II. MIXER TOPOLOGY

A. Topologies Comparison

Figure.1 (a) shows the conventional Gilbert mixer. It consists of a transconductance stage (M5, M6), switch pairs (M1~M4) and load impedances. The low frequency voltage signal is converted to the current signal by the transconductance stage, and then switched between the two signal paths by the switch pairs. Finally the load impedances convert the current signal back to the voltage signal.

Figure.1 (b) shows a switched transconductor upconversion mixer topology[1]. It also consists of transconductance stages (M1~M4), switch pairs (M5~M8) and load impedances. But the relative position of the former two is changed, and the switch pairs are replaced with inverters. In the positive half cycle of LO, the output of left inverter (consists of M5 and M6) is at low voltage level, while the output of right inverter is high. So, the left transconductance pair of M1 and M2 is switched on, while the right pair is off. In the negative half cycle of LO, the situation is opposite. The frequency translating principle is just the same as the conventional mixers.



(a) Conventional topology (b) Switched transconductor topology

Figure.1. Mixer topologies

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B. Noise Figure

The flick noise and thermal noise current generated by a MOSFET are as equation (1) and (2) respectively [2]. They are both functions of g_m. When the MOSFET is cut off, the noise can be negligible. Since the LO switches the transconductance stages periodically, only half of the transconductor MOSFETs are switched on at one time. Though the number of the transconductor MOSFETs doubles in the switched transconductor topology, the noise introduced is just the same as the conventional topology.

$$\overline{i_{n,1/f}^2} = \frac{K}{C_{ox}WL}\frac{1}{f}g_m^2 \quad (1)$$

$$\overline{i_{n,thm}^2} = 4kT\gamma g_m \quad (2)$$

In the switched transconductor topology, the noise current generated by the switches is in common mode, because the two MOS transistors from one transconductantor pair are working at the same state. Then the noise will be cancelled in the differential outputs. But in the conventional topology, the situation is totally different. Each switch transistor will contribute notable output noise [3]. That's why the switched transconductor topology has lower NF.

The approximate SSB NF of Gilbert mixers in Figure.1 (a) has been derived as equation (3) [4], where the α and c are LO related parameters, and γ, r_g and g_m denote the noise factor, gate resistance and transcondcutrance respectively.

$$NF_{SSB} = \frac{\alpha}{c^2} + \frac{2\left(\gamma_5 + r_{g5}g_{m5}\right)g_{m5}\alpha + 4\gamma_1\overline{G_1} + 4r_{g1}\overline{G_1^2} + 1/Z_L}{c^2 g_{m5}^2 R_s} \quad (3)$$

Since the noise generated by the switch is cancelled, the SSB NF of the switched transconductor topology can be derived as equation (4) [1].

$$NF_{SSB} = \frac{\alpha}{c^2} + \frac{2\left(\gamma_1 + r_{g1}g_{m1}\right)g_{m1}\alpha + 1/Z_L}{c^2 g_{m1}^2 R_s} \quad (4)$$

C. Linearity

When the transconductance stage is switched on, the common-source node of it is at low voltage. So, the NMOS of corresponding inverter is at linear region, acting as a resistor R_o. The output differential current can be derived as equation (5) [1], where the g_1,g_2 and g_3 denote the Taylor coefficients derived from the I-V of the MOSFET.

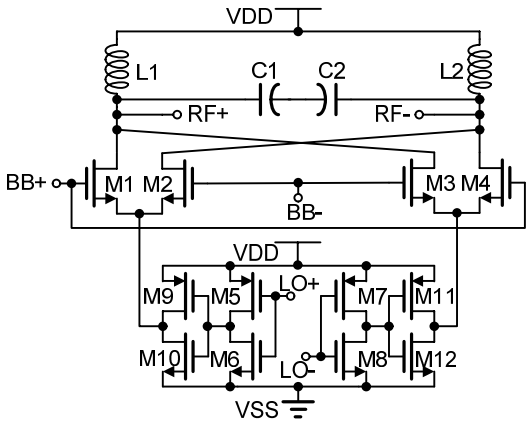


Figure.2. Schematic of the upconversion mixer

$$i_o = g_1 v_{RF} + \left(\frac{g_3}{4} - \frac{g_2^2 R_o}{1+2g_1 R_o}\right)v_{RF}^3 \quad (5)$$

Though g_3 is negative when the MOSFET is in strong inversion, the deterioration of the linearity resulted from R_o can be negligible if R_o is small enough.

III. UPCONVERSION MIXER DESIGN

Figure.2 shows the schematic of the low noise high linearity upconversion mixer. To achieve better switching, the size of the inverter should be increased. Out of question, that will lead to larger power dissipation. To solve this problem, two inverters with small size are cascaded to replace the single inverter switches. And the inverters with small size make the VCO design easier, reducing the driving capability requirement.

LC tank is employed as output loads, as the output signal is narrow RF band. There's no expense of any DC voltage headroom, So that the mixer can work in the low voltage power supply. In this design, a center-tapped differential inductor [5] is implemented, instead of two independent inductors to saves the chip area. The differential equivalent parallel resistance of the LC tank can be as high as 1k ohms, which reduce the requirement of g_m to achieve given conversion gain (CG). According to equation (6), the over drive voltage of the transconductance NMOS can be large, leading to good

linearity.

$$V_{GS} - V_T = \frac{2I_{DS}}{g_m} \quad (6)$$

IV. SIMULATION AND MEASUREMENT RESULT

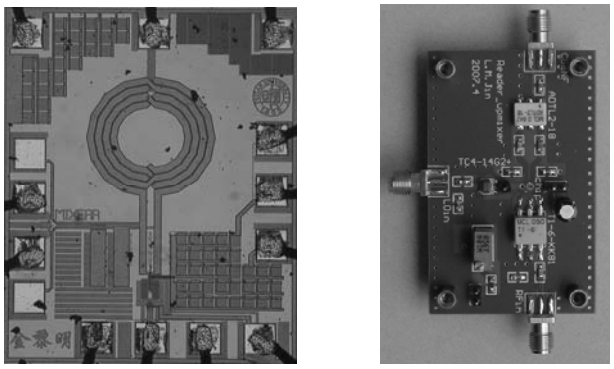
The chip is implemented in SMIC 0.18-μm RF CMOS process. Figure.3 is the photograph of the chip after bonding and the test PCB board. The chip size including IO pads is 0.63mm0×0.78mm. And it consumes 10mA current at 1.8V power supply on average. The chip is COB packaged to reduce the affect of parasitics. The power supply VDD is connected to the corresponding pad on the PCB via three bonding wires to reduce the parasitic inductance, which will deteriorate the RF performance of the circuit.

The 900MHz LO is given to measure the performance of the mixer chip. Figure.4 shows the simulated and measured conversion gain. The resonant frequency of the LC tank is about 50MHz away from simulation, and the Q factor is a little smaller so that the curve is more flatten.

The input referred third-order intercept point (IIP3) is measured with the two-tone test at 9.5MHz and 10.5MHz. Figure.5 shows the output spectrum when the power level of every input tone is -11dBm. The central two peaks are the two-tone signals, while the side two peaks are the third order intermodulation products. Figure.6 shows measured IIP3 with input level sweeping. Though the output is attenuated due to impedance mismatch, the IIP3 is not impacted absolutely, since it lies on the difference between the 1st and 3rd order. The measure IIP3 is 10.5dBm, while the simulated IIP3 is 12dBm.

Figure.7 shows the simulated and measured NF with output buffer, which will heighten NF by about 0.5dB. The measured SSB NF is about 11dB.

Table I gives the measurement results of the designed mixer compared with several published works. It can be seen that the NF and IIP3 performance of this work are more competitive. It should be noticed that SSB NF is 3dB larger than DSB NF commonly.



(a) (b)

Figure.3. Photograph of (a) the chip (b) the PCB

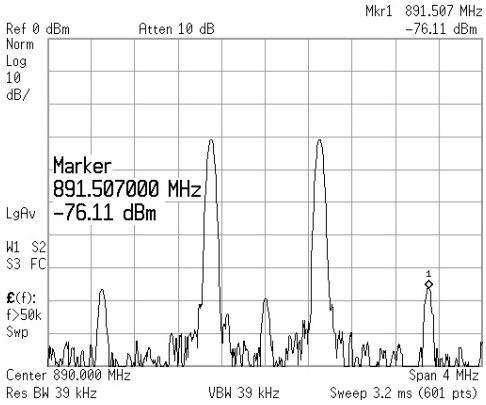


Figure.5. Spectrum of two-tone measurement

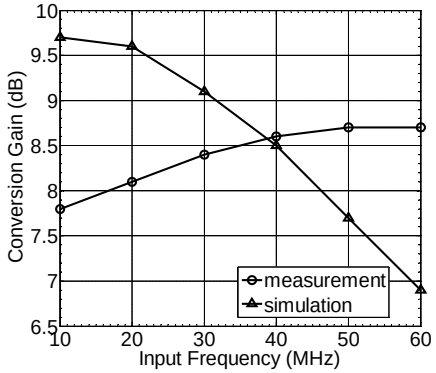


Figure.4. Simulated and measured CG

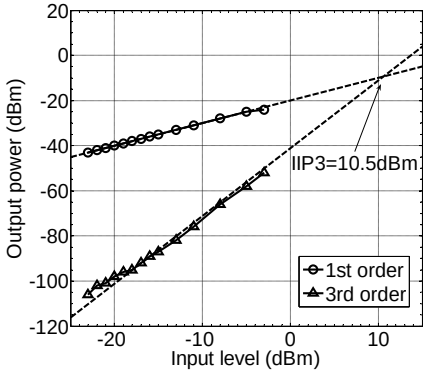


Figure.6. Measured IIP3

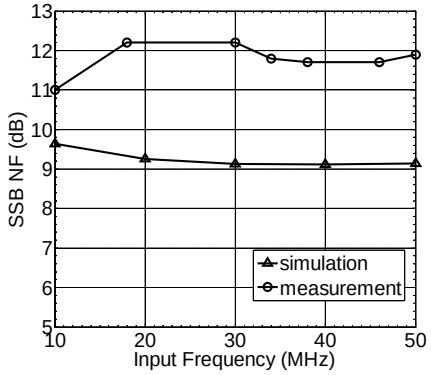


Figure.7. Simulated and measured NF

V. CONCLUSION

In this paper, an upconversion mixer exploiting a switched transconductor topology is designed and measured. The advantage of the topology in NF and IIP3 is analyzed compared with the conventional one. The measurement result shows that the designed mixer achieved high gain, low NF and high IIP3.

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Table I

Summary of measurement results and performance comparison

	[1]	[6]	[7]	This work
Process	0.18-μm CMOS	0.18-μm CMOS	0.13-μm CMOS	0.18-μm CMOS
Gain (dB)	10	6.6	1	8
NF (dB)	24 (DSB)	21 (SSB)	11.8 (DSB)	11 (SSB)
IIP3 (dBm)	6	1.5	11	10.5
Power	0.6mW	N/A	2mA×1.2V	10mA×1.8V
Die area (mm^2)	0.075×0.065 (core)	N/A	0.08×0.15	0.63×0.78