A high linearity multi-band and gain adjustable channel-select filter for TV-tuner application

Wang Xin(王心), Cheng Tao(程涛), Liu Jie(刘杰), and Tang Zhangwen(唐长文)†

ASIC & System State Key Laboratory, Fudan University, Shanghai 201203, China

Abstract: This paper presents a channel-select filter that employs an active-RC bi-quad structure for TV-tuner application. A design method to optimize the IIP3 of the bi-quad is developed. Multi-band selection and gain adjustment are implemented using switching resistors in the resistor array and capacitors in the capacitor array. Q-factor degradation is compensated by a tuning segmented resistor. A feed-forward OTA with high gain and low third-order distortion is applied in the bi-quad to maximize linearity performance and minimize area by avoiding extra compensation capacitor use. An RC tuning circuit and DC offset cancellation circuit are designed to overcome the process variation and DC offset, respectively. The experimental results yield an in-band IIP3 of more than 31 dBm at 0 dB gain, a 54 dB gain range with 6 dB gain step, and a continuous frequency tuning range from 0.25 to 4 MHz. The in-band ripple is less than 1.4 dB at high gain mode, while the gain error and frequency tuning error are no more than 3.4% and 5%, respectively. The design, which is fabricated in a 0.18 μm CMOS process, consumes 12.6 mW power at a 1.8 V supply and occupies 1.28 mm^2.

Key words: channel select filter; high linearity; gain adjustable; multi-band; TV tuner

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1. Introduction

Recently, increasing attention has been paid to direct conversion receivers (DCRs) due to their low power, small area and insensitiveness of image problem[1]. It is shown that multi-mode and multi-band DCR TV-tuner solutions are economical for applications[2]. In this architecture, a channel-select filter, which could select the wanted channels and filter out unwanted adjacent-channel interference, is needed. There are two important issues in DCRs that could be harmful to base-band circuits[3]. The first is DC offset due to the self-mixing of the mixer and other DC offset sources in the base band, such as the op-amp offset. The second is the $1/f$ noise. The most challenging aspect for the design of channel-select filters in the base band is the high linearity requirement due to the large range variation in the desired signal strength and the strong out-of-band interference, which could destroy the performance of the filter. So, a channel-select filter with DC offset cancellation, low noise, high in-band IIP3, as well as out-of-band IIP3 and multiple band selection, is needed for multi-standard TV-tuner applications. An active-RC filter is usually hired due to its high linearity performance[4, 5].

The Volterra series is usually used to analyze the linearity performance of a memory system[6]. But multi-feedback, which is commonly used in filter design, is not convenient and efficient for analysis using a signal flow graph (SFG). To simplify linearity analysis using the Volterra series, References [7, 8] discussed a new approach that treats multiple feedback loops as a two-port network by introducing three new network transfer functions. The scaling down technique was introduced to deal with the trade-off between the dynamic range or SFDR performance and power consumption. But the optimal parameter determination of components in the filter under certain power consumptions has not yet been discussed.

In this paper, an optimization method maximizing the bi-quad IIP3 by choosing optimal parameters of passive components in the bi-quad is discussed in detail for filter design. The band selection is completed not only using a resistor array, which could just realize discrete frequency selection, but also using a binary capacitor array, which is economical for realizing continuous frequency tuning. An on-chip auto-RC calibration circuit is designed to ensure an accurate cutoff frequency under RC variation.

Unlike the traditional structure that uses a programmable gain amplifier (PGA) with a large gain range before the channel select filter to cover the variation in base-band input signal strength, a gain variable filter with a large gain range and small gain error is proposed in this paper. The benefit of this system is that the optimization of IIP3 and noise can be considered at the same time to maximize the SFDR of the base-band circuit. In the final stage of the signal path, a post-PGA, which functions as an output buffer, is used to realize fine gain adjustment.

2. System design considerations

2.1. The filter structure

In a DCR system, the channel-select filter is actually a low-pass filter. The trade-off between power and adjacent rejection determines the order of the filter. An elliptic filter is chosen to meet the stringent rejection specification, as this type always provides a larger roll-off rate and moderate group delay at the same order compared to other types of filter[9].

A Tow-Thomas II bi-quad is chosen as the building block of this active RC filter to realize high linearity performance and orthogonal adjustment on the DC gain, cutoff frequency

† Corresponding author. Email: zwtang54@fudan.edu.cn

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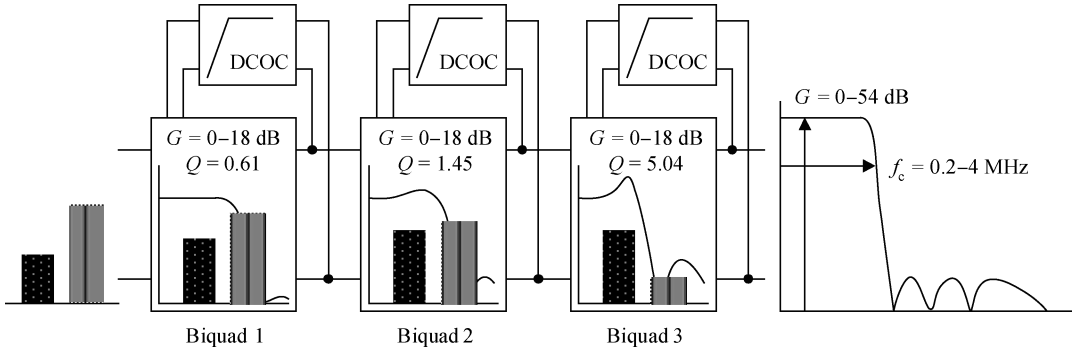


Fig. 1. The filter structure including DCOC.

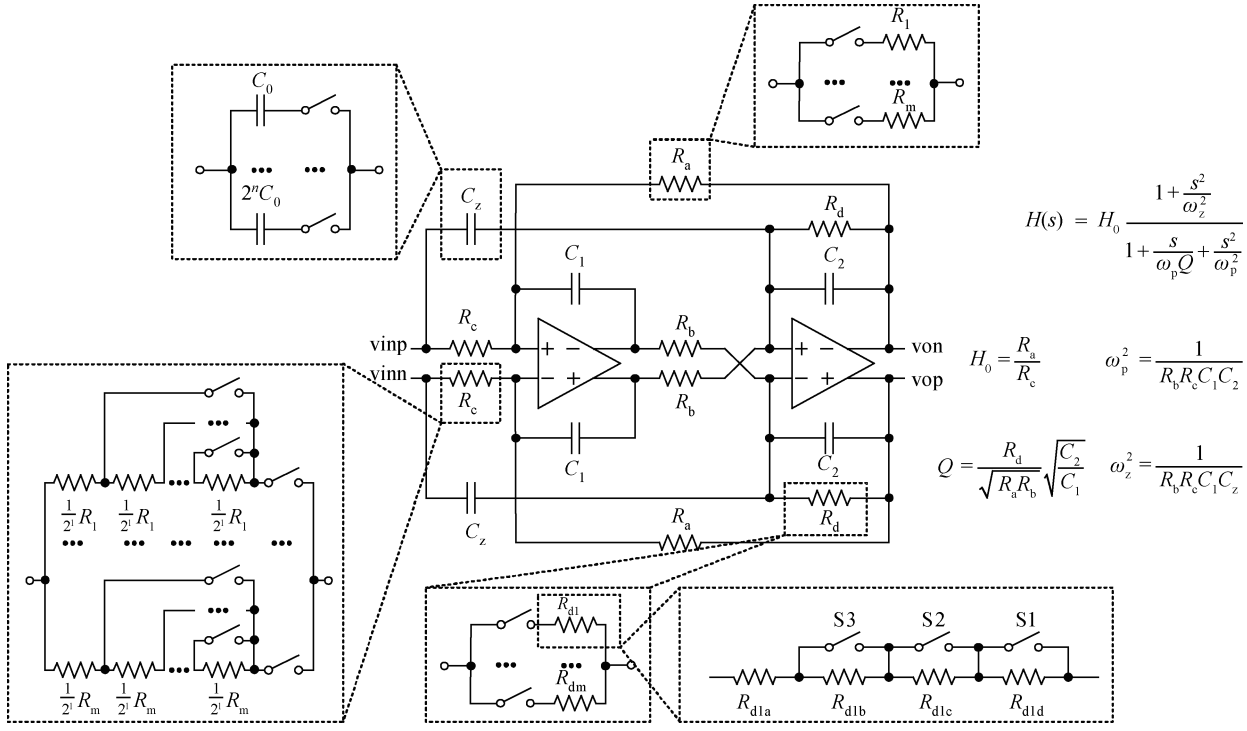


Fig. 2. The Tow-Thomas bi-quad structure.

and Q factor. Figure 1 shows the structure of the filter, including the DC offset cancellation (DCOC) loop at each stage. A six order filter is realized by cascading three bi-quads together. Each stage has an 18 dB gain range and the cutoff frequency is tunable. So the filter has a 54 dB gain range in total. Figure 2 shows a detailed schematic of a single bi-quad. All the resistor arrays and capacitor arrays are tunable. A classic network analysis of the bi-quad reveals the gain, cutoff frequency and Q factor, which could change by adjusting R_c, R_a and R_d, respectively. To maximize the in-band linearity performance, high-Q poles are assigned to the nearby zeros instead of remote zeros. Figure 3 shows the pole-zero pairing scheme. This kind of pole-zero pairing could minimize the amplitude peak of high-Q poles near the cutoff frequency. The bi-quads are ordered as the Q-factor gradually increases to maximize the in-band IIP3.

2.2. IIP3 optimization

Since passive resistors and capacitors can be very linear, the main cause of distortion in the bi-quad is the nonlinearity of OTAs. As will be shown below, the IIP3 and DC gain of the OTA determines the IIP3 of the bi-quad. The feedback path could also have an impact on the linearity performance. The Volterra series is usually used to analyze the linearity performance of a memory system[6], but it is cumbersome to simplify multiple feedback paths using SFG. In Refs. [7, 8], another useful analysis method was introduced and exemplified, but the discussions were mainly restricted to the scaling technique, which needs to scale all the elements using different scaling factors at the same time. In this paper, employing a similar approach, a procedure which is used in this design to maximize the IIIP3 of the bi-quad by normalizing all the passive element parameters to a reference resistance and capacitance when the IIP3 and DC gain of the OTA are fixed is developed.

Because of balance structure use, the second-order distortion of the bi-quad could be ignored. As shown in Fig. 4, two different kinds of transfer functions, which have been explained in Ref. [8], are used. H_{0j} is the transfer function from

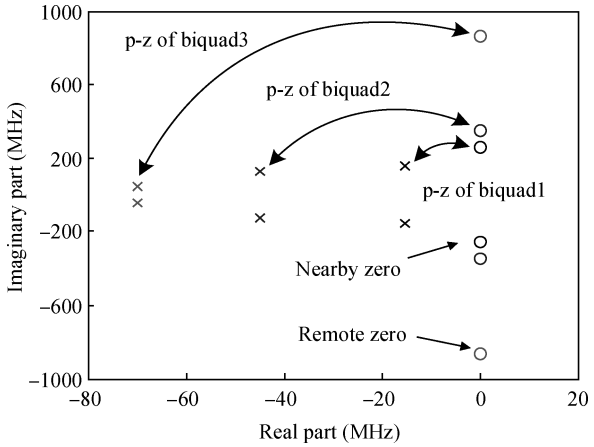


Fig. 3. Pole and zero pairing.

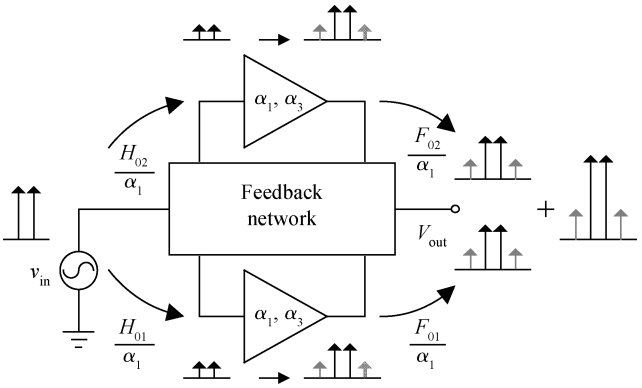


Fig. 4. The distortion analysis model.

the input of the bi-quad to the output of j th OTA, while F_{0j} is the transfer function from the input of j th OTA to the output of the bi-quad. In Fig. 4, the two-tone input and distortion impact of each OTA are shown. The total third-order intermodulation distortion (IMD3) product of the output is the sum of two distortion outputs from each OTA. This could be expressed like

$$\mathrm{IMD3} = \frac{v_{\mathrm{in}}^3}{\alpha_1^3 V_{\mathrm{IIP3,\,OTA}}^2}\left(H_{01}^3 F_{01} + H_{02}^3 F_{02}\right), \tag{1}$$

where $V_{\mathrm{IIP3,\,OTA}}$ is the IIP3 of OTA, and α_1 is the linear gain of OTA. IIP3 can be expressed as

$$\mathrm{IIP3} = V_{\mathrm{IIP3,\,OTA}}\sqrt{\frac{H_0\alpha_1^3}{H_{01}^3 F_{01} + H_{02}^3 F_{02}}}. \tag{2}$$

H_{01}, H_{02}, F_{01}, F_{02} are calculated using typical network circuit analysis. If we focus on the in-band IIP3, to simplify analysis, $\omega \approx \omega_{\mathrm{p}}$ is a reasonable assumption. In this case,

$$H_{01} \approx H_0\frac{R_{\mathrm{b}}}{R_{\mathrm{d}}}, \quad H_{02} \approx H_0,$$

$$F_{01} \approx 1 + H_0, \quad F_{02} \approx 1 + \frac{R_{\mathrm{d}}}{R_{\mathrm{b}}}.$$

Substitute these expressions into Eq. (7), and we get

$$\mathrm{IIP3} = \frac{V_{\mathrm{IIP3,\,OTA}}}{H_0}\sqrt{\frac{\alpha_1^3}{\left(\frac{R_{\mathrm{b}}}{R_{\mathrm{d}}}\right)^3(1+H_0) + \frac{R_{\mathrm{d}}}{R_{\mathrm{b}}} + 1}}. \tag{3}$$

Once the filter has been designed on a system level, all the parameters like ω_{p}, Q are fixed. This means that the product of R_{a}, R_{b}, C_1 and C_2 is constant. The minimum area of the capacitors and resistors is achieved when R_{a} is equal to R_{b} and C_1 equal to C_2. For simplifying the analysis, we set $C_1 = C_2 = C$. Using filter parameter expressions, R_{b} and R_{d} could be normalized to R_{a} and C, and expressed as

$$R_{\mathrm{b}} = \frac{1}{R_{\mathrm{a}}\omega_{\mathrm{p}}^2 C^2}, \tag{4}$$

$$R_{\mathrm{d}} = \frac{Q}{\omega_{\mathrm{p}} C}. \tag{5}$$

So IIP3 could be expressed like

$$\mathrm{IIP3} = \frac{V_{\mathrm{IIP3,\,OTA}}}{H_0}\times \sqrt{\frac{\alpha_1^3}{\left(\frac{1}{Q\omega_{\mathrm{p}}C}\right)^3\left(\frac{1}{R_{\mathrm{a}}}\right)^3(1+H_0) + Q\omega_{\mathrm{p}}CR_{\mathrm{a}} + 1}}. \tag{6}$$

This tells us that the IIP3 of the bi-quad could be improved by increasing the IIP3 of OTA, and the high gain of the filter means a low IIP3. Suppose OTA has maximum IIP3 and enough high DC gain at certain power consumption. The IIP3 of the filter could be improved further by optimizing the feedback loops, which means choosing proper passive element parameters in the feedback network. For a fixed C, if we set

$$R_{\mathrm{a}} = (3+3H_0)^{1/4}\frac{1}{\omega_{\mathrm{p}} QC}, \tag{7}$$

maximum IIP3 could be reached. But the optimal value could change if the filter operates under different gain modes. We focus on the low gain mode because the input signal strength is typically strong at this mode. In this case, H_0 equals 1. Thus, $R_{\mathrm{a,\,IIP3}} \approx 1.57/\omega_{\mathrm{p}} QC$.

Whether R_{a} could equal this value depends on other specifications. To found out the limitation on R_{a}, the noise characteristic also needs to be analyzed. The noise analysis model is shown in Fig. 5. R_{n} is the equivalent input noise resistor of the OTA. The total output noise of the bi-quad is

$$\overline{V_{\mathrm{n,\,out}}^2} \approx 4kTR_{\mathrm{a}}\left(2 + H_0 + \frac{1}{Q\omega_{\mathrm{p}}CR_{\mathrm{a}}}\right) + 4kTR_{\mathrm{n}}\left[(1+H_0)^2 + \left(\frac{1}{Q} + \omega_{\mathrm{p}}R_{\mathrm{a}}C\right)^2\right]. \tag{8}$$

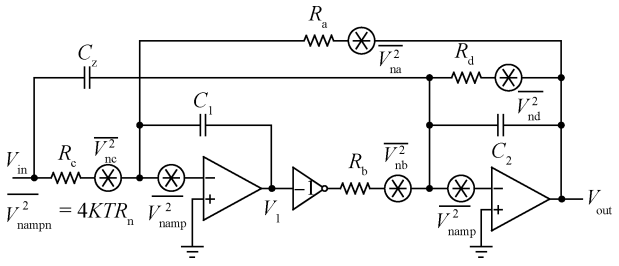


Fig. 5. The noise analysis model.

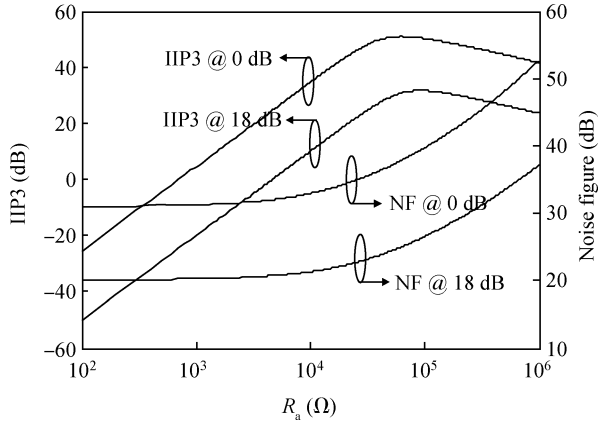


Fig. 6. The optimization of IIP3 and NF trade-off.

According to the definition of noise figure in Ref. [10], we get

$$\begin{aligned} \mathrm{NF} &= 1 + \frac{\overline{V_{\mathrm{n,in}}^2}}{4kTR_{\mathrm{s}}} \\ &\approx 1 + \frac{R_{\mathrm{a}}}{R_{\mathrm{s}}H_0^2}\left(2 + H_0 + \frac{1}{Q\omega_{\mathrm{p}}CR_{\mathrm{a}}}\right) \\ &\quad + \frac{R_{\mathrm{n}}}{R_{\mathrm{s}}H_0^2}\left[(1+H_0)^2 + \left(\frac{1}{Q} + \omega_{\mathrm{p}}R_{\mathrm{a}}C\right)^2\right]. \end{aligned} \quad (9)$$

Three indications are conveyed in this expression: (1) the noise contribution of R_{d} is individually decided by the filter and capacitance parameters; (2) R_{c} contributes more noise at high gain mode; and (3) the OTA noise could be dominant if its input equivalent noise is large enough.

To show the trade-off between IIP3 and NF, Figure 6 plots the relationship of NF and IIP3 with R_{a}. C could be chosen under chip area consideration. In this example, we set C = 3 pF. As is shown in the graph, the range of resistor values is determined by the specification of IIP3 at low gain and NF at high gain. If we choose R_{a} at the right side of the optimal value, IIP3 could be less sensitive to the variation in R_{a}, but the noise will be higher because of the larger value of R_{a}. Below the optimal value of R_{a}, IIP3 changes dramatically with R_{a} while the NF curve is relatively flat.

3. Circuit design

3.1. Band selection and gain adjustment

Since the cutoff frequency is determined by the RC product, if C remains constant, then different resistors refer to different cutoff frequencies. So, by switching resistors in the resistor array, the bandwidth of the filter could change from one to another. The first flaw in this method is that the number of bands is restricted by the number of resistors in the array, and the second is that it can only realize discrete frequency tuning. By adding a capacitor array as shown in Fig. 7, a mixed approach is employed in this design. The resistor array is used to select a center frequency, and by increasing or decreasing the number of unit capacitors in the capacitor array, the cutoff frequency could change around the center frequency. Thus, the cutoff frequency of the filter is continuously adjustable. This step is determined by the capacitance of the unit capacitor in the capacitor array. To maintain an elliptic frequency response shape, R_{b}, R_{c}, R_{d}, and C_{z} should change at the same time according to R_{a} and C.

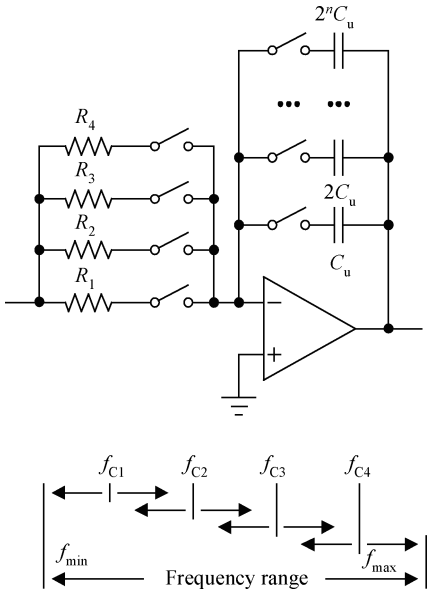


Fig. 7. The band selection and frequency tuning scheme.

Accuracy gain is desired to ensure that the auto gain control (AGC) loop is working correctly. As analyzed before, the gain of the bi-quad is determined by the ratio of the two resistors. R_{c} is chosen to change the gain of the bi-quad due to R_{c} having no influence on the cutoff frequency. As shown in Fig. 2, R_{c} is a resistor array with segmented resistors. The array operates synchronously with the switching of R_{a} to maintain an elliptic filter frequency response, while segmented resistors are used to change the gain of the bi-quad. Figure 8 shows the SFG of the bi-quad with a non-ideal integrator model. $A(\mathrm{j}\omega)$ is the open loop gain of OTA. Using SFG analysis, a more accurate expression of the bi-quad transfer function is given as

$$H_{\mathrm{r}}(s) = H_{0\mathrm{r}}\frac{1 + \dfrac{s}{\omega_{\mathrm{zr}}Q_{\mathrm{zr}}} + \dfrac{s^2}{\omega_{\mathrm{zr}}^2}}{1 + \dfrac{s}{\omega_{\mathrm{pr}}Q_{\mathrm{r}}} + \dfrac{s^2}{\omega_{\mathrm{pr}}^2}}. \quad (10)$$

Subscript r indicates the effective filter parameter differing from the ideal one. As explained in Ref. [9], gain and Q are more dependent on $A(\mathrm{j}\omega)$. The ratio of effective gain and Q

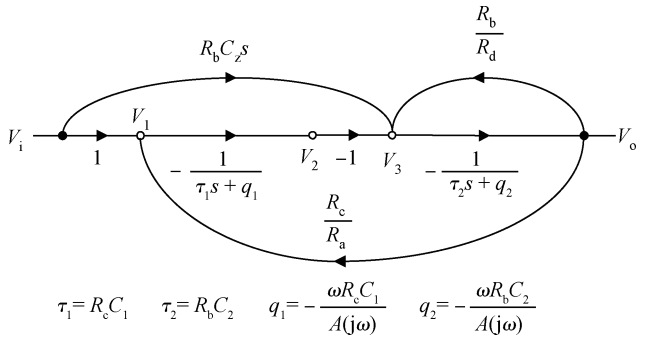


Fig. 8. The SFG of the bi-quad with a non-ideal integrator model.

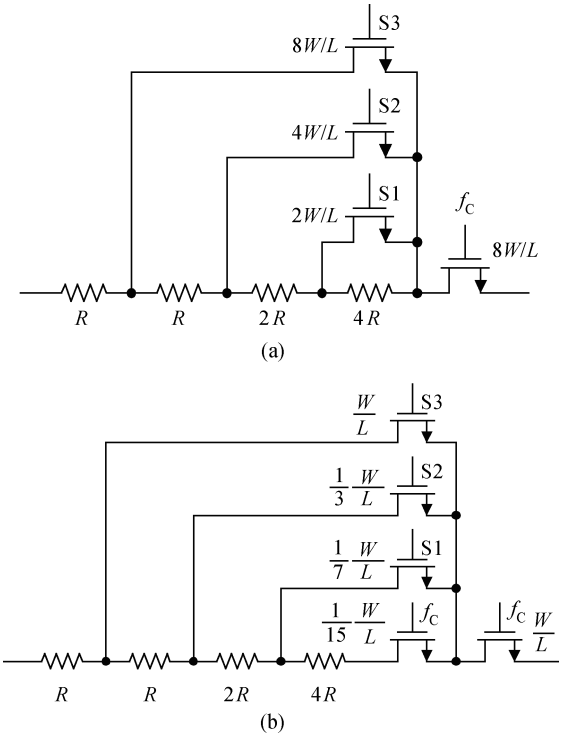


Fig. 9. The match scheme for small gain error. (a) The traditional method. (b) The proposed method.

are approximately expressed as

$$\frac{H_{0r}}{H_0} \approx \frac{1}{1-\dfrac{\omega}{Q\omega_p A(j\omega)}}, \tag{11}$$

$$\frac{Q_r}{Q} \approx \frac{1}{1-2H_0 Q\dfrac{\omega}{\omega_p A(j\omega)}}. \tag{12}$$

It is shown that only if the gain of OTA is large enough, can the gain of the bi-quad be treated as the ratio of the resistors. Thus, when the OTA has sufficient gain, the gain accuracy of the bi-quad is decided only by the match between the two resistors. Figure 9(a) shows a traditional segmented resistor with MOS transistors operating as switches. The MOS transistor can be treated as a resistor when it operates in the linear region. Thus, the gain should be the ratio between two equivalent resistances which include the output resistances of the transistors. For a fixed band, the value of equivalent R_a is constant.

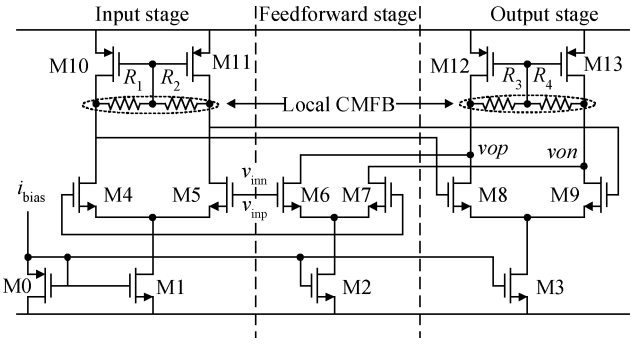


Fig. 10. Schematic of the feed-forward OTA.

An accurate 6 dB gain step should be achieved if the value of the effective R_c also has a binary property. But in Fig. 9(a), no matter what sizes of transistors are used, it is impossible to realize a binary effective R_c because of non-symmetry. On the contrary, by adding an additional switch and properly sizing, which is shown in Fig. 9(b), an effective R_c could have a binary property. Thus, the gain of the bi-quad has a slight error because the two effective resistances have a good match.

As the conclusion of non-ideal SFG analysis indicated, the phenomenon of non-ideal OTA deteriorates the Q-factor due to the finite gain and bandwidth product (GBW). A high-Q could cause a large ripple in the pass band of the filter[10], which is not desired. In high gain mode especially, the GBW is reduced due to heavy load. Noticing that the Q-factor is actually the ratio of two resistors that hardly vary, a reduced R_d at high gain mode could reduce the effective Q, which in turn compensates for the degradation due to finite GBW. So the resistors are constructed by segmented resistors in the array of R_d as shown in Fig. 2. By shorting or connecting segmented resistors, the effective R_d could change according to the gain mode of the bi-quad. The control code of this Q-tuning element comes from the gain control code. So no additional decoding circuit is needed.

3.2. Feed-forward OTA

OTA is the most important element in active RC filters. As explained before, an OTA with high gain, low noise and high linearity is needed. This is not only beneficial for improving IIP3 and gain accuracy, but also for lowering band ripple.

To reduce the total area of the filter, the use of extra capacitors such as Miller compensation capacitors and compensation capacitors for common mode feedback stability should be avoided in this design. A feed-forward OTA, which was introduced in Ref. [11], is applied. The schematic of this kind of OTA is shown in Fig. 10. Instead of pushing the dominant pole to a lower frequency, it creates a zero on the left plane in the s domain, which is beneficial for the phase margin and high bandwidth at low power. Local common mode feedback is completed using resistors as shown in the figure, and the OTA gain is limited by them. In Ref. [12], the low distortion benefit of this feed-forward OTA was discussed in detail by simulation. In this part, the theoretical analysis of distortion will be discussed in detail. The Volterra series is used again here to analyze the IIP3 of this OTA.

Figure 11 shows a differential pair of NMOS transistors. We use the model taking mobility degradation into account. i_d,

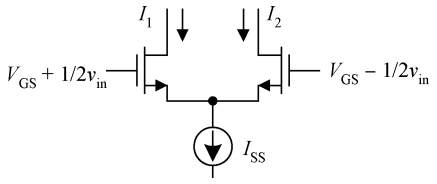


Fig. 11. The differential g_m unit.

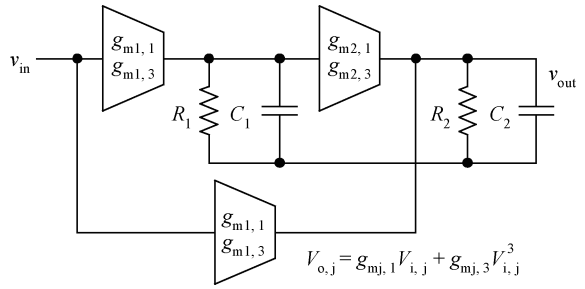


Fig. 12. The nonlinear model of OTA for distortion analysis.

the differential output current, could be expressed as

$$i_d = I_1 - I_2 = \frac{k\,(v_{GS1} - v_{th})^2}{1 + \theta\,(v_{GS1} - v_{th})} - \frac{k\,(v_{GS2} - v_{th})^2}{1 + \theta\,(v_{GS2} - v_{th})}$$
$$= \frac{k\left(V_{OV} + \dfrac{v_{in}}{2}\right)^2}{1 + \theta\left(V_{OV} + \dfrac{v_{in}}{2}\right)} - \frac{k\left(V_{OV} - \dfrac{v_{in}}{2}\right)^2}{1 + \theta\left(V_{OV} - \dfrac{v_{in}}{2}\right)}. \tag{13}$$

By Taylor expansion, i_d could be approximately expressed like

$$i_d \approx \frac{kV_{ov}\,(2 + \theta V_{OV})}{1 + \theta V_{OV}} v_{in} - \frac{1}{4}\frac{k\theta}{(1 + \theta V_{OV})^4} v_{in}^3$$
$$= g_{m1} v_{in} - g_{m3} v_{in}^3. \tag{14}$$

There is no second-order distortion because of balance application. Figure 12 is the model for distortion analysis including the nonlinear g_m model of each stage. The relationship between input and output is

$$v_{out} \approx G_{efft,1}\frac{\left(1 + \dfrac{s}{z_1}\right)}{\left(1 + \dfrac{s}{p_1}\right)\left(1 + \dfrac{s}{p_2}\right)} v_{in}$$
$$- G_{efft,3}\frac{\left(1 + \dfrac{s}{z_2}\right)}{\left(1 + \dfrac{s}{p_1}\right)\left(1 + \dfrac{s}{p_2}\right)} v_{in}^3, \tag{15}$$

where $p_1 = 1/R_1C_1$, $p_2 = 1/R_2C_2$, $z_1 = p_1(1 + g_{m1,1}g_{m2,1}R_1/g_{m3,1})$, $z_2 = p_1(1 + (g_{m1,3}g_{m2,1}R_1 + g_{m1,1}^3 g_{m2,3}R_1)/g_{m3,3})$, are the poles and zeros. $G_{efft,1} = (g_{m1,1}g_{m2,1}R_1 + g_{m3,1})R_2$ is the equivalent linear gain, and $G_{efft,3} = (g_{m1,3}g_{m2,1}R_1 + g_{m1,1}^3 g_{m2,3}R_1 + g_{m3,3})R_2$ is the third-order gain factor. IIP3 could expressed as

$$\text{IIP3} \approx \sqrt{\frac{4}{3}\frac{G_{efft,1}}{G_{efft,3}}}$$
$$= \sqrt{\frac{4}{3}\frac{g_{m1,1}g_{m2,1}R_1 + g_{m3,1}}{g_{m1,3}g_{m2,1}R_1 + g_{m1,1}^3 g_{m2,3}R_1 + g_{m3,3}}}. \tag{16}$$

For phase compensation, z_1 is close to p_2, which can be far away from the dominant pole p_1. Assume

$$g_{m1,1}g_{m2,1}R_1 + g_{m3,1} = \xi g_{m3,1}, \quad \xi > 1.$$

Thus,

$$\text{IIP3} = \sqrt{\frac{4}{3}\frac{1}{\dfrac{g_{m1,3}}{g_{m1,1}}\dfrac{\xi - 1}{\xi} + g_{m1,1}^2\dfrac{g_{m2,3}}{g_{m2,1}}\dfrac{\xi - 1}{\xi} + \dfrac{1}{\xi}\dfrac{g_{m3,3}}{g_{m3,1}}}}. \tag{17}$$

It seems that if the zero is designed to compensate for the dominant pole, which will make ξ equal to 1, then the distortion of g_{m1} and g_{m2} could be minimized. This is not practical because it will consume infinite power to make g_{m3} become infinite. But increasing g_{m3} without exceeding the power limit is good for reducing the distortion of g_{m1} and g_{m2}.

There are three indications: (1) if p_2 is far enough away from p_1, then zero compensation for p_2 is power economical. Distortion of the first stage is dominant in this case. (2) To lower the influence of second-stage distortion, $g_{m1,1}$, which is the linear transconductance of the first stage, should not be too large. (3) If p_1 and p_2 are not far away, designing the created zero to be located between the dominant pole and the non-dominant pole could compromise the power consumption and distortion reduction of g_{m1} and g_{m2}, and this may make the distortion of g_{m3} dominant.

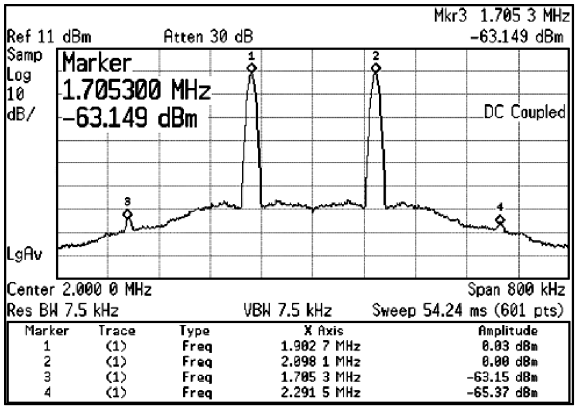
From the previous analysis in this section, we have

$$\frac{g_{mj,3}}{g_{mj,1}} = \frac{\theta}{4V_{ov}\,(2 + \theta V_{OV})\,(1 + \theta V_{OV})^3}. \tag{18}$$

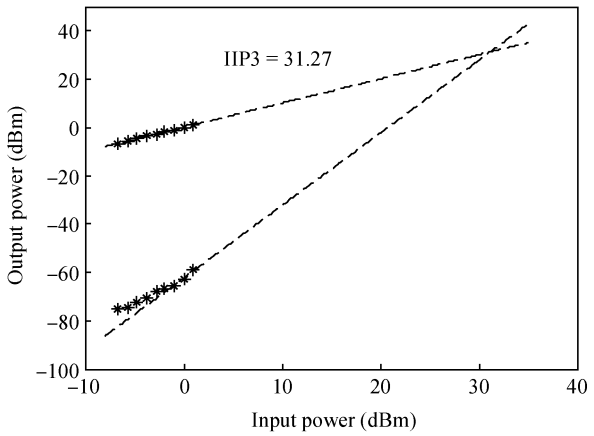
So, the increase over the drive voltage is a direct way to reduce the distortion of each g_m stage.

3.3. Others

The variation in on-chip resistors and capacitors are detected by an on-chip RC time constant detector, which is then calibrated by an auto-RC tuning engine to ensure an accurate cutoff frequency that meets the application requirements. A traditional analog DC feedback method is used to cancel the DC offset[14]. But to achieve a low high-pass corner frequency and minimize the area of capacitors required at the same time, a multiple DCOC loop strategy is adopted here. The feedback network senses the DC voltage at the output of the bi-quad and then feeds back current to the resistors in the bi-quad. Thus, a voltage in the opposite phase is generated to cancel the input offset voltage.



(a)



(b)

Fig. 13. In-band IIP3 test. (a) In-band two-tone test. (b) Extrapolated IIP3.

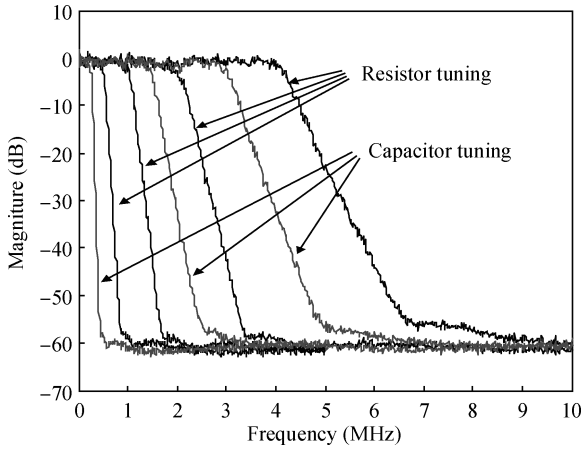
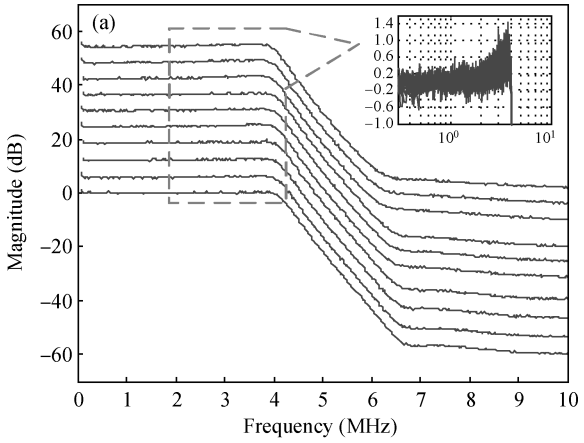


Fig. 14. The band selection of the filter.

4. Test results

Figure 13(a) illustrates the two-tone test result when the gain is set at 0 dB. The in-band IIP3 is 31.27 dBm for 1.9 MHz and 2.1 MHz tones. Figure 13(b) is the extrapolated IIP3 graph from different input and output test results.

Figure 14 shows the band-selection function of this filter. The four dark traces are the bands selected by switching resistors, while the blue traces are the bands tuned using capacitor arrays. The frequency tuning range is from 0.25 to 4 MHz. By comparing the –3 dB point with designed cutoff frequency, the automatic tuning accuracy could be evaluated. Data from the traces shows that a frequency tuning error of less than 5% could be reached.



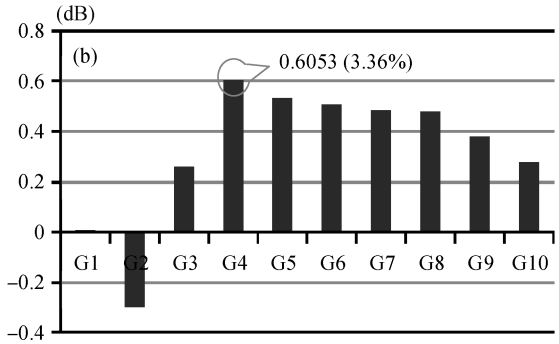


Fig. 15. The gain step test. (a) Gain range and magnified ripple detail, and (b) gain error.

Table 1. Performance summary.

Parameter	Value
Technology	0.18 μm CMOS
Die area	1×1.28 mm^2
Power consumption @1.8V	12.6 mW
Gain range/Gain step	54 dB/6 dB
Bandwidth tuning range	0.250–4 MHz
Gain error	$< 3.4\%$
Cutoff frequency error	$< 5\%$
DC offset @ 54 dB gain	12 mV
Attenuation @ 1.315 f_c/stop band	35 dB/60 dB
In-band ripple	< 1.4 dB
In band IIP3 @ 0 dB gain	> 31 dBm

Figure 15(a) shows the gain range, which could vary from 0 to 54 dB. The attenuation at 1.315 times the cutoff frequency and stop band could reach 35 dB and 60 dB, respectively. To show the details of the ripples, the frequency response traces, posted in the upper right of Fig. 15(a), are magnified and normalized by subtracting the average gain of each gain mode. All the normalized traces meet together at high frequency in the graph, which indicates that this normalization method is right because gain error is excluded. It is shown that the biggest ripple is less than 1.4 dB. In Fig. 15(b), the gain errors of each gain mode are shown. The most significant one has a difference of

Table 2. Comparison to recently published work.

	Process (nm)	Type	Order	V_{dd} (V)	Power/Pole (mW/Pole)	$f_{cut\text{-}off}$ range (MHz)	IIP3 (dBm)	Gain (dB)	Ripple (dB)	Continuously tuning	DCOC Included
Ref. [4]	130	B/C	4	1.2	1.36	0.28–3	29	0–18	—	Yes	Yes
Ref. [10]	130	C/I	1/3/5	1	0.6–1.5	1–5	31.3	0	—	Yes	No
Ref. [12]	180	Elliptic	3	1.8	0.6	8.5	30.8	0	2.2	No	No
This work	180	Elliptic	6	1.8	1.05	0.25–4	31.27	0–54	1.4	Yes	Yes

B indicates Butterworth, while C and I indicate Chebyshev and Inverse-Chebyshev, respectively. The topologies used in these papers are all active-RC. IIP3 is the in-band IIP3.

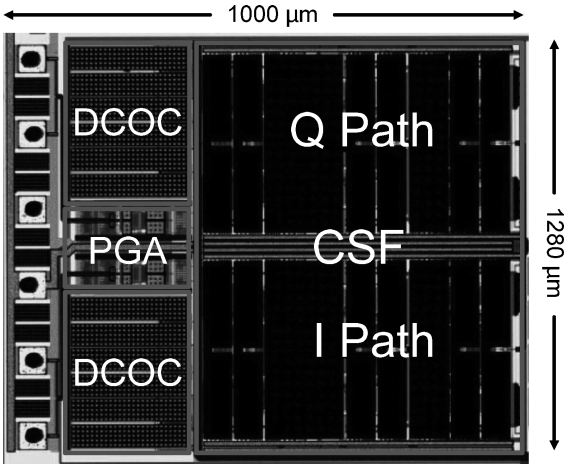


Fig. 16. The die photo.

0.6053 dB with the designed value, which means that the gain error is less than 3.4%. The performance of this filter, including the DCOC and auto-RC tuning circuit, is summarized in detail in Table 1. A comparison to recently published work is shown in Table 2. The proposed filter with a steeper transient band or better band selection due to higher order has high linearity performance, which is comparable to the best results listed in Table 2: multi-band selection with continuous frequency tuning, wide gain range with small gain error, and small in-band ripple. Figure 16 is the die photo. The channel-select filter has I and Q paths.

5. Conclusion

This paper develops a bi-quad IIP3 optimization procedure by normalizing passive element parameters to a reference resistor. Detailed theoretical analysis can be used in the design of this particular channel-select filter, and other kinds of filter as well. The gain error control method and frequency tuning scheme are also presented. To overcome in-band ripples originating from the degradation of the effective Q-factor, a segmented resistor technique is introduced. Test results show that the filter, which is suitable for TV-tuner application, has more than 31 dBm in-band IIP3 at a low gain mode and 54 dB gain range with a gain error of less than 3.4%. The frequency tuning range covers signal bands of all the applications from 0.25 to 4 MHz with a frequency tuning error of no more than 5%.

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References

[1] Namgoong W, Meng T H. Direct-conversion RF receiver design. IEEE Trans Commun, 2001, 49: 518
[2] Chang J H, Kim H, Choi J H, et al. A multistandard multiband mobile TV RF SoC in 65 nm CMOS. IEEE ISSCC Dig of Tec Papers, 2010: 462
[3] Antoine P, Bauser P, Beaulaton H, et al. A direct-conversion receiver for DVB-H. IEEE J Solid-State Circuits, 2005, 40(12): 2536
[4] Wang W, Chang X, Wang X, et al. A 4th-order reconfigurable analog baseband filter for software-defined radio applications. Journal of Semiconductors, 2011, 32(4): 045008
[5] Zou L, Liao Y, Tang Z. An eighth order channel selection filter for low-IF and zero-IF DVB tuner applications. Journal of Semiconductors, 2009, 30(11): 115002
[6] Wambacq P, Sansen W M C. Distortion analysis of analog integrated circuits. Springer, 1998
[7] Palaskas Y, Tsividis Y. Dynamic range optimization of weakly nonlinear, fully balanced, G_m–C filters with power dissipation constraints. IEEE Trans Circuits Syst II: Analog and Digital Signal Processing, 2003, 50(10): 714
[8] Meghdadi M, Bakhtiar M S. Analysis and optimization of SFDR in differential active-RC filters. IEEE Trans Circuits Syst I: Regular Papers, 2012, 59(6): 1168
[9] Schaumann R, the late Valkenburg M E V. Design of analog filters. Oxford University Press, USA, 2001
[10] Amir-Aslanzadeh H, Pankratz E J, Sanchez-Sinencio E. A 1-V +31 dBm IIP3, reconfigurable, continuously tunable, power-adjustable active-RC LPF. IEEE J Solid-State Circuits, 2009, 44(2): 495
[11] Harrison J, Weste N. A 500 MHz CMOS anti-alias filter using feed-forward op-amps with local common-mode feedback. IEEE ISSCC Dig Tec Papers, 2003: 132
[12] Krishnapura N, Agrawal A, Singh S. A High-IIP3 third-order elliptic filter with current-efficient feedforward-compensated opamps. IEEE Trans Circuits Syst II: Express Briefs, 2011, 58(4): 205
[13] Mak P I, Seng-Pan U, Martins R P. On the design of a programmable-gain amplifier with built-in compact DC-offset cancellers for very low-voltage WLAN systems. IEEE Trans Circuits Syst I: Regular Papers, 2008, 55(2): 496