A 2-to-2.4-GHz differentially-tuned fractional-*N* frequency synthesizer for DVB tuner applications*

Meng Lingbu(孟令部), Lu Lei(卢磊), Zhao Wei(赵薇), and Tang Zhangwen(唐长文)†

(State Key Laboratory of ASIC & System, Fudan University, Shanghai 201203, China)

Abstract: This paper describes the design of a fractional-*N* frequency synthesizer for digital video broadcasting-terrestrial (DVB-T) receivers. Transfer functions in differentially-tuned PLL are derived and loop parameters are designed. In addition, a fully-differential charge pump is presented. An 8/9 high speed prescaler is analyzed and the design considerations for the CML logic are also presented. Test results show that the RMS phase error is less than 0.7° in integer-*N* mode and less than 1° in fractional-*N* mode. The implemented frequency synthesizer draws 10 mA from a 1.8-V supply while occupying a die area of about 1-mm^2 in a 0.18-μm CMOS process.

Key words: frequency synthesizer; fully-differential; phase noise; charge pump
DOI: 10.1088/1674-4926/31/7/075007 **EEACC:** 1270

1. Introduction

The fast growing market of digital video broadcasting has driven much research towards the development of high-performance low-cost silicon tuners. This is especially true when referring to the implementation of highly integrated and low phase noise RF frequency synthesizers. DVB tuners with double conversion architecture need a wide range frequency synthesizer to cover the whole tuning range as well as a narrow-band frequency synthesizer to down-convert the target signal band[1, 2]. The synthesizer should fulfill a stringent phase noise requirement over the entire tuning range and have a fast locking time. Usually a fractional-*N* synthesizer[3] is adopted because the fractional-*N* synthesizer can avoid some intrinsic limitations of the integer-*N* synthesizer. The main one is that the output frequency resolution has to be equal to a multiple of the reference frequency. If a finer frequency resolution is needed, a lower reference frequency has to be used. This makes the loop bandwidth small because it must be much lower than 1/10 of the reference frequency to keep loop stable[4]. The consequence of the narrow bandwidth is that PLL locking is very slow. Moreover, a low reference frequency needs a high feedback division ratio *N* to synthesize the desired output frequency range, thus causing a strong degradation of in-band phase noise[5]. Fractional-*N* synthesizers can solve the problems mentioned above and achieve fast locking, potentially arbitrary output frequency resolution, and more freedom in the reference oscillator choice[6].

Differentially-tuned synthesizers are area-efficient and effectively suppress the common-mode noise compared to their single-ended tuned counterparts[7]. However, the closed-loop characteristics in differentially-tuned synthesizer are relatively complicated since both the charge pump and the loop filter have two equal branches. The transfer function becomes not straightforward. In this paper the closed-loop transfer functions of the differentially-tuned synthesizers are derived and are analyzed in detail. The transfer functions and phase noise contribution are the same as single-end tuned frequency synthesizers except that the thermal noise of resistors in loop filter doubles their phase noise contribution to the PLL output. But by choosing proper loop parameters the noise deterioration from the loop filter can be lowered and is not of much concern. This makes the differentially-tuned frequency synthesizers desirable where stringent phase noise and small area requirements are needed.

The paper is organized as follows. In section 2, open loop and closed-loop transfer functions for differentially-tuned frequency synthesizers are derived and compared to their single-ended tuned counterparts. Section 3 shows the detailed circuits design, including fully-differential charge pump, high speed 8/9 prescaler and other blocks. Section 4 gives some measurement results, such as phase noise, RMS phase error and reference spurs at different output frequencies. The last section draws some conclusions.

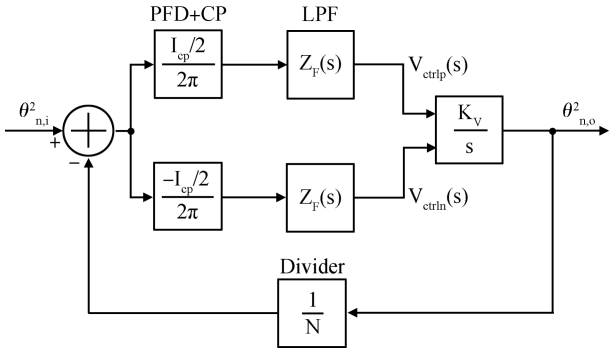

Fig. 1. Simplified block diagram for differentially-tuned frequency synthesizer.

* Project supported by the National Natural Science Foundation of China (No. 60876019), the National S&T Major Project of China (No. 2009ZX0131-002-003-02), the Shanghai Rising-Star Program, China (No. 09QA1400300), and the National Scientists and Engineers Service for Enterprise Program, China (No. 2009GJC00046).

† Corresponding author. Email: zwtang@fudan.edu.cn

Received 4 January 2010, revised manuscript received 24 February 2010 © 2010 Chinese Institute of Electronics

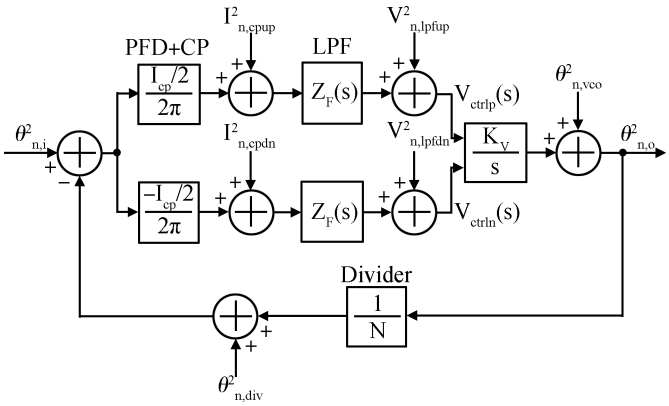

Fig. 2. Noise model for differentially-tuned frequency synthesizer.

2. Loop dynamics analysis

2.1. Open loop transfer function

Figure 1 shows a simplified block diagram for differentially-tuned frequency synthesizer, where I_{CP} is the charge pump current, N is the division ratio, K_V is the VCO tuning gain, and $Z_F(s)$ is the loop filter transfer function. The current of charge pumps I_{CP} decreases to a half in each branch since the charge pump current is split into two equal parts for the differentially-tuned frequency synthesizer. The relationship between output frequency phase $\theta_{n,o}$ and input frequency phase $\theta_{n,i}$ can be expressed as:

$$\left[\left(\theta_{n,i}-\frac{\theta_{n,o}}{N}\right)\frac{I_{CP}/2}{2\pi}Z_F(s)-\left(\theta_{n,i}-\frac{\theta_{n,o}}{N}\right)\frac{-I_{CP}/2}{2\pi}Z_F(s)\right]\times K_V/s=\theta_{n,o}. \quad (1)$$

The open loop transfer function for the differentially-tuned frequency synthesizer is:

$$H_o(s)=\frac{\theta_{n,o}}{\theta_{n,i}}=\frac{I_{CP}}{2\pi}\frac{1}{N}\frac{K_V}{s}Z_F(s). \quad (2)$$

Although differentially configured, the open loop transfer function is the same as that for the single-ended tuned frequency synthesizers.

2.2. Noise transfer function

Figure 2 shows the noise model for differentially-tuned frequency synthesizer, where $\theta^2_{n,i}$ and $\theta^2_{n,div}$ are phase noise from reference clock and frequency divider respectively, $I^2_{n,cpup}$ and $I^2_{n,cpdn}$ are charge pump output current noise from up and down braches respectively, while $V^2_{n,lpfup}$ and $V^2_{n,lpfdn}$ are voltage noise from up and down loop filters.

Obviously, the noise transfer functions from the divider and VCO to PLL output are the same as those for the single-ended tuned frequency synthesizer. The noise transfer functions from charge pump and loop filter will be derived. Only taking charge pump current noise $I^2_{n,cpup}$ into consideration, the following equation holds:

$$\left[\left(\frac{-\theta_{n,o}}{N}\frac{I_{CP}/2}{2\pi}+I_{n,cpup}\right)Z_F(s)-\frac{-\theta_{n,o}}{N}\frac{-I_{CP}/2}{2\pi}Z_F(s)\right]\times K_V/s=\theta_{n,o}. \quad (3)$$

The current noise transfer function from the charge pump output to the PLL output can be found as:

$$H_{CP}(s)=\frac{\theta_{n,o}}{I_{n,cpup}}=\frac{2\pi N}{I_{CP}}\frac{H_o(s)}{1+H_o(s)}. \quad (4)$$

For the loop filter, only taking voltage noise $V^2_{n,lpfup}$ into consideration. Another equation follows:

$$\left[\frac{-\theta_{n,o}}{N}\frac{I_{CP}/2}{2\pi}Z_F(s)+V_{n,lpfup}-\frac{-\theta_{n,o}}{N}\frac{-I_{CP}/2}{2\pi}Z_F(s)\right]\times K_V/s=\theta_{n,o}. \quad (5)$$

The voltage noise transfer function from loop filter to the PLL output can be obtained as:

$$H_{LPF}(s)=\frac{K_V/s}{1+H_o(s)}. \quad (6)$$

Comparing the derived transfer functions for differentially-tuned frequency synthesizer with these for single-ended tuned one[5], it can be found that transfer functions for both architectures are all the same.

The noise transfer function from charge pump output to PLL output can be expressed as:

$$\theta^2_{n,o,cp}=(I^2_{n,cpup}+I^2_{n,cpdn})\left[\frac{2\pi N}{I_{CP}}\frac{H_o(s)}{1+H_o(s)}\right]^2. \quad (7)$$

The noise transfer function from loop filter to PLL output can be expressed:

$$\theta^2_{n,o,lpf}=(V^2_{n,lpfup}+V^2_{n,lpfdn})\left[\frac{K_V(s)}{1+H_o(s)}\right]^2. \quad (8)$$

For the charge pump in the differentially-tuned frequency synthesizer, it has two equal two parts and each part is half that in single-ended frequency synthesizer. The output current noise $I^2_{n,cpup}$ and $I^2_{n,cpup}$ are equal and thus equal to the charge pump output current noise in the single-ended frequency synthesizer. So although configured differentially, the charge pump noise contribution for the differentially-tuned frequency to the PLL output, as shown in Eq. (7), is the same as the that for the single-ended frequency synthesizers.

For the loop filter, as will be shown in section 3, the loop filter in the differentially-tuned frequency synthesizer has two equal parts. Each part is equal to that for the single-ended frequency synthesizer. So the thermal noise from the resisters in the loop filter doubles. As a result, as Equation (8) indicates, the phase noise contribution from the loop filter to PLL output is twice that for the single-ended frequency synthesizer.

Figures 3 and 4 show the behavior simulation of settling time and phase noise respectively in this design. The thermal noise from loop filter is effectively suppressed through the PLL closed loop. Its phase noise contribution to PLL output is lower than VCO near the loop bandwidth.

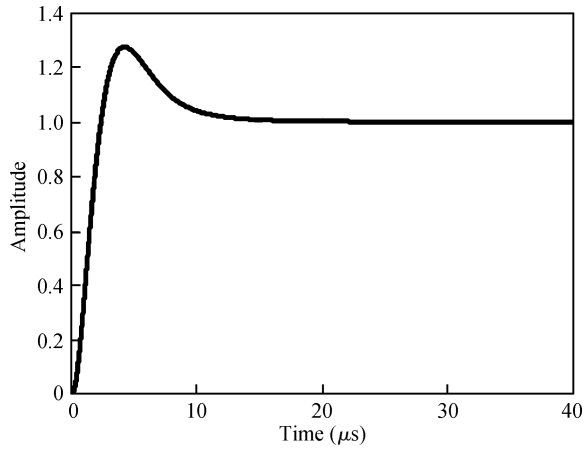

Fig. 3. PLL locking time simulation.

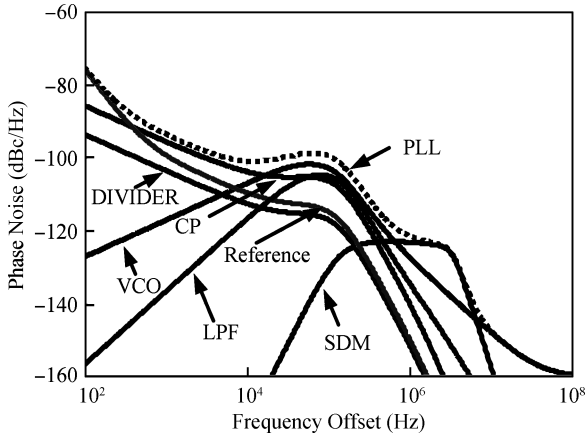

Fig. 4. PLL phase noise simulation.

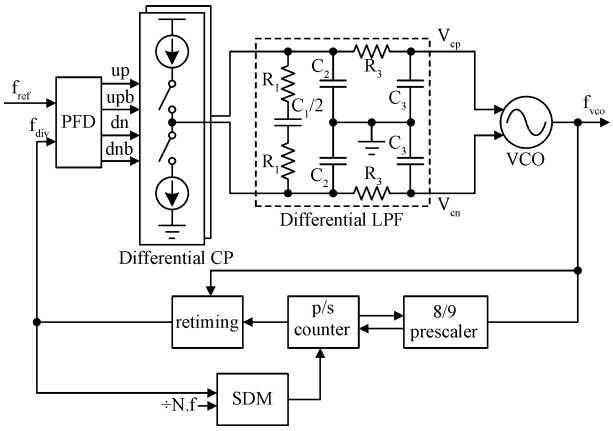

Fig. 5. Block diagram of the 2–2.4 GHz fractional-N frequency synthesizer.

3. Circuit design

The presented 2–2.4 GHz differentially-tuned fractional-N frequency synthesizer is shown in Fig. 5. For this differentially-tuned architecture, the big capacitor C_1 in loop filter is exactly half that in single-ended frequency synthesizer so that the loop filters transfer function keep unchanged compared with that in single-ended architecture. By this way the loop filter can be easily integrated. A conventional tri-state deadzone free phase-frequency detector (PFD) is employed here. The charge pump with common-mode feedback is also differential and can achieve excellent current match. Programmed P/S counters and 8/9 prescaler is used for the multi-modulus divider to obtain the desired division ratio. A retiming circuit is used to lower the phase noise from the divider.

3.1. Charge pump

Charge pump with high linearity is desirable in the CP-PLL. The nonideal effects such as leakage current and the current mismatch can cause not only the deterioration of the reference spur but also degradation of in-band phase noise in fractional-N mode. Fully-differential charge pump is often prior in that it achieves a higher linearity. Additionally, differential charge pump can effectively suppress the common-mode noise from the power supply and substrate.

A modified fully-differential charge pump from Ref. [8] is shown in Fig. 6. The positive and negative branches of the fully-differential charge pump are the left and right circuits respectively. For simplicity, only the positive circuit is considered. Transistors M1, M3, M6, M9 compose a replica circuit. M4 and M7 are switches which control whether the charge pump is open or not. The additional MOS branches composed by transistors M5 and M8 and the added capacitance C_s are combined to stabilize the common source nodes A and C. Operational amplifier A1 is configured as buffer to ensure M5 and M8 working properly when charge pump is closed. By using an error amplifier A3, the voltage V_{OPC} follows the voltage V_{OP}. If $(W/L)_1 = (W/L)_2$, $(W/L)_3 = (W/L)_4$, $(W/L)_6 = (W/L)_7$ and $(W/L)_9 = (W/L)_{10}$, current flowing through M3 will be equal to that flowing through M4 and because the transistor in the two path are matched. At the same time, current flowing through M6 will be equal to that flowing through M7. So the sinking current equals the sourcing current. In this way, current matching characteristics can be obtained regardless of the variation of output controlling voltages.

All of the transistors except the dummy transistors (M11–M14) work in the saturation region. One notable advantage is that transistors working in the saturation region are of smaller gate-to-drain capacitance C_{gd} than transistors working in the linear region; another advantage is that the saturation transistors have a faster speed. The operational amplifiers in the charge pump only need a bandwidth comparable with the loop bandwidth of the PLL so as to respond in time to the variation at the output nodes. What is more, the load of these operational amplifiers is only the parasitic capacitance of the transistors which is quite small. As a result, the four operational amplifiers employed in the charge pump consume only limited power.

The signals from PFD toggle between VSS and VDD and are not suitable to switch these transistors working in saturation region directly. Thus a level shift is needed to convert the rail-to-rail signals from PFD output to the targeted analog signals. Figure 7 illustrates the simplified partial level shift circuits used in the charge pump. After the level shift the analog control signals can be obtained. Besides, the switches in the level shift are connected to a moderate resistance so as to make the complementary control signals UP, UP– more symmetrical so as to effectively reduce the high speed glitch[8].

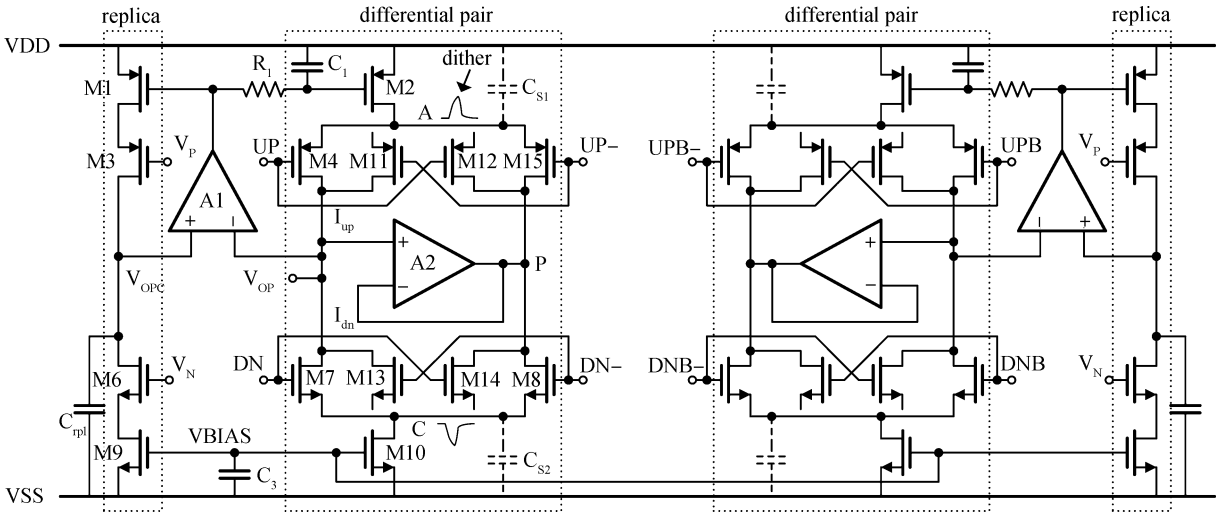

Fig. 6. Fully-differential charge pump without common-mode feedback.

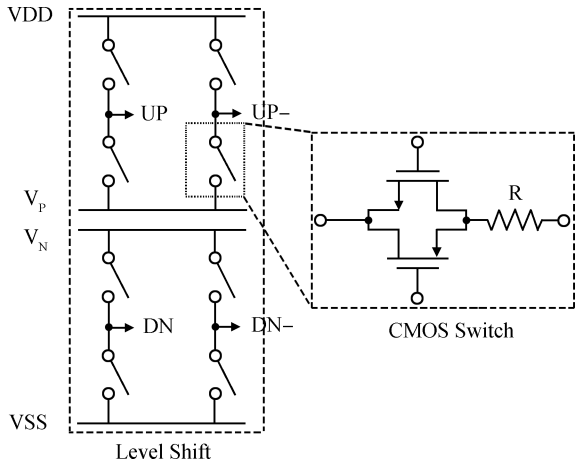

Fig. 7. Level shift and switch.

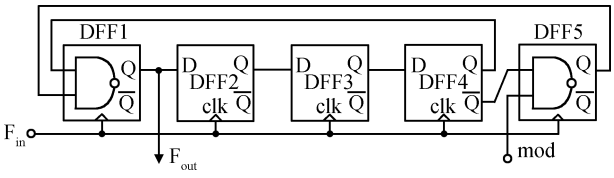

Fig. 8. High speed synchronous 8/9 prescaler diagram.

3.2. Prescaler

For the high speed prescaler, both synchronous and asynchronous architectures can be adopted. A synchronous 8/9 prescaler[6] is used in this design and is shown in Fig. 8. When mod is 0, DFF5 is disabled, the prescaler works in divide-by-8 mode. When mod is high, it works in the divide-by-9 mode. Compared to the asynchronous 8/9 prescaler, the NAND logic can be easily incorporated in the current mode logic (CML) latch.

Figure 9 shows the CML D-flip-flop schematic which incorporates the NAND logic. Four NMOS transistors are emerged in the first latch to incorporate the NAND logic. The tail current sources are eliminated to increase its operation speed. Inside each latch, a differential transistor pair (M5 and M6, M13 and M14, M9 and M10) charges and discharges its output nodes. The gate capacitance of these transistors adds to the load of the latch. Operation speed and power consumption of the flip-flop are determined by the transistors sizes and load resistance. Since the operation speed is decided by the time taken for the current to charge the output nodes, the circuit speed directly depends on the current through the stage. Increasing the currents would require reduction in load resistance to maintain swing and thus increase in NMOS device sizes. The increase in the device size implies a proportional increase in parasitic capacitances. Therefore, the above two variations cancel out the effect of higher current on speed improvements. Thus for a given process and voltage swing the maximum operation speed is only limited by the parasitic capacitance. So all metal interconnects are as short as possible especially the lines between the master outputs and slave inputs. High resistivity polysilicon resistors without a silicide layer are used as the load to reduce the size and thus parasitic capacitance. In order to tolerate process, voltage, and temperature variation, the input sensitivity of the prescaler leaves a sufficient margin.

3.3. Other blocks

To meet the stringent phase noise requirements, LC VCO is used for its potential to achieve superior phase noise performance[9]. For the presented frequency synthesizer, the 2–2.4 GHz tune range can result in an excessively high tuning sensitivity K_V. In practice, this is undesirable since the voltage-controlled nodes introduce substantial noise originating from preceding block especially the thermal noise from the resistors in the loop filter mentioned in section 2. Also noise on the voltage-controlled nodes appears across the varactors and modulates the device junction capacitance, resulting in phase noise deterioration. To solve these problems, the targeted frequency range is split into 64 sub-bands by means of a switched varactors array[6]. The varactors are digitally selected and driven by the loop control voltage. This split is useful to reduce the VCO gain associated with the analog control voltage, thus lowering the sensitivity to noise appearing on the voltage-controlled nodes.

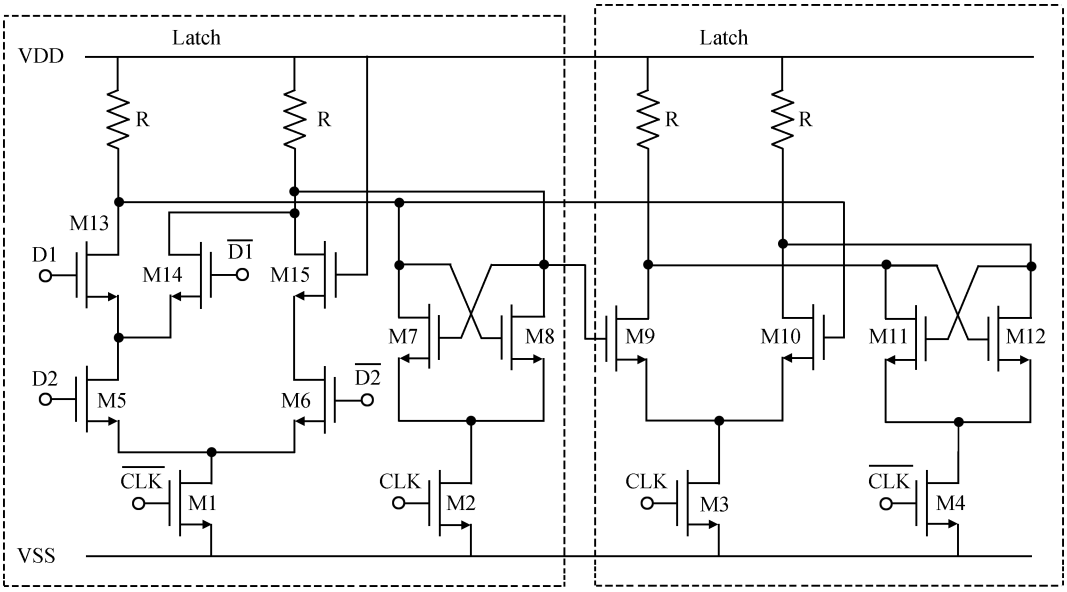

Fig. 9. "NAND" embedded CML D-flip-flop.

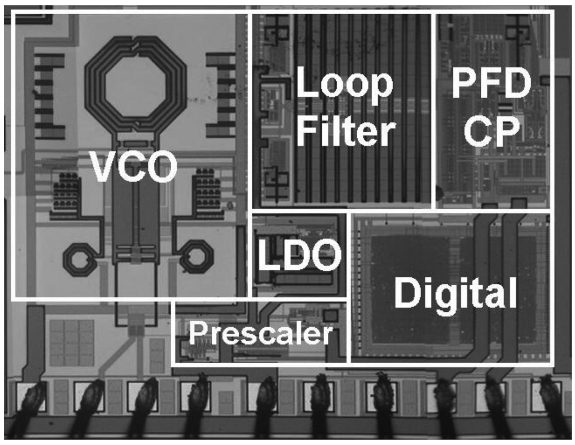

Fig. 10. Die photograph.

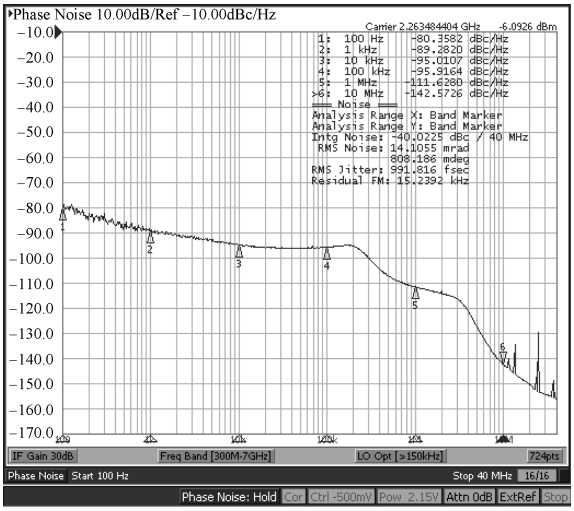

Fig. 11. Measured phase noise at an oscillation frequency of 2.26 GHz.

Single-stage multiple feed forward SDM is adopted here[10]. Fewer output levels of SDM are preferred so as to lower the in-band phase noise deterioration through noise folding by quantization noise going through analog blocks with non-linearity.

4. Experimental results

The frequency synthesizer was fabricated in SMIC 0.18-μm CMOS technology. The chip microphotograph is shown in Fig. 10. The die area of the frequency synthesizer is about 1.2 $\times$ 0.8 mm^2.

Operating at 2.2 GHz, the frequency synthesizer draws 10 mA from 1.8-V supply. The measured loop bandwidth is approximately 100 kHz. The measured phase noise plots for the frequency synthesizer are shown in Fig. 11. In-band phase noise at 10 kHz offset is –95 dBc/Hz and at 1 MHz offset the measured phase noise is −111 dBc/Hz. The integrated RMS phase error is 0.8°. Figure 12 shows the measured RMS phase error integrated from 100 Hz to100 MHz in both fractional-N mode and integer-N mode respectively. The RMS phase error is less than 0.7° in integer-N mode and less than 1° in fractional-N mode across the overall tuning range. Table 1 lists the performance comparison with other frequency synthesizers for tuner applications. Comparing with other frequency synthesizers for tuners applications, the presented frequency synthesizer achieves superior phase noise performance and low power consumption.

Figure 13 shows the measured power spectrum density (PSD) of the oscillation amplitude at 2.3 GHz; the reference spur is –66 dBc. Figure 14 shows the reference spurs at different output frequencies. The reference spur is less than –63 dBc in across the overall tuning range.

5. Conclusion

A fractional-N frequency synthesizer for DTV tuner applications has been presented in this paper. Transfer func-

Table 1. PLL performance comparison.

Reference	Ref. [11]	Ref. [12]	Ref. [13]	This work
Technology	0.13-μm CMOS	0.11-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Application	DVB-S	ISDB-T	DVB-T	DVB-T
Tuning type	Single-ended	Single-ended	Single-ended	differential
Loop bandwidth (kHz)	1000	100	100	100
Output frequency (GHz)	2.24–4.48	1.5–3.78	1.1–2.2	2–2.4
Phase noise (dBc/Hz)	–98 @ 100 kHz –100 @ 1 MHz	–88 @ 10 kHz –118 @ 1 MHz	–90 @ 10 kHz –90 @ 10 kHz	–95 @ 10 kHz –111 @ 1 MHz
RMS phase error (°)	0.8	NA	1.5	0.8
Power consumption (mW)	132	20	NA	18
Chip size (mm^2)	0.3	1.9	1.2	1

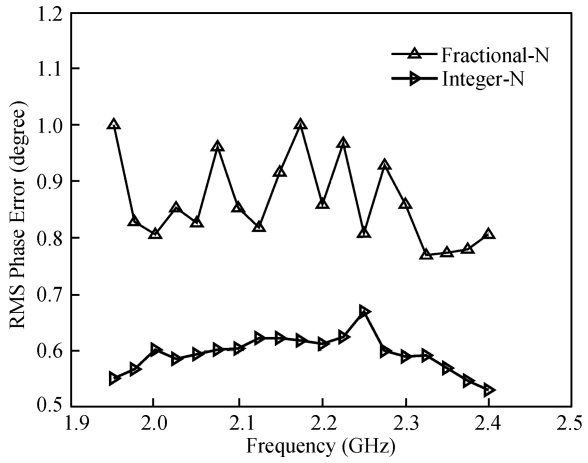

Fig. 12. RMS phase error (integrated from 100 Hz to 100 MHz).

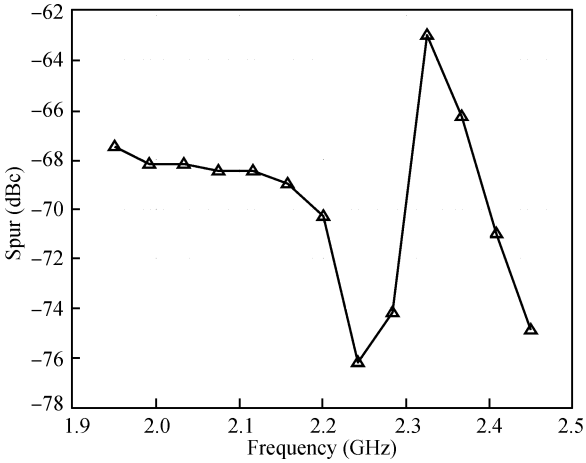

Fig. 14. Reference spurs at different output frequencies.

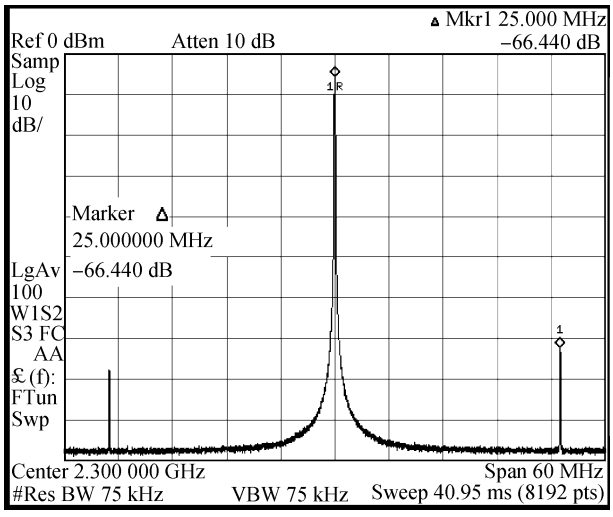

Fig. 13. Measured power spectrum density (PSD) of the oscillation amplitude at 2.3 GHz.

tions for the differentially-tuned frequency synthesizer are derived. The loop filter doubles their phase noise contribution in differentially-tuned frequency synthesizer, but through proper loop parameters, loop filter phase noise can be lowered. Circuit details are also presented. Complimentary CMOS switches connected with resistance are adopted to enhance the analog loop (PFD + CP) linearity. Test results show that although the charge pump design is relatively complicated, the CP current match performance is superior in terms of reference spurs. 8/9 high speed prescaler is analyzed and the design considerations for the CML logic is also presented. Measured results show that the presented frequency synthesizer could meet the DVB tuner applications.

References

[1] Dawkins M, Burdett A P, Cowley N. A single-chip tuner for DVB-T. IEEE J Solid-State Circuits, 2003, 38(8): 1307

[2] Saias D, Montaudon F, Andre E, et al. A 0.12 μm CMOS DVB-T tuner. IEEE Int Solid-State Circuits Conf Tech Dig, Feb 2005: 430

[3] Wu T, Hanumolu P K, Mayaram K, et al. Methods for constant loop bandwidth in LC-VCO PLL frequency synthesizers. IEEE J Solid-State Circuits, 2009, 44(2): 427

[4] Gardner F M. Charge-pump phase-lock loops. IEEE Trans Circuits Syst, 1980, 28(11): 1849

[5] He J. Frequency synthesizer for DVB-T receivers. PhD Dissertation, Fudan University

[6] Lu L. Frequency synthesizer for RF receivers. PhD Dissertation, Fudan University

[7] Lu L, Chen J, Yuan L, et al. An 18-mW 1.175–2 GHz frequency synthesizre with constant bandwidth for DVB-T tuners. IEEE Trans Microvew Theory Tech, 2009: 928

[8] Cheng S. Design and analysis of an ultrahigh-speed glitch-free fully differential charge pump with minimum output current variation and accurate matching. IEEE Trans Circuits Syst II, Express Breiefs, 2006, 53(9): 843

[9] Tang Z, He J, Min H. A low-phase-noise 1-GHz LC VCO differentially tuned by switched step capacitors. IEEE Asia Solid-State

Circuits Conference Proceedings, Nov 2005: 409
[10] Rhee W, Song B S, Ali A. A 1.1-GHz CMOS fractional-*N* frequency synthesizer with a 3-b third-order delta-sigma modulator. IEEE J Solid- State Circuits, 2000, 35: 1453
[11] Maxim A, Poorfard R, Kao J. A sub-1.5° phase-noise ring-oscillator-based frequency synthesizer for low-IF single-chip DBS satellitetuner-demodulator SoC. IEEE Int Solid-State Circuits Conf Tech Dig, Feb 2006: 618
[12] Marutani M, Anbutsu H, Kondo M, et al. An 18 mW 90 to 770 MHz synthesizer with agile autotuning for digital TV-tuners. IEEE Int Solid-State Circuits Conf Tech Dig, Feb 2006: 192
[13] Gupta M, Lerstaveesin S, Kang D, et al. A 48-to-860 MHz CMOS direct-conversion TV tuner. IEEE Int Solid-State Circuits Conf Tech Dig, Feb 2007: 206