A low-phase-noise digitally controlled crystal oscillator for DVB TV tuners*

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Abstract: This paper presents a 25-MHz fully-integrated digitally controlled crystal oscillator (DCXO) with automatic amplitude control (AAC). The DCXO is based on Colpitts topology for one-pin solution. The AAC circuit is introduced to optimize the phase noise performance. The automatic frequency control is realized by a 10-bit thermometer-code segmental tapered MOS capacitor array, ensuring a $\sim$ 35 ppm tuning range and $\sim$ 0.04 ppm frequency step. The measured phase noise results are –139 dBc/Hz at 1 kHz and –151 dBc/Hz at 10 kHz frequency offset, respectively. The chip consumes 1 mA at 1.8V supply and occupies 0.4 mm^2 in a 0.18-μm CMOS process.

Key words: crystal oscillator; DCXO; phase noise; supply pushing; VCTCXO; VCXO
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1. Introduction

Crystal oscillator plays an important role in modern communication systems for its precise oscillation frequency, low phase noise and low power. However, the oscillation frequency will drift with temperature as well as with the crystal aging. So a frequency tuning circuit is necessary to adjust the frequency to sub-ppm accuracy to cover a wide range of working temperatures over several years. Besides, low phase noise is also an important concern in tuner systems since the close-in phase noise of a PLL is dominated by the up-converted flicker noise ($1/f$) of the crystal oscillator.

The popular way to make the frequency of a crystal oscillator (XO) adjustable is to use a varactor embedded into an XO and tune its voltage. However, this needs an extra ADC to convert the digital signal from the baseband to an analog voltage. It is a costly and inefficient way for power consumption and pin limitation concerns. A more efficient approach is to design an XO that can be controlled by digital input and so is called DCXO[1].

A simplified scheme of a DCXO is shown in Fig. 1. The DCXO is based on Colpitts topology for one-pin solution. Frequency tuning is achieved by a digitally-controlled capacitance C_2. To obtain a reasonable tuning range, the value of C_2 may vary in a range of 10–50 pF. This large variation will impact the start-up constraints and bias current must be large to insure oscillation when all the capacitance of C_2 is connected to the tank. Moreover, due to the PVT (Process, Voltage and Temperature) variation the oscillation amplitude will change a lot for a fixed bias current, thus degrading the phase noise performance. So a well defined amplitude of oscillation is desired to balance the phase noise and power consumption. The other reason why a well controlled amplitude is needed is that the power dissipated in the crystal is determined by the amplitude at the crystal node. A very high amplitude will speed up the crystal aging.

DCXOs with a good temperature frequency stability are published in Refs. [2, 3]. But the bias current in Ref. [2] is generated by a bandgap voltage divided by a resistor and the amplitude cannot be controlled. Reference [3] has designed a clock buffer to make the output swing changeable. However, the amplitude at the oscillation node which is directly connected to the crystal is not concerned.

In this paper, a low-phase-noise DCXO with an automatic amplitude control loop implemented in a 0.18-μm CMOS process is presented. The AAC circuit is introduced to optimize the phase noise performance. An impedance boost technique is employed to suppress the supply pushing effect and $1/f$ noise from the power supply. The AFC frequency tuning is achieved by digitally switching a 10-bit thermometer-code MOS capacitor array to guarantee a monotonic frequency tuning characteristic.

2. Basic crystal oscillator design

One of the best known oscillator structures is the so called three-point oscillator. Depending on which of the three points is ac grounded, the circuit is known as Colpitts, Pierce and Clapp oscillators. A Colpitts topology is preferred for it only requires one connection pin which is suitable with the pin-limited low-cost package[4].

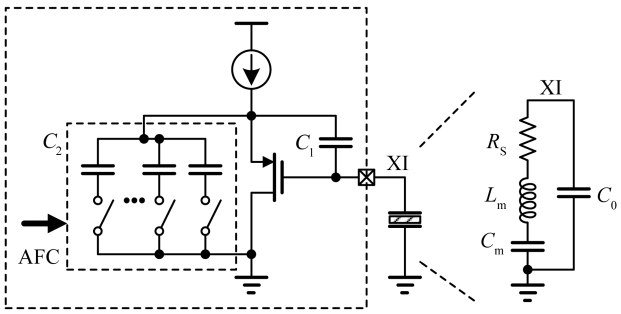

Fig. 1. Basic DCXO scheme.

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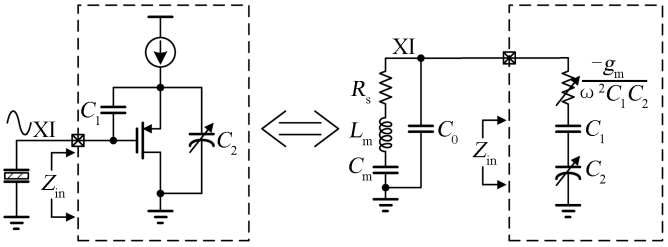

Fig. 2. Simplified DCXO and its small-signal model.

Figure 2 shows a simplified Colpitts crystal oscillator and its equivalent small-signal model. The crystal can be modeled by shunt capacitance C_0 in parallel with a series combination of a motional inductance L_m, a motional capacitance C_m and a motional resistor R_s. The oscillation frequency of the circuit is approximately given by

$$f_{osc} = \frac{1}{2\pi\sqrt{L_m \dfrac{C_m(C_0+C_L)}{C_m+C_0+C_L}}} \approx \frac{1}{2\pi\sqrt{L_m C_m}}\left[1+\frac{C_m}{2(C_0+C_L)}\right], \quad (1)$$

where C_L is the series combination of C_1 and C_2. The small-signal model of the circuit includes two capacitors $C_1$and C_2, and a negative resistor which can be shown to be

$$-R = \frac{g_m}{\omega^2 C_1 C_2}, \quad (2)$$

where ω is the oscillation frequency, and g_m is the transconductance of the PMOS transistor. The negative resistance compensates the loss in the crystal, thus sustaining the oscillation. For the frequency stability concern[5], C_1 and C_2 are a few times larger than C_0. Frequency tuning is achieved by digitally switching the capacitance C_2 from an AFC code.

The circuit is connected to the power supply through a current source. An impedance boost technique is adopted to increase the output impedance of the current source, thus making the oscillation frequency insensitive to the supply variation and suppressing the $1/f$ noise from the power supply. The phase noise performance of the DCXO is also an important concern since the flicker noise of the crystal oscillator goes up-converted to the close-in phase noise of the frequency synthesizer.

3. Phase noise specification of DCXO

For DVB-T tuner applications, a wideband fractional-N synthesizer is usually used to cover a frequency range of 975 to 1960 MHz. To meet the requirements of tuners, low phase noise and low phase error are demanded for the synthesizer. The close-in phase noise of a typical frequency synthesizer is dominated by the up-converted flicker noise of crystal oscillator and out-of band phase noise is contributed mainly from the voltage-controlled oscillator (VCO). A DCXO with good phase noise can relax the PLL design since a larger loop bandwidth can be adopted to suppress the VCO phase noise, although more reference noise contributes to the output, which has a negligible effect on the total integrated rms phase error. Figure 3 shows a simulation result of the noise contribution in a PLL. The total PLL output phase noise is mainly the superposition of the low-passed yet up-converted reference noise and high-passed VCO noise. Besides, the low-passed charge pump noise also has some contribution at in-band frequency offset.

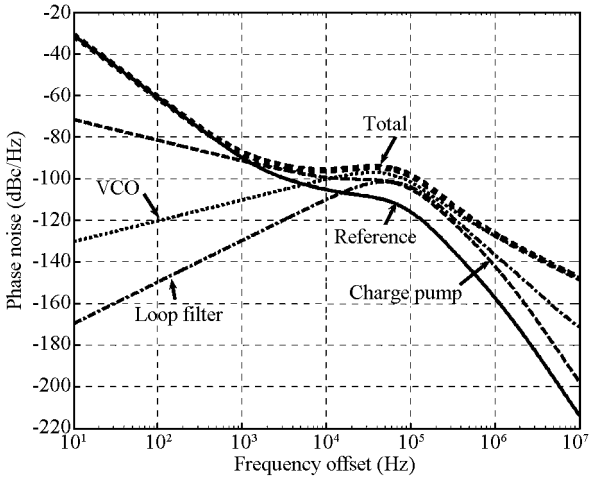

Fig. 3. Simulation result of the output phase noise in a PLL.

For a 25-MHz crystal oscillator, the division modulus in a PLL should be as large as 80 to cover the frequency band. To meet tuner applications, an integrated rms phase error less than 1° is required[6]. A phase error of 0.1°–0.2° margin should be taken into consideration due to other noise sources from charge pump and loop filter. The in-band phase noise of a PLL is calculated to be −90 dBc/Hz for an integrated RMS phase error of 0.8°. Therefore, the phase noise requirement of the DCXO should be less than $-90\text{dBc/Hz} - 20\lg 80 = -128$ dBc/Hz at 1 kHz frequency offset.

4. Circuit design

Figure 4 shows the complete circuit schematic of the DCXO, which is based on Colpitts topology for one-pin solution. This DCXO is powered by an integrated LDO. An impedance boost technique is adopted to get a high power supply rejection ratio (PSRR) current source, thus, reducing the DCXO supply pushing effect. Frequency tuning is achieved by tuning the capacitance C_2 value digitally through a digital AFC code. The oscillator amplitude control loop comprises a peak detector, two comparators, and a binary search algorithm to sense and regulate the oscillator amplitude. There is also a chain of inverter buffers intended for outputting reference clocks to baseband circuitry and phase-frequency detector (PFD) in frequency synthesizers. The input of the output buffer is connected to the gate of M1 for lower phase noise[7]. The gate of M1 is set to the logic threshold voltage of the first inverter that is biased through a replica bias cell to achieve a good duty cycle.

4.1. Frequency tuning

The tuning range requirement is primarily determined by the amount of frequency instability in the crystal which includes the initial crystal offset, temperature instability and the

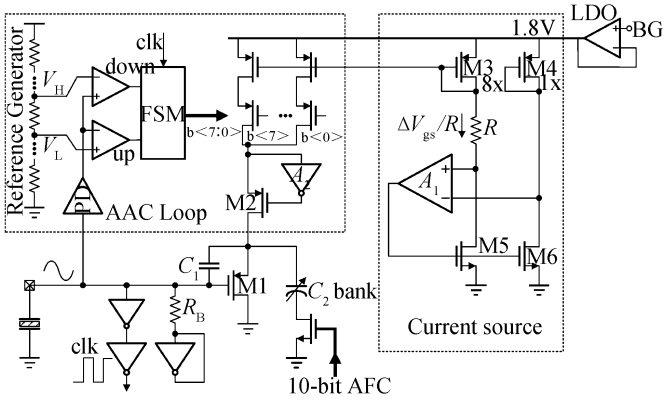

Fig. 4. Detail circuit topology of the DCXO.

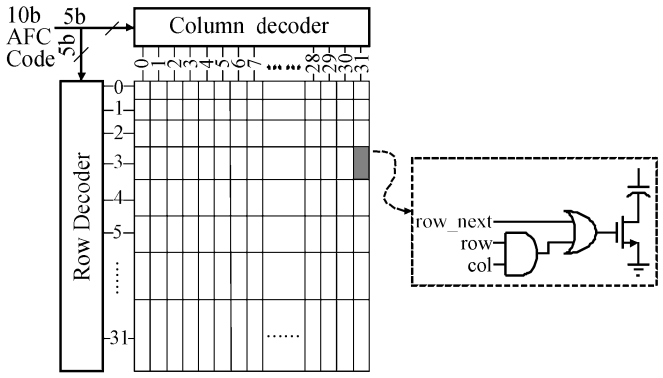

Fig. 5. 10-bit AFC capacitor array with segmental tapered scheme.

frequency instability due to aging. In this design, frequency tuning is realized by tuning C_2, thus tuning C_L. The tuning range can be approximately calculated to be

$$\text{Tuning Range} \approx \frac{C_m(C_{L\max} - C_{L\min})}{2(C_0 + C_{L\max})(C_0 + C_{L\min})}. \quad (3)$$

It can be seen that one way to increase the tuning range is to maximize the difference between $C_{L\max}$ and $C_{L\min}$.

A 10-bit AFC capacitor array is designed to achieve a frequency error smaller than 0.1 ppm. As shown in Fig. 5, the 10-bit capacitor array is a segmented array with a 5-bit MSB row decoder and a 5-bit LSB column decoder. A predistortion scheme is adopted to linearize the frequency transfer function versus AFC code. The capacitor size is segmental tapered when the AFC code decreases. The capacitor size within one row is kept same to facilitate the layout.

To achieve a reasonable tuning range, the size of the MOS transistors should be carefully chosen. Inversion mode MOS (I-MOS) capacitors are used. The ratio of the unit capacitance between on-state and off-state should be as large as possible. However, the parasitic capacitor should be minimized when the capacitance is off, otherwise, even 1-fF parasitic capacitor per unit cell can reduce the tuning range greatly. Reducing parasitic capacitance through device size reduction means worse $1/f$ noise, namely worse close-in phase noise. It is a tradeoff.

4.2. Automatic amplitude control

In general, a high amplitude is necessary to minimize the phase noise degradation. However, a very high amplitude can cause the waveform distortion and induce a jitter due to the non-linear effect. Also a very high amplitude will overdrive the crystal and impact the crystal frequency with aging. So a well defined amplitude of oscillation is required to optimize the phase noise performance and minimize the power dissipation at the same time.

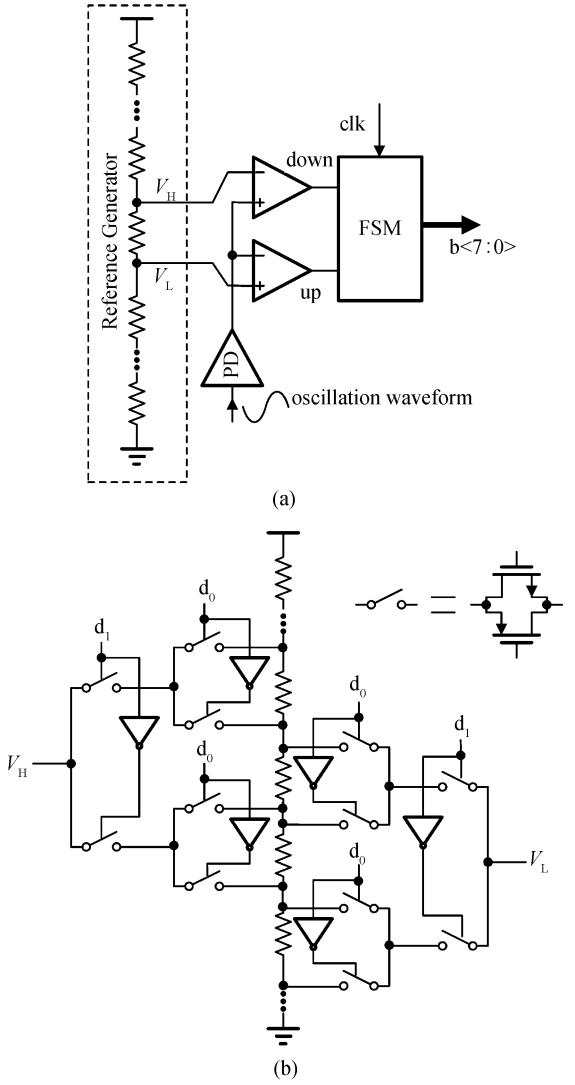

Fig. 6. Automatic amplitude control loop. (a) Amplitude control diagram. (b) Reference voltage generator.

The automatic amplitude control (AAC) diagram is shown in Fig. 6(a). A peak detector (PD) is used to sense the oscillation amplitude, which is compared with two reference voltages V_H and V_L. The outputs of the comparators are fed back to a finite state machine (FSM) that decides whether to update the bias current or to end the amplitude adjustment. The amplitude will finally fall into a target window which is between V_H and V_L. Moreover, the target window can be programmed by changing the two reference voltages. Figure 6(b) shows the reference voltage generator, which is a resistor chain with programmable digital control signals.

It is noted that there must be sufficient resolution of the amplitude to allow the PD to finally let its output fall into the target window. Otherwise, the amplitude will "hunt" between two reference voltages on and on. So the amplitude response

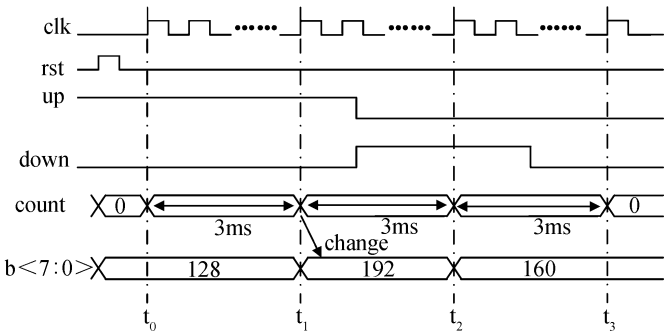

Fig. 7. Timing plan of the AAC block.

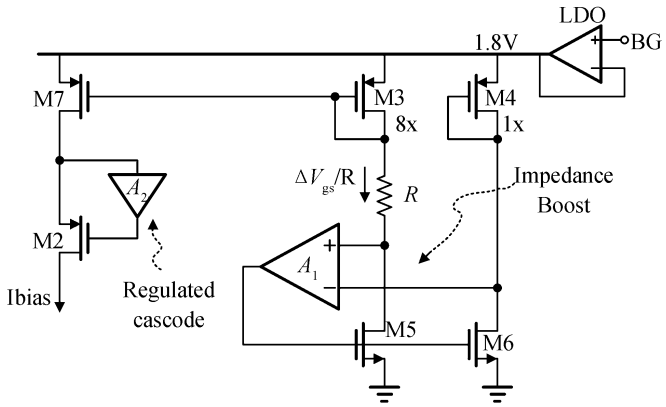

Fig. 8. High-PSRR current source.

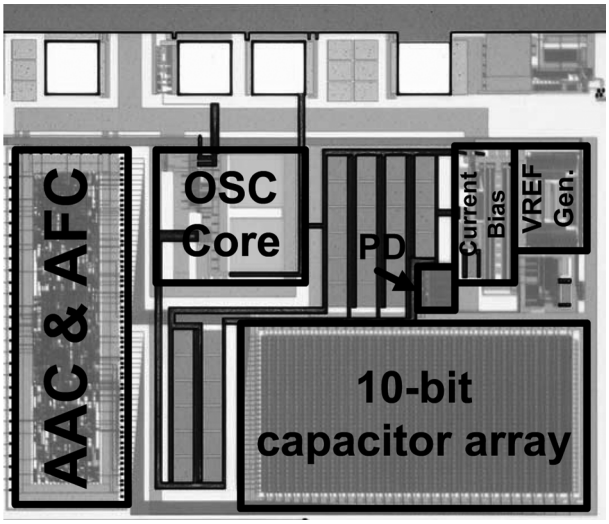

Fig. 9. Die microphotograph.

to the bias current should be carefully simulated. In addition, the offset of the two comparators should also be minimized compared with the target window defined by the two reference voltages.

Since the amplitude response to the bias current is quite slow due to the high-Q characteristic of the crystal, the change of the bias current, which is controlled by b<7:0>, must wait enough time until the amplitude is stable. Figure 7 illustrates the detailed timing plan in one comparison step. Before oscillation happens, an *rst* signal is given to set an initial state of b<7:0>. The initial state is set to 128 in this case. After a while, the circuit starts oscillation and generates a clock for the AAC algorithm. At time t_1, the output b<7:0> gets changed when a counter inside AAC counts up to 3 ms. Since the up signal is high, b<7:0> turns out to be 192 to increase the amplitude. At time t_2, the down signal is high and b<7:0> decreases to 160. At time t_3, the amplitude falls in the target window and both signals, up and down, become low. The output b<7:0> keeps the last state and a desired amplitude is obtained. Current boosting is enabled to shorten the start-up time. The amplitude control logic AAC is implemented by a binary search algorithm to save comparison time.

4.3. High-PSRR current source

This DCXO is powered by a dedicated LDO, which takes the bandgap voltage as its reference. A high-PSRR current source is designed to suppress the supply pushing effect and noise at the same time. In Fig. 8, a Wildar type current source with an impedance boost technique (A1, M5 and M6) is used. The impedance looking down to the ground is boosted by the gain of amplifier A1. The gate voltages of M3 and M4 follow the supply voltage, so the current is immune to the supply variation. A current mirror with a regulated cascode (M2 and A2) is used to generate the current bias. The output impedance is calculated to be

$$R_{\text{out}} \cong g_{\text{m2}} r_{\text{ds2}} r_{\text{ds7}} (1 + A_2). \tag{4}$$

Compared to a single cascode, the output impedance is boosted by the gain of amplifier A2. High output impedance makes the current insensitive to the supply variation. Since the flicker noise of LDO gets up-converted to be close-in phase noise of the DCXO, the impedance boost technique can effectively reduce the noise contribution from LDO.

4.4. Phase noise design considerations

The phase noise of a reference clock is important for close-in phase noise of a frequency synthesizer. The dominant noise sources of the DCXO are up-converted $1/f$ noises from the oscillator core driver M1, the LDO, bias current sources, and replica bias for buffer. The noise from the first stage of the output buffer is an important concern since in the waveform there is a sinusoidal wave that makes the switching time of the first stage much longer than that of the following stages. The large size of the first buffer can prevent phase noise degradation. However, the capacitive loading on the crystal node is increased and the tuning range is reduced.

This Colpitts topology oscillator operates in the class-C configuration. The peak drain current of M1 happens when the gate voltage of M1 is in the lowest level which is in the least phase-noise-sensitive region. For this reason, Colpitts oscillator usually achieves excellent phase noise performance[8]. A PMOS device is chosen in the oscillator core for its better $1/f$ noise.

5. Measurement results

The chip was fabricated in a 0.18-μm CMOS process and the microphotograph is shown in Fig. 9. The total area of this

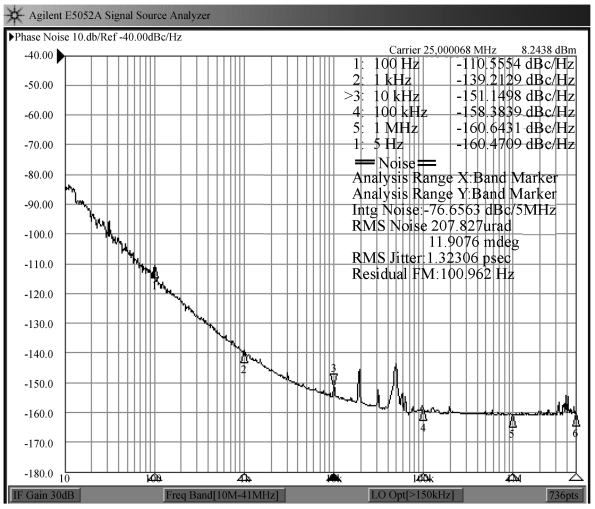

Fig. 10. Measured DCXO phase noise.

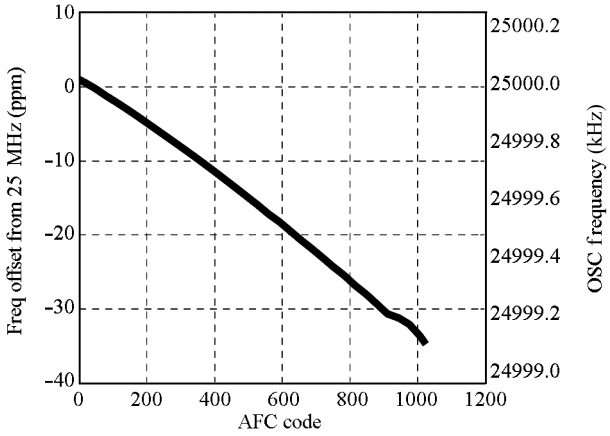

Fig. 11. Measured AFC tuning range.

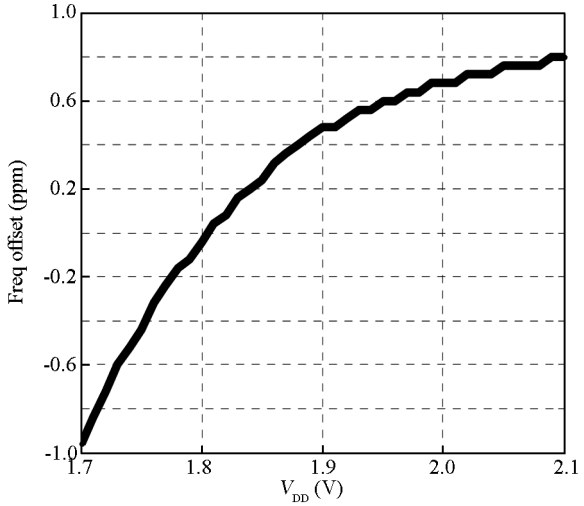

Fig. 12. Measured supply pushing characteristic.

DCXO is 0.5 × 0.8 mm^2 excluding PADs. The power consumption is 1.8 mW.

Figure 10 shows the measured phase noise with –139 dBc/Hz at a 1 kHz frequency offset and –151 dBc/Hz at a 10 kHz frequency offset. The excellent phase noise performance significantly relaxes the PLL phase noise requirement. The tuning range of this DCXO is illustrated in Fig. 11. About a 35 ppm tuning range is achieved and it is wide enough to cover the temperature instability and crystal aging. An average frequency step of 0.04 ppm is achieved, which is sufficient for applications of less than 0.1 ppm frequency accuracy. The frequency versus code transfer function is fairly linear due to the predistortion scheme. The center frequency is a bit lower than 25.000000 MHz due to the unexpected estimation error of MOS capacitor array. Figure 12 shows the measured DC supply pushing at 25 MHz. The frequency variation is less than 2 ppm from 1.7 to 2.1 V due to the impedance boost techniques.

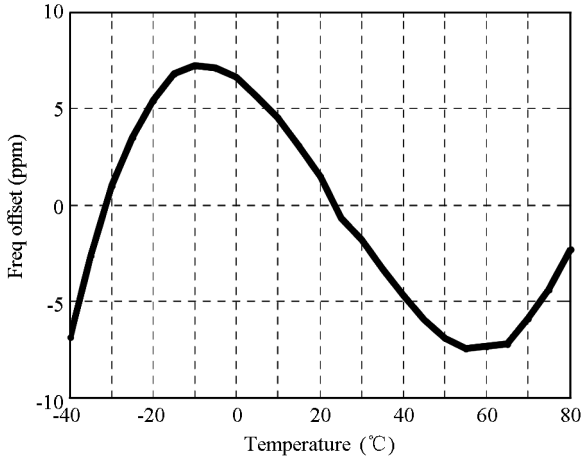

Fig. 13. Measured frequency instability over temperature.

Table 1. Performance Summary.

Parameter	Value
Voltage	1.8 V
Current	1 mA
Oscillation frequency	25 MHz
Tuning range	∼ 35ppm
Frequency step per AFC code	∼ 0.04ppm
Phase noise @25MHz	–139 dBc/Hz @ 1 kHz offset –151 dBc/Hz @ 10 kHz offset
Frequency instability at –40 to 80 ℃	±7 ppm
Area	0.4 mm^2
Technology	0.18 μm CMOS

Figure 13 shows the DCXO frequency instability over temperature. Since the DCXO is used in tuner application, the requirement of frequency instability is not so tight. The frequency variation is ±7 ppm across the temperature range from –40 to 80 ℃. Table 1 summarizes the measurement results of this DCXO, and the performance comparison is given in Table 2. As for the multi-standard wireless application, the temperature instability requirement is much tighter than that achieved for this DCXO. References [2, 3] show DCXOs with temperature compensation.

6. Conclusions

In this paper, a 25-MHz low-phase-noise DCXO is implemented in a 0.18-μm CMOS process. An automatic ampli-

Table 2. Performance comparisons.

Parameter	Ref. [1]	Ref. [2]	Ref. [3]	This Work
Frequency (MHz)	26	26	19.2	25
Application	GSM/Bluetooth/WLAN	WCDMA	—	DVB tuner
Phase noise @ 1 kHz (dBc/Hz)	–140	–138	–137	–139
Supply voltage (V)	1.4	1.5	2.7	1.8
Tuning range (ppm)	~ 70	~ 28	N.A	~ 35
Power consumption (mW)	3	4.2	6.5	1.8
Supply pushing (ppm/V)	1	—	0.2	± 2
Frequency instability at –10 to 55 ℃ (ppm)	±4	2	< 3	±7
Die area (mm^2)	0.18	0.52	0.75	0.4
Technology	90 nm CMOS	0.13 μm CMOS	0.35 μm SiGe BiCMOS	0.18 μm CMOS

tude control loop is introduced to balance the phase noise performance and the power consumption. A 10-bit thermometer-code capacitor array with segmentally tapered capacitor size is adopted to guarantee the monotonocity. The impedance boost technique is employed to suppress the supply pushing. The measured phase noise is about –139 dBc/Hz at 1 kHz and –151 dBc/Hz at 10 kHz frequency offset while it only draws 1 mA from a 1.8 V supply. The measured supply pushing is ± 2 ppm/V. Measurements show that this DCXO has a ~ 35 ppm tuning range with a ~ 0.04 ppm frequency step. The DCXO with good phase noise and frequency stability can meet the requirements of tuner applications.

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