A 900 MHz, 21 dBm CMOS linear power amplifier with 35% PAE for RFID readers*

Han Kefeng(韩科锋), Cao Shengguo(曹圣国), Tan Xi(谈熙)†, Yan Na(闫娜), Wang Junyu(王俊宇), Tang Zhangwen(唐长文), and Min Hao(闵昊)

(State Key Laboratory of ASIC & System, Fudan University, Shanghai 201203, China)

Abstract: A two-stage differential linear power amplifier (PA) fabricated by 0.18 μm CMOS technology is presented. An output matching and harmonic termination network is exploited to enhance the output power, efficiency and harmonic performance. Measurements show that the designed PA reaches a saturated power of 21.1 dBm and the peak power added efficiency (PAE) is 35.4%, the power gain is 23.3 dB from a power supply of 1.8 V and the harmonics are well controlled. The total area with ESD protected PAD is 1.2×0.55 mm^2. System measurements also show that this power amplifier meets the design specifications and can be applied for RFID reader.

Key words: CMOS; power amplifier; PAE; power matching; RFID; reader
DOI: 10.1088/1674-4926/31/12/125005 **EEACC:** 1220

1. Introduction

During the past several decades, CMOS has achieved great success for low cost and high yield, and it is also a popular choice of system on chip for radio frequency (RF) wireless connectivity. Nowadays, CMOS RF building blocks, such as LNAs[1], mixers[2] and VCOs[3], have achieved good performance compared with other technologies, except for the PA because CMOS technology suffers from some serious problems. Firstly, with a lossy substrate, a poor on-chip passive component such as an inductor may degrade the whole efficiency of the PA. Meanwhile, substrate coupling may also cause some fatal problems to other blocks. Secondly, a low voltage supply scaled with technology limits the output power and linearity dramatically. Critically, its low breakdown voltage is a catastrophic factor for a PA's reliability if it tries to deliver a high output level. In addition, the low mobility of CMOS results in a much larger dimension for transistors, so its performance at high frequency may be deteriorated because of a complicated parasitic effect. Finally, the hot carrier effect also affects the performance and reliability. As a result, a higher integration for the on-chip PA becomes more challenging.

Recently, most wireless standards would like to use non-constant envelope modulation schemes to enhance the data rate and the system capacity. Taking the RFID system as an example, ASK is adopted to simplify the complexity and lower power consumption for passive tags that acquire energy from electromagnetic waves. As a result, a linear PA is still a good solution to deal with the variable envelope modulated signals. However, one disadvantage of the linear PA is the efficiency, which is critical for use-time in practical applications. Another problem is how to achieve a high power and efficiency in deep sub-micro CMOS technology with a scaled supply.

In this paper, a two-stage differential class-AB CMOS PA for a UHF RFID reader is presented. To overcome the reliability problem, a cascode topology is employed. To gain a power of more than 20 dBm from a supply of 1.8 V, output matching for this differential PA is analyzed in detail and realized on a PCB board. To gain a higher efficiency and maintain relatively good linearity, the PA works in deep class-AB mode. Measurements show that this PA offers 21.1 dBm saturated power and 18.4 dBm at 1dBCP to the load without thick-oxide MOS, the maximum PAE is measured to be 35.4%. With the adopted harmonics termination, the output harmonics are also well controlled, as will be shown.

2. Basic theory of linear PA

The basic circuit of a linear PA is shown in Fig. 1. Different from a switch-mode PA, the power transistor M1 is modeled as a voltage-controlled current source, L_C is the RF choke for feeding power to the drain and blocking RF signals, C_B is a through capacitor between the drain and output load, L_S with C_p forms a LC tank at the working frequency for filtering the unwanted harmonics, and R_L represents the load of the PA. V_B

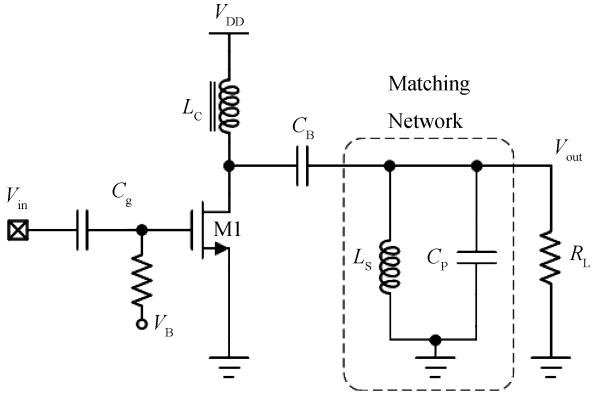


Fig. 1. Basic topology of linear power amplifier.

* Project supported by the Ministry of Science & Technology of China (No. 2008BAI55B07).
† Corresponding author. Email: tanxi@fudan.edu.cn
Received 21 April 2010, revised manuscript received 25 July 2010

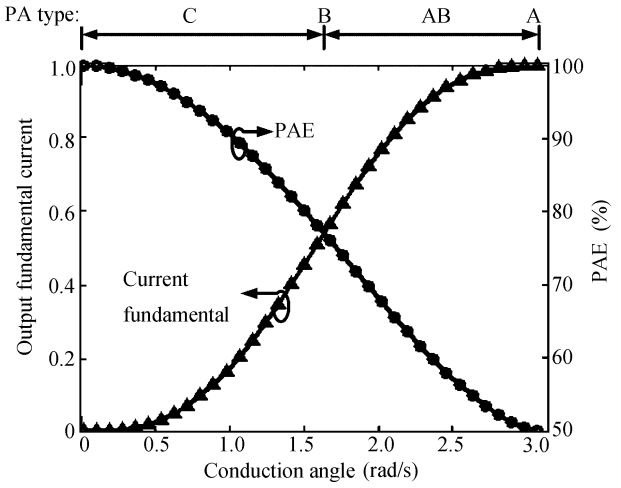


Fig. 2. Current fundamental and PAE in terms of conduction angle.

is the DC bias for M1, which determines the conduction angle, thus PA is classified to class A, AB, B or C with corresponding angles. Each class has different performances, such as gain, efficiency, and linearity.

For simple analysis[4], the output current fundamental i_{fund} and PAE of a linear PA can be expressed in terms of the conduction angle θ, given as

$$i_{\text{fund}} = \frac{i_{\text{rf}}\,(2\theta - \sin 2\theta)}{2\pi}, \tag{1}$$

$$\text{PAE} = \frac{2\theta - \sin 2\theta}{4\,(\sin\theta - \theta\cos\theta)} \times 100\%. \tag{2}$$

Here, the range of conduction angle θ is from 0° to 180°, and Figure 2 depicts the results of Eqs. (1) and (2) with respect to θ. As shown in Fig. 2, class-A has a maximum output fundamental current which implies a higher gain by sacrificing the PAE, while class-C gains a PAE of 100% with a penalty of less output power. Of all the cases, class-AB is the most widely used choice for a tradeoff between linearity and efficiency.

3. Design of the two-stage CMOS PA

3.1. Circuit design of linear PA

The overall schematic of the two-stage PA is shown in Fig. 3. The transistors M1 and M2 are configured as the first stage with dimension of 192 μm/0.18 μm. The second stage is similar and the dimensions are 2700 μm/0.18 μm. The on-chip inductor L_{L1} paralleled with C_{L1} is as LC load of first stage, the inductor is of center tapped differential type[5] to save chip area, and the power supply is fed via the center tap. Inter-stage matching is done by RC high pass network, and the bias of the second stage is given by the resistors. The outputs of the PA are connected to an off-chip balun, and the power is supplied by off-chip inductors L_{B1} and L_{B2}.

Due to the large dimension of the transistors, simulated input parasitic capacitance of M3a or M3b is up to 4 pF when the transistors are biased at about 0.5 V, so the inductance of L_{L1} should not be too large and capacitor C_{L1} should be chosen carefully with the post-layout simulation. The large coupling capacitance of C_{c3} and C_{c4} is preferable because the signal will be divided by the coupling capacitor and the input parasitic capacitor of the transistors, otherwise the whole gain will suffer from great loss.

The first stage is biased at a relatively high overdrive level in order to maintain a good linearity. In our test settings, the bias voltage is 0.74 V. For the second stage, the bias voltage is set to 0.53 V, close to its knee voltage but a bit more than simulation, thus the second stage works at the mode of class-AB, closer to class-B for exchange of efficiency. It is worth mentioning that the 3rd order distortion of the transconductor (g_{m}) is around zero[6].

The output matching and harmonic control network is created using discrete components, L_1 series with C_1 is for the 2nd order harmonic termination and L_2 with C_2 is for output power matching to maximize the output power, which will be discussed in particular next.

3.2. Differential versus single-ended topology

Generally, on-chip circuits are differential to suppress the noise from the substrate or supply and reject common-mode interferences, and even order harmonics can be eliminated ideally. However, most antennas are single-ended, so differential to single-ended conversion is inevitable either on-chip or off-chip. On-chip conversion needs passive or active balun. The former is a good choice with the cost of chip size, while the latter one has to deal with large signal swing. As a result, efficiency degradation is evident and the linearity is a practical problem too. So an off-chip balun is applied in our scheme.

Differential topology is also expected to have an extra 6 dBm power than a single-ended one, and this is desirable especially for CMOS technology when the supply voltage scales down. From another point of view, the output balun acts as a power combiner to the load and, as a result, the output power increases.

3.3. Single-stage versus two-stage scheme

In our transmitter scheme, an active up-mixer uses a LC tank as its load, so when it is cascaded directly with power transistors, the input capacitance of the PA will greatly affect the frequency response of the LC load. To drive the power stage, an inter-stage amplifier is placed between the up-mixer and the PA as a buffer and this reduces the input parasitic capacitance. One disadvantage is that the driver stage will consume a fixed power from the supply and the efficiency will be degraded compared to the single-stage scheme. The gain of the driver should be small because in the transmitter path, the signal level is much higher than a receiver, so linearity plays an important role for SNR. High gain is often provided by the last stage and low gain is for the baseband circuit and up-mixer. In this way, the transmitter can satisfy the stringent output spectrum requirement, such as the adjacent channel power ratio (ACPR)[7]. So, the high output level of the first stage to the last stage will exceed the linear range of the PA and, consequently, the spectrum of output power will not satisfy the emission requirements.

3.4. Cascode versus common source

The breakdown effect has become a key factor for the output power and reliability for designing a PA in deep sub-micro CMOS technology. To a traditional CS stage, a gate is most

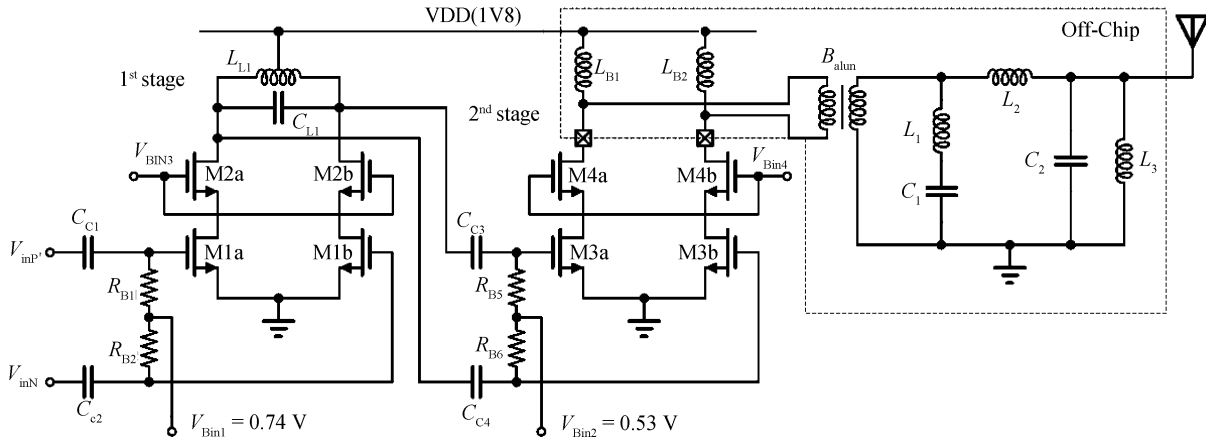


Fig. 3. Schematic of designed CMOS two-stage linear PA for RFID reader.

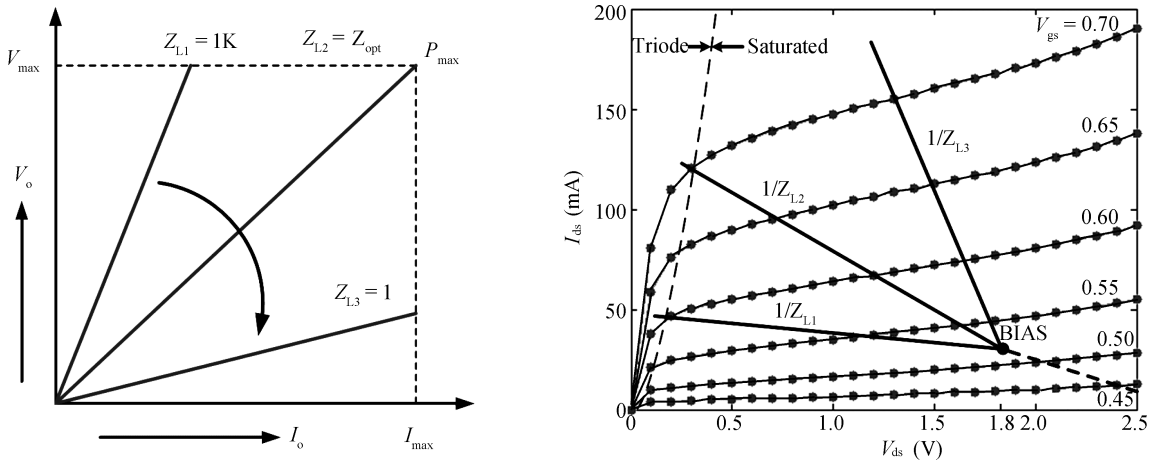


Fig. 4. Relationship of load, output current and voltage.

likely to suffer from breakdown because it undergoes a large anti-phase signal swing with the drain. If a cascode transistor is stacked on the CS transistor, the risk of breakdown can be reduced[8]. In this work, normal transistors are applied rather than thick-oxide MOS because the maximum output swing at the drain is $2V_{DD}$ for the linear type of PA. So, even in the worst case, there is still enough margin to keep the cascode transistors from breakdown if the gate is biased close to 1.8 V for the cascode transistor[16].

Another issue is a stability problem which is very common in the PA design. For the CS stage, a feedback resistor is often placed between the gate and the drain for the sake of stability. In the cascode type PA, isolation can be improved by a cascode transistor without the feedback resistor. It should be noted that the reverse feed-through is also an important factor for instability in the PA. The penalty of the cascode is that its linearity performance is inferior to the CS type—a difference of 2–5 dB can be found for the third-order inter-modulated component (IM3) for different bias to our simulation.

3.5. Output power matching

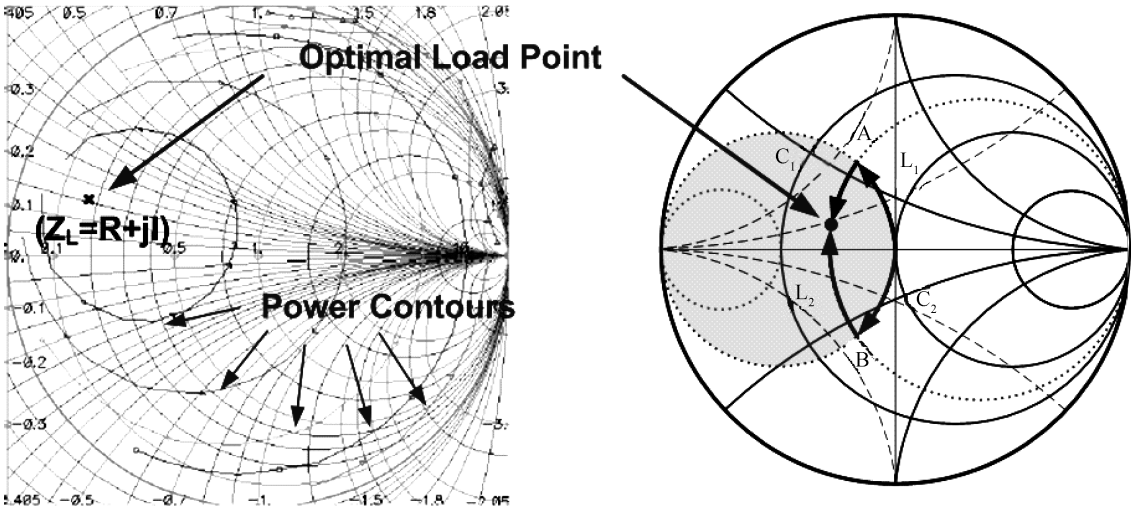
As the supply voltage scales down, it becomes more challenging to realize a high output power PA on the chip. To a 0.18 μm CMOS technology, the typical supply voltage for normal operation is 1.8 V, so the maximum power it can send to the 50 Ω load is 12.92 dBm if a knee voltage of 0.4 V is considered for a single-ended circuit without any output matching method. Though the output level can be 6 dBm more for a differential type, the power is still less than 20 dBm without any output matching.

Actually, when the dimension of a power transistor is chosen, the maximum output power it can deliver to the load is determined[9] because the peak current of this power transistor is limited, so in theory the ultimate power (in dBm) that the PA can deliver is

$$P_{\max}|_{\mathrm{dBm}} = 10\lg\left(\frac{V_{\mathrm{DD}} I_{\max}}{2} \times 1000\right). \tag{3}$$

Here, $I_{\max}$ is the peak current of the power transistor. Actually, $P_{\max}$ in Eq. (3) cannot be reached because the maximum value of the output voltage and the current may not be achieved simultaneously. As shown in Fig. 4, for a load of 1 kΩ, the voltage fast reaches a maximum value while the current is still far away from its limit. In contrast, when the load is 1Ω, the corresponding voltage is low enough when the current achieves its peak. This case implies a conclusion that there is an optimal load in Eq. (3), and this optimized value can be expressed as

$$Z_{\mathrm{opt}} = \frac{V_{\mathrm{DD}}}{I_{\max}}. \tag{4}$$



(a) (b)

Fig. 5. Load-pull simulation and output matching methods.

The way to gain P_{max} is called load-line matching or power matching. The practical value for optimal impedance (Z_{opt}) seen by the PA can be determined by complicated load-pull measurements, and the results may vary with the environmental temperature, input power level, PCB parasitic parameters, device aging and so on.

Figure 5(a) shows the simulated load pull power contours using spectra at an input of 0 dBm, and Figure 5(b) shows the matching methods to the optimal point. For a linear PA design, the optimal point is often located in the shadowed circular region. So, generally speaking, Z_{opt} is lower than the load R_L. Thus for a power matching PA, the small signal gain will drop compared to a PA that drives the load directly, while in large signal condition, the output power will be improved and, accordingly, the efficiency is enhanced dramatically.

Figure 6 shows the two types of output matching network and the simulated frequency responses for each case in Agilent ADS by an ideal or Murata component model for matching. Path B is adopted here to suppress more of the harmonics or spurious components at higher frequency. A new branch for 2nd order termination is inserted between the output balun and the matching network for two reasons. Firstly, the 2nd order distortion in g_m is maximized when 3rd order distortion is set to be zero intentionally. As a result, due to mismatch in differential outputs, the 2nd order component may exceed 3rd order harmonics in practice. Secondly, the capacitance of C_{gd} couples the 2nd order harmonics to the input, and 3rd order harmonics will be regenerated by fundamental and fed back 2nd order harmonics[6]. With the output matching and harmonic control network, the output power and harmonics will be greatly improved, as will be shown in the section of measurements. The PAE will also be improved, together with more output power to the load, according to

$$\mathrm{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \times 100\%, \tag{5}$$

where P_{out} and P_{in} refer to the output and input power respectively, and P_{DC} means the total power of the PA driven from the supply.

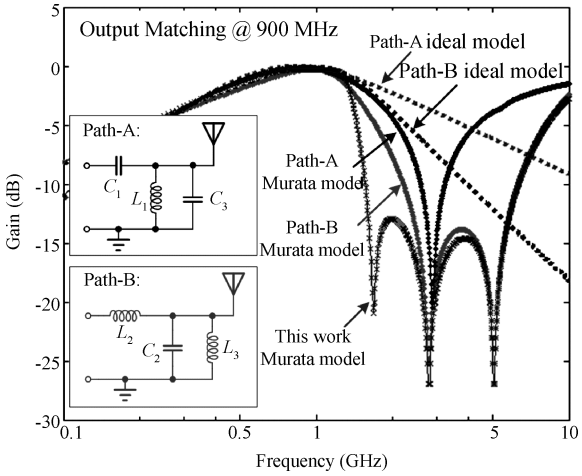


Fig. 6. Two types of matching network of the PA.

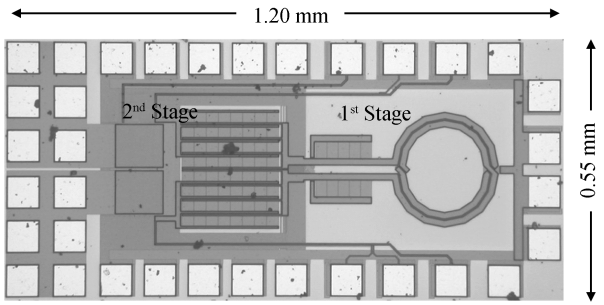


Fig. 7. Die micrograph of the designed two-stage CMOS PA.

4. Chip implementation and experimental results

The chip was fabricated by SMIC in a 0.18 μm CMOS mixed-signal 1P6M process. Its micrograph is shown in Fig. 7. Multi-pads were applied for differential outputs and ground to minimize the inductance of the bond-wire.

Input matching was done by an off-chip LC type network (not shown in Fig. 3) and a balun (Mini-circuits: TC4-14G2+)

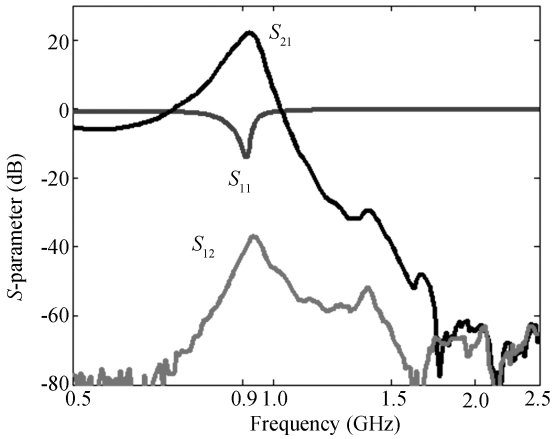


Fig. 8. Measured S-parameter of the PA.

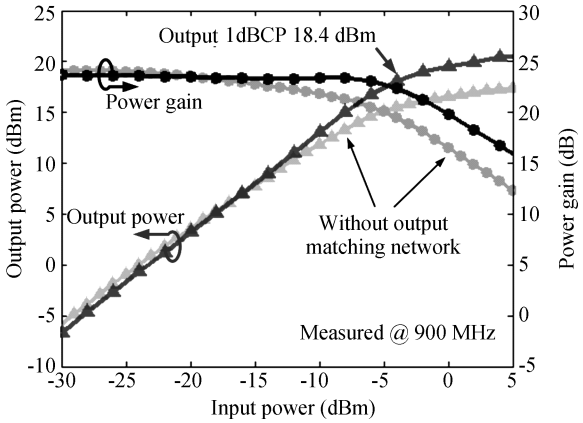


Fig. 9. Power gain and output power versus input power.

was used for single-to-differential conversion. This balun with a typical loss of about 0.85 dB at 900 MHz was also applied to the outputs and the maximum RF power provided was 24 dBm, which was enough for this test.

Two independent LDOs (NS: LM317) were used for the test PCB: one was for voltage bias and the other was a power supply for the PA. With 5 V input, the LDOs offered a 1.8 V supply and a maximum 1.5 A current to the load. Decoupling capacitors were placed carefully on the PCB to avoid instability, which is very common and hazardous in designing a PA.

I–V curves of the two stages were firstly plotted by measuring the gate voltages and corresponding currents, then bias voltages for the PA could be set according to the I–V curve. The DC current of this PA was 35 mA after de-embedding the currents from the LDOs.

Scattering parameters were measured by an Agilent E5071B VNA from 0.5 to 2.5 GHz, as shown in Fig. 8. Good input matching (S_{11}) was achieved at a frequency of 900 MHz and the power gain (S_{21}) reached a peak value of 22 dB around the desired frequency. S_{12} was about –38 dB, so the PA provided good isolation and hence improved the stability.

An Agilent E4440A PSA was used for power, gain and harmonics measurements of the device under test (DUT). In Fig. 9, the power gain is measured to be 23.3 dB at 900 MHz and the saturated power is 21.1 dBm after de-embedding 1.3 dBm loss of balun, PCB runner and test line to the instrument. The output power at 1dBCP is up to 18.4 dBm and the corresponding input power is about –4 dBm. The power and gain curves are also given. Although the PA with a matching network suffers from a little gain loss for small signal inputs, the saturated power gains about 3.7 dBm improvement. The harmonics (at least up to 4th order) are less than –50 dBc at the output power of 8.88 dBm (without calibrating the output loss) and the harmonics are still below –40 dBc at their 1dBCP with the 2nd order termination. As shown in Fig. 10, the harmonics are greatly improved with the output matching and 2nd order termination network in this work.

The maximum PAE is measured to be 35.4% and it drops to 29.2% at 1dBCP, a little lower than its peak value, as shown in Fig. 11. When back off 4 dB from 1 dBCP, the PAE is still up to 20.0%. For the case of no output matching network, the peak PAE is only 17.5%, so the efficiency is greatly improved

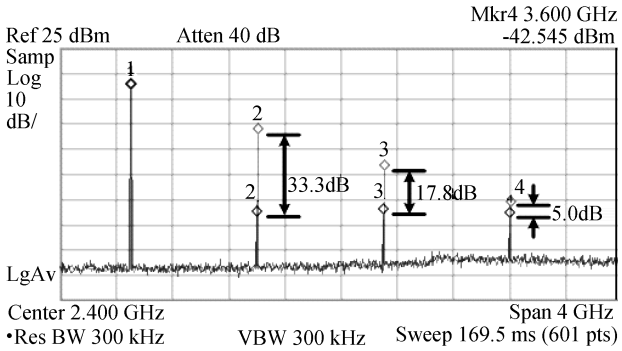


Fig. 10. Measured harmonics with/without matching and harmonics control network.

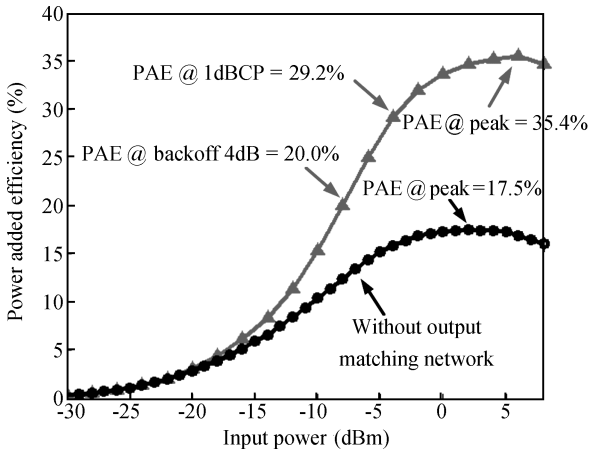


Fig. 11. Measured power added efficiency of the PA.

with the matching network now adopted in this work.

The IM3 and IM5 components shown in Fig. 12 were measured by a two-tone test with frequencies of 899 MHz and 901 MHz. To make comparisons, the adjacent channel power ratio (ACPR1) and alternative channel power ratio (ACPR2) are also given in Fig. 12. The ACPR was measured by a 160-kHz PIE DSB-ASK signal, which was generated by a vector signal generator (Agilent PSG 8267D). As shown in Fig. 13, the spectrum which meets the emission mask requirement defined by EPC global[14] is measured by an input of –14 dBm

Table 1. Performances summary and comparisons with other works.

Parameter	Ref. [6]	Ref. [10]	Ref. [11]	Ref. [12]	Ref. [13]	This work
CMOS process	0.18 μm Cu	0.25 μm	0.18 μm	0.25 μm	0.5 μm	0.18 μm
Power supply (V)	2.5	2.5	2.4	2.5	3.3	1.8
Frequency (GHz)	2.45	0.9	2.4	2.45	1.75	0.9
PA mode	Class-AB	Class-AB	Self-biased	Class-AB	Class-AB	Class-AB
Power gain (dB)	17.5	14.5	38	11.2	23.9	23.3
Power (dBm) Saturated	N/A	N/A	23.5	N/A	N/A	21.1
1 dBCP	20.5	27	20.5	20	24	18.4
PAE (%) Saturated	N/A	N/A	45	30	33	35.4
1 dBCP	37	28	17	28	29	29.2
Back-off	28 (4 dB)	17 (5 dB)	7 (4 dB)	13 (4 dB)*	17 (5 dB)	20 (4 dB)
PA stages	2	2	2	2	2	2
Size (mm^2)	1.34	4.4*	0.46	0.77	3.2	0.66

* Estimated from the paper.

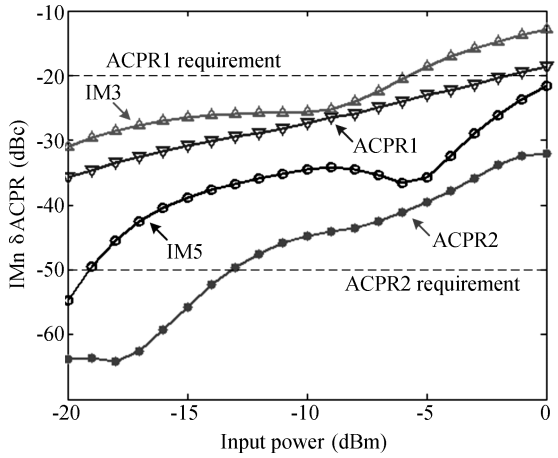


Fig. 12. Measured inter-modulated components and ACPR.

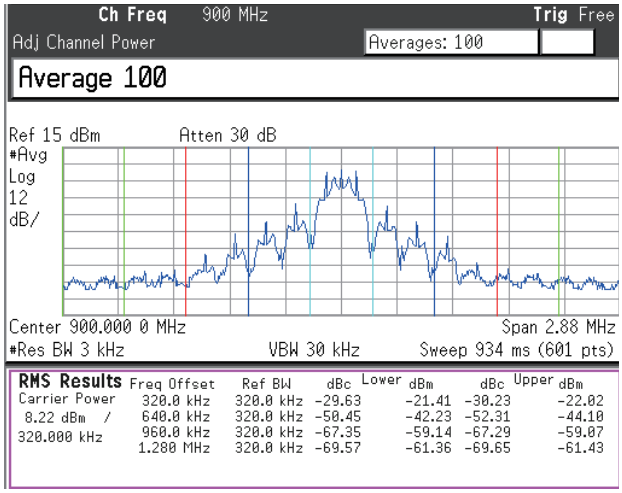


Fig. 13. Measured spectrum for a 160 kHz DSB-ASK input at 8.22 dBm output.

and the RMS channel power is 8.22 dBm without calibrating the loss.

This PA is also integrated into the RFID reader transceiver chip[15]. According to the system measurements with a digital baseband, the reader with an integrated PA can read the information reflected by the passive tag.

5. Conclusion

A linear PA used for a RFID reader was implemented in CMOS 0.18-μm technology. With an output matching network and a harmonic control strategy, measurements show that this PA achieves a saturated power of 21.1 dBm, a power gain of 23.3 dB and a maximum PAE of 35.4% from a 1.8 V supply at 900 MHz. The harmonics are measured to be less than −40 dBc at its 1 dBCP.

Table 1 summarizes the performances of this work, and makes comparisons with similar work. From this table, it can be seen that the performances of this work are comparable with other work from a 1.8 V supply. Other work with higher power supplies do not emphasize the matching network, so the output power and efficiency may suffer from a little degradation.

References

[1] Bruccoleri F, Klumperink E A M, Nauta B. Wide-band CMOS low-noise amplifier exploiting thermal noise canceling. IEEE J Solid-State Circuits, 2004, 39(2): 275

[2] Zhuo W, Embabi S, de Gyvez J P, et al. Using capacitive cross-coupling technique in RF low noise amplifier and down-conversion mixer design. IEEE Proc ESSCIRC, 2000: 77

[3] Chen S F, Lee Y B, Sun C H, et al. A 65 nm CMOS low-noise direct-conversion transmitter with carrier leakage calibration for low-band EDGE application. IEEE Proc RFIC, 2009: 193

[4] Lee T H. The design of CMOS radio-frequency integrated circuits. 2nd ed. Beijing: Publishing House of Electronics Industry, 2005

[5] Lu Lei, Zhou Feng, Tang Zhangwen, et al. Equivalent model and parameter extraction of center-tapped differential inductors. Chinese Journal of Semiconductors, 2006, 27(12): 2150

[6] Kang J, Yoon J, Min K, et al. A highly linear and efficient differential CMOS power amplifier with harmonic control. IEEE J Solid-State Circuits, 2006, 41(6): 1314

[7] Gu Q. RF system design of transceivers for wireless communications. New York: Springer, 2005

[8] Jeong J, Pornpromlikit S, Asbeck P M, et al. A 20 dBm linear RF power amplifier using stacked silicon-on-sapphire MOSFETs. IEEE Microw Wireless Compon Lett, 2006, 16(12): 684

[9] Cripps S C. RF power amplifiers for wireless communications. 2nd ed. Norwood: Artech, 2006

[10] Han J, Kim Y, Park C, et al. A fully-integrated 900-MHz CMOS

power amplifier for mobile RFID reader applications. IEEE Proc RFIC, 2006

[11] Sowlati T, Leenaerts D M W. A 2.4-GHz 0.18 μm CMOS self-biased cascode power amplifier. IEEE J Solid-State Circuits, 2003, 38(8): 1318

[12] Yen C C, Chuang H R. A 0.25-μm 20-dBm 2.4-GHz CMOS power amplifier with an integrated diode linearizer. IEEE Microw Wireless Compon Lett, 2003, 13(2): 45

[13] Wang C, Vaidyanathan M, Larson L E. A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers. IEEE J Solid-State Circuits, 2004, 39(11): 1927

[14] EPC UHF radio frequency identity protocols: Class 1 Generation 2 UHF RFID Ver. 1.2.0, EPC global, 2007

[15] Tan Xi, Liu Yuan, Lu Lei, et al. A 1.8 V CMOS direct conversion receiver for 900 MHz RFID reader chip. Journal of Semiconductors, 2008, 29(9): 1734

[16] Si W W, Mehta S, Samavati H, et al. A 1.9-GHz single-chip CMOS PHS cellphone. IEEE J Solid-State Circuits, 2006, 41(12): 2737