An eighth order channel selection filter for low-IF and zero-IF DVB tuner applications*

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Abstract: An eighth order active-RC filter for low-IF and zero-IF DVB tuner applications is presented, which is implemented in Butterworth biquad structure. An automatic frequency tuning circuit is introduced to compensate the cut-off frequency variation using a 6-bit switched-capacitor array. Switched-resistor arrays are adopted to cover different cut-off frequencies in low-IF and zero-IF modes. Measurement results show that precise cut-off frequencies at 2.5, 3, 3.5 and 4 MHz in zero-IF mode, 5, 6, 7 and 8 MHz in low-IF mode can be achieved, 60 dB frequency attenuation can be obtained at 20 MHz, and the in-band group delay agrees well with the simulation. Two-tone testing shows the in-band IM_3 achieves –52 dB and the out-band IM_3 achieves –55 dB with –11 dBm input power. This proposed filter circuit, fabricated in a SMIC 0.18 μm CMOS process, consumes 4 mA current with 1.8 V power supply.

Key words: active-RC filter; Butterworth; frequency tuning; group delay; noise; linearity

DOI: 10.1088/1674-4926/30/11/115002 **EEACC:** 1270

1. Introduction

In digital video broadcasting (DVB) tuner systems, shown in Fig. 1, wide bandwidth and high linearity requirements make analog-to-digital converters (ADC) difficult to implement. To obtain a good adjacent channel rejection (ACR) before ADC, a high-order analog filter is adopted to achieve good attenuation and an active-RC architecture is selected to achieve high linearity. The cut-off frequency of an integrated active-RC filter is determined by on-chip resistors and capacitors which may vary greatly with the process, voltage and temperature (PVT). Thus, an automatic frequency tuning (AFT) circuit should be engaged to calibrate the cut-off frequency variation.

For DVB-T/H protocols, different signal bandwidths, such as 5, 6, 7 and 8 MHz, have been defined. To cover all these signal bandwidths, a programmable channel selection filter with switched-capacitor arrays and switched-resistor arrays is proposed in this paper. In zero-IF mode, the channel selection filter covers the cut-off frequencies of 2.5, 3, 3.5 and 4 MHz. Halving the switched-capacitor value automatically, this filter can also be switched to low-IF mode, in which the corresponding cut-off frequencies are 5, 6, 7 and 8 MHz respectively.

This paper also illustrates the system requirements of noise and linearity in detail, shows the circuit design, including the selection of biquad structures, amplifier design and AFT tuning circuit, and proposes critical design insights to minimize the non-ideal factors which will affect tuning precision.

2. System requirements

The specification of an analog filter can be summarized as two parts: the first part is the ACR, which includes the cut-off frequency and frequency attenuation; the second part is the error vector magnitude (EVM) loss, which includes the in-band ripple, group delay, noise and linearity. The in-band ripple and group delay determine the quality of the signal transfer function, and the noise and linearity determine the EVM loss caused by the analog filter itself. Here, the critical system requirements will be discussed.

2.1. Noise and linearity

In DVB tuner receivers, noise figure (NF) and linearity are critical performance parameters, which affect the system signal-to-noise ratio (SNR). The definition of sensitivity is:

$$P_{\text{in, min}} = KT + \text{NF} + 10\lg B + \text{SNR}_{\text{min}}. \tag{1}$$

To meet the minimum SNR requirement,

$$\text{NF} < P_{\text{in, min}} - KT - 10\lg B - \text{SNR}_{\text{min}}. \tag{2}$$

Linearity can be defined in different forms, such as IIP_3, $P_{1\text{dB}}$, composite second order distortion (CSO) and composite triple beat distortion (CTB). Because CSO, CTB and $P_{1\text{dB}}$ have a direct relationship with IIP_3[1], only IIP_3 will be considered here. In DVB tuner systems, the adjacent interferences become a bottleneck of the linearity requirement; DVB-T/H protocols clearly show that adjacent channels may be 40 dB larger than the desired channel. To assure enough SNR, the

* Project supported by the National High Technology Research and Development Program of China (No. 2007AA01Z282).

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Received 5 May 2009, revised manuscript received 26 May 2009

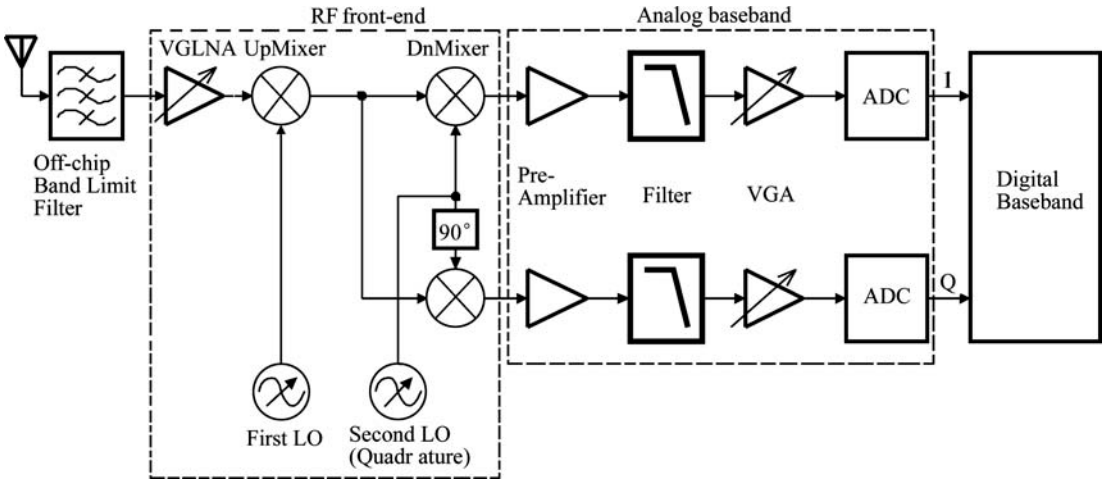

Fig. 1. Architecture of RF tuner.

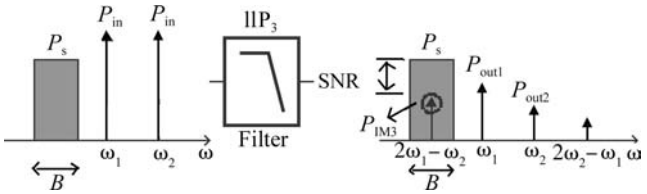

Fig. 2. IIP_3 calculation for analog filter.

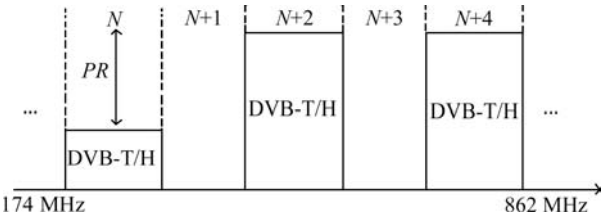

Fig. 3. Pattern L3 in the case of channel $N+2$ or $N+4$ for DVB-T/H.

product of IM_3 must be rigidly constrained. Assume that there are two interferential signals P_{in} in adjacent channels with the same power, and P_s is the power of the desired channel, as shown in Fig. 2.

According to the IIP_3 definition of an analog filter with 0 dB gain,

$$\mathrm{IIP_3} = P_{in} + \frac{P_{in} - P_{IM3}}{2}. \tag{3}$$

To meet the minimum SNR,

$$P_s - P_{IM3} > \mathrm{SNR_{min}}. \tag{4}$$

Substituting Eq. (3) into Eq. (4), the following can be derived:

$$\mathrm{IIP_3} > P_{in} + \frac{P_{in} - P_s + \mathrm{SNR_{min}}}{2} = P_{in,max} + \frac{\mathrm{PR} + \mathrm{SNR_{min}}}{2}, \tag{5}$$

where $P_{in} - P_s$ is defined as the protection ratio (PR).

For the modules in front of the channel selection filter in DVB tuners, adjacent interferences in the $N+2$ and $N+4$ channels are the primary non-linearity contributors, because the adjacent interferences in the $N+2$ and $N+4$ channels are much larger than the others. But for the modules behind the channel selection filter, such as VGA and ADC, the adjacent interferences in the $N \pm 1$ channels are the major non-linearity contributors, because the interferences in the other channels can be attenuated by the channel selection filter. Now, the pattern L3 of DVB-T/H protocols[2] is chosen to determine the NF and IIP_3 of the channel selection filter. This pattern has one digital DVB-T/H signal on the channel $N+2$ and another digital DVB-T/H signal on the channel $N+4$ in addition to the desired DVB-T/H signal on the channel N, as shown in Fig. 3.

The most rigid requirements of adjacent interferences are given in Table 1, where reference BER is defined as BER = 2×10^{-4} after Viterbi decoding.

The noise and linearity requirements are determined by the minimum and maximal input power separately. In our system design, the input power of the channel selection filter is controlled between –35 and –15 dBm by an automatic gain control (AGC) loop. The SNR requirements for digital demodulation are listed in Table 1. If a 3 dB margin is considered, the SNR requirement should be 26 dB for DVB-T and 20 dB for DVB-H. According to Eqs. (2) and (5), the requirements of NF and out-band IIP_3 of DVB-T protocol can be obtained as follows,

$$\begin{aligned}\mathrm{NF} &< P_{in,\,min} - KT - 10\lg B - \mathrm{SNR_{min}} \\ &= (-35 + 174 - 69 - 26)\,\mathrm{dB} = 44\,\mathrm{dB},\end{aligned} \tag{6}$$

$$\begin{aligned}\mathrm{IIP_3} &> P_{in,max} + \frac{\mathrm{PR{+}SNR_{min}}}{2} \\ &= \left(-15 + \frac{32 + 26}{2}\right)\mathrm{dBm} = 14\,\mathrm{dBm}.\end{aligned} \tag{7}$$

For DVB-H protocol, the requirements of NF and out-band IIP_3 can be given,

$$\begin{aligned}\mathrm{NF} &< P_{in,\,min} - KT - 10\lg B - \mathrm{SNR_{min}} \\ &= (-35 + 174 - 69 - 20)\,\mathrm{dB} = 50\,\mathrm{dB},\end{aligned} \tag{8}$$

$$\begin{aligned}\mathrm{IIP_3} &> P_{in,max} + \frac{\mathrm{PR{+}SNR_{min}}}{2} \\ &= \left(-15 + \frac{42 + 20}{2}\right)\mathrm{dBm} = 16\,\mathrm{dBm}.\end{aligned} \tag{9}$$

Table 1. Immunity to pattern L3 and SNR requirements of digital demodulation for DVB-T/H.

Protocol	Mode	PR	SNR (Portable P_1)	BER
DVB-T	2K/4K/8K 64QAM CR = 2/3 GI = All	32 dB	23 dB	4
DVB-H	2K/4K/8K 16QAM CR = 2/3 GI = All	42 dB	17 dB	6

Table 2. Filter specifications.

Filter specification	Value
Supply voltage	1.8 V
Power consumption	< 6 mA
–3 dB frequency	2.5, 3, 3.5, 4 MHz, 5, 6, 7, 8 MHz
Input power	–35 to –15 dBm
Pass-band ripple @ 2.5, 3, 3.5, 4 MHz @5, 6, 7, 8 MHz	< 2 dB
Attenuation @ 20 MHz	60 dB
In-band group delay variation	< 1 μs
Out-band IIP_3	> +16 dBm
Noise figure	< 44 dB
Tuning error	±5%

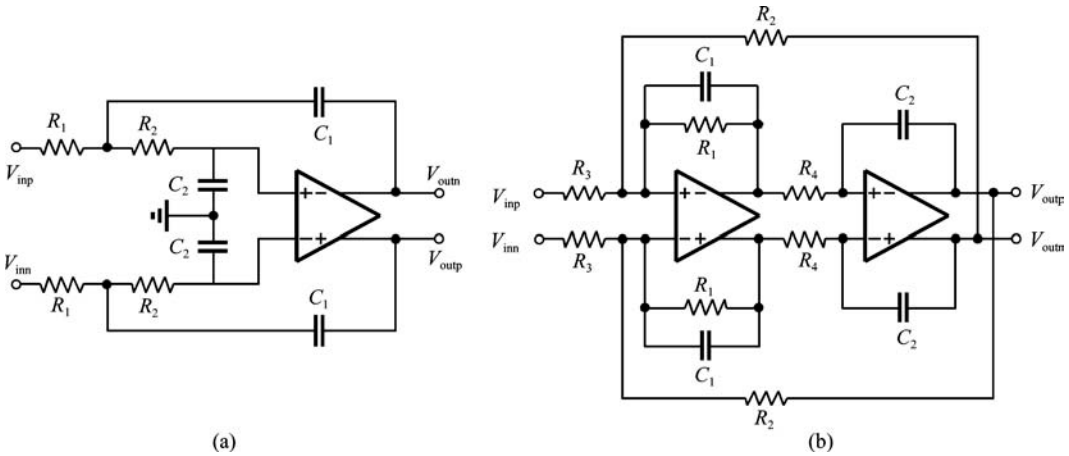

Fig. 4. (a) Sallen-Key biquad; (b) Tow-Thomas biquad.

So, the minimum requirement of NF is 44 dB, and the maximal requirement of out-band IIP_3 is +16 dBm.

2.2. Other issues

The main purpose of the analog channel filter in RF receiver is to select the desired signal and provide anti-aliasing for the following ADC. Channel selection can be achieved in either analog or digital domains. The implement in analog domain increases the dynamic range requirement of analog filter, but lowers the ADC's resolution. However, a digital filter can conquer the variation of components, the phase and gain error suffered by the analog filter, but requires increased resolution and dynamic range of ADC. The power of ADC will swiftly increase as the resolution requirement increases[3], which can be shown as,

$$P_{\mathrm{ADC}} = E_{\mathrm{conv}} \times 2^N \times f_{\mathrm{S}} \,(\text{Nyquist-Rate ADC}), \qquad (10)$$

where E_{conv} is the required power for one bit, 2^N is the number of bits, and f_{S} is the sample rate. Detailed power optimization between the channel selection filter and Nyquist-rate ADC is given in Ref. [4].

According to the requirements of ACR and anti-aliasing, this filter should achieve 60 dB attenuation at 20 MHz and the precision of the cut-off frequency should be controlled within ±5%. In this paper, an eighth order Butterworth filter is chosen here for the flat pass-band and sharp transition-band frequency response, and an AFT tuning circuit is engaged to compensate the cut-off frequency variation. Detailed filter specifications are given in Table 2.

3. Filter circuit design

3.1. Biquad selection

Sallen-Key and Tow-Thomas are the two most popular biquads in filter design, as shown in Fig. 4. Two poles are implemented in the Sallen-Key biquad, using only one amplifier, but two amplifiers are used in the Tow-Thomas biquad. Compared with the Tow-Thomas biquad, the Sallen-Key biquad has an obvious advantage in power consumption. But, in fact, the

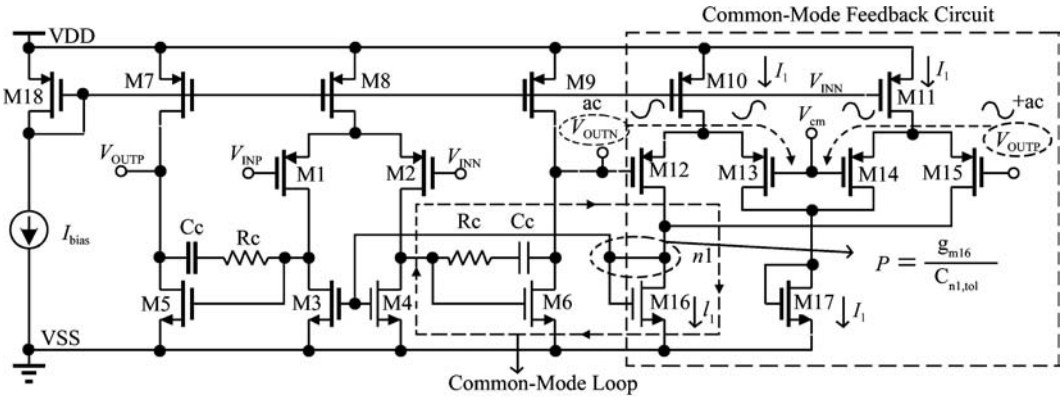

Fig. 5. A fully differential two-stage amplifier.

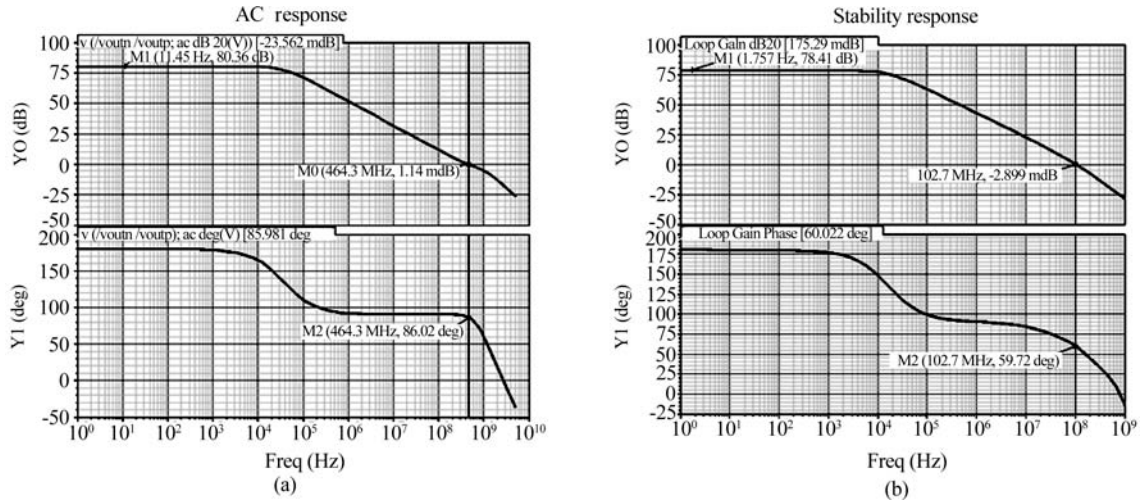

Fig. 6. (a) Bode diagram of differential-mode signal; (b) Bode diagram of common-mode signal.

Sallen-Key biquad is more sensitive to PVT variation than the Tow-Thomas biquad, and its performance at high frequencies is susceptible to parasitic capacitance. Thus, here the Tow-Thomas biquad is a better choice for a high-order filter.

This eighth order Butterworth filter consists of four cascaded biquads. The high Q biquad is placed in the head of the filter chain to optimize the noise performance. Here, the capacitors are designed to be a programmable switched-capacitor array with binary-weighting to obtain an adjustable RC constant, which is controlled by 6-bit digital signals. The selection of resistor and capacitor value is a trade-off between die area and power.

3.2. Amplifier design

The amplifier in the Tow-Thomas biquad is shown in Fig. 5. A fully differential two-stage amplifier is selected to improve the differential gain and drive the following resistor load. A common-mode feedback circuit is introduced to stabilize the common-mode outputs of the fully differential two-stage amplifier. The gates of transistors M12 and M15 connect with the amplifier outputs to detect the common-mode voltage. Compared with the voltage $V_{\rm cm}$, the error of common-mode voltage is fed back through the bias network M16, M3 and M4, and finally works on the voltage $V_{\rm outp}$ and $V_{\rm outn}$. A pole which located at $p = g_{\rm m16}/C_{\rm n1,tol}$ is additionally introduced into the common-mode loop. The gain of the common-mode circuit should not be set too large to avoid affecting the stability of the common-mode loop. The GBW of the amplifier should be wide enough to conquer the gain peaking around the cut-off frequency. The GBW requirement can be shown as[5]

$$\mathrm{GBW} \geqslant \left|\frac{A_{\rm C}(\mathrm{j}\omega_{\rm C})}{\delta - 1}\right| \left|\left[1 + A_{\rm C}\left(\mathrm{j}\omega_{\rm C}\right)\right]\omega_{\rm C}\right|, \qquad (11)$$

where $A_{\rm C}(\mathrm{j}\omega_{\rm C})$ is the open loop gain of the amplifier, $\omega_{\rm C}$ is the cut-off frequency of the filter, and δ is the error in the transform function. The simulation results show the differential-mode GBW 464 MHz with phase margin 86°, and the common-mode GBW 103 MHz with phase margin 60°. The power consumption is 490 μA for every amplifier.

3.3. Tuning circuit design

An accurate cut-off frequency is necessary in the channel selection filter to satisfy both channel selection and ACR. To meet the ±5% frequency variation required by the system, a Master–Slave tuning circuit is introduced to adjust the absolute precision by relative precision. Every tuning circuit needs an absolute reference. Commonly, there are only two absolute references, which are bandgap voltage and crystal frequency. Here the frequency of the crystal oscillator is chosen to keep

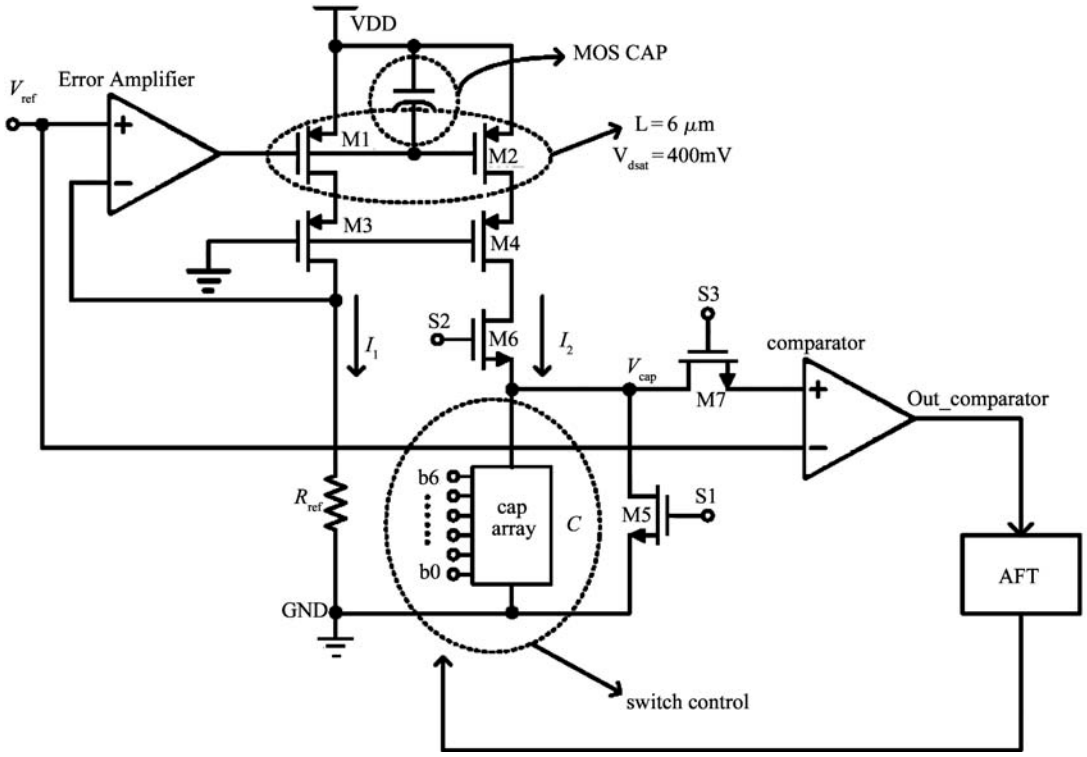

Fig. 7. Tuning circuit.

the same dimension with constant RC. The method of realizing RC tuning is to adjust the switched-capacitor array. The overall schematic of the proposed tuning circuit is shown in Fig. 7[6].

A voltage reference obtained from the bandgap output after voltage division separately connects the inputs of error amplifier and comparator. A current reference of $I_1 = V_{\rm ref}/R_{\rm ref}$ can be obtained through the feedback of the error amplifier, and then a mirror current I_2 can be generated to charge the switched-capacitor array to a voltage $V_{\rm cap}$. $V_{\rm cap}$ and $V_{\rm ref}$ voltages are compared in a comparator. The comparison result enters into the AFT algorithm to form a feedback loop. By controlling the digital input signals of the switched-capacitor array, $V_{\rm cap}$ will be equal to $V_{\rm ref}$ after tuning. The process can be shown as follows:

$$V_{\rm cap} = \frac{Q}{C} = \frac{I_2\Delta t}{C} = \frac{I_1\Delta t}{C} = \frac{V_{\rm ref}}{R_{\rm ref}C}\Delta t, \tag{12}$$

$$\Delta t = R_{\rm ref}C, \tag{13}$$

where Δt is the period multiples of the reference clock. $R_{\rm ref}$ is the on-chip poly resistor. The resistor $R_{\rm ref}$ and the capacitor C in the tuning circuit match the ones in the filter core circuit. So the constant time $R_{\rm ref}C$ is determined by Δt after tuning and maintains relative precision with the constant time of the filter core circuit. In other words, the cut-off frequency is tuned to maintain the relative precision with the frequency of the reference clock.

Some useful design considerations are proposed as follows. The amplifier offset, including random offset and systematic offset, affects the comparison result. Random offset can be minimized by engaging big sizes and small overdrive voltages of input transistors. In Fig. 7, if the comparator is the same as the error amplifier, the systematic offset will be cancelled. The consideration of current mirrors is to minimize the difference between currents I_2 and I_1 during the whole charging process. Here, the cascode transistors are used to improve the output resistance for good DC matching. The channel length of the current mirrors is 6 μm and the overdrive voltage of M1 and M2 transistors is designed to be as large as 400 mV to improve the matching, while there is still a trade-off when sizing M1 and M2, because large transistors may deteriorate clock feed-through effects, which will worsen dynamic current mismatch. The MOS capacitor is engaged to reduce clock feed-through. When the switched-capacitor array is charging, $V_{\rm cap}$ increases at the same time, and the current I_2 will vary non-linearly. Thus, the value of $V_{\rm ref}$ cannot be set too high. Meanwhile, the charging current should be designed carefully to get a reasonable charging time.

The detailed timing plan in one comparison step is illustrated in Fig. 8. The sizes of all the switches are as small as possible to decrease the charge injection. When the transistor M5 turns on, the voltage $V_{\rm cap}$ is discharged to GND. The lager size of the transistor M5 will help to lower the turn-on resistor but increase the charge injection; it is a trade-off. When the transistor M6 turns on, the current I_2 is generated by current mirrors. An initial time is usually needed for current settling, which will cause dynamic current mismatch. Since the transistor M6 is already on before the transistor M5 turns off, the initial settling is avoided to charge the capacitor C.

A binary-search algorithm is employed in AFT control logic to save calibration time. The clock frequency is 12.5 MHz. The whole calibration needs six comparison steps,

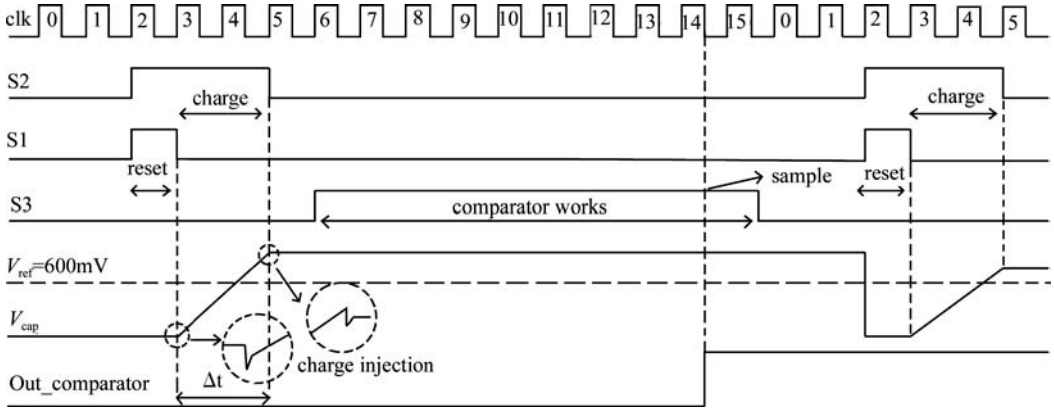

Fig. 8. Detailed timing plan in one comparison step.

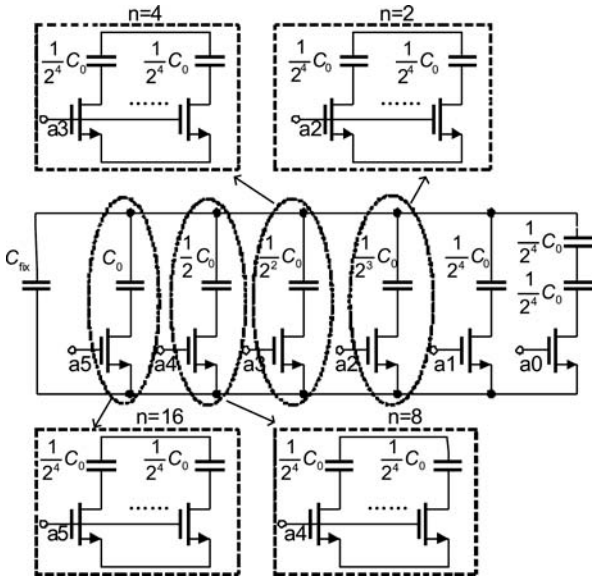

Fig. 9. 6-bit digital controlled switched-capacitor array.

taking only 7.68 μs.

3.4. Tuning error

Error factors which affect the tuning precision can be summarized as follows: quantization error of the switched-capacitor array, resistor and capacitor mismatch between the master and slave circuits, current mismatch, offset voltage of the comparator, charge injection of MOS switches, clock feed-through, etc.

The programmable switched-capacitor array in Fig. 9 is considered as a capacitor digital-to-analog converter (CAP-DAC) whose input is a digital signal and output is capacitance.

$$C_{\max} = C_{\text{fix}} + \left(2 - \frac{1}{2^{n-1}}\right) C_0, \tag{14}$$

$$C_{\min} = C_{\text{fix}}, \tag{15}$$

$$C_{\text{center}} = \sqrt{C_{\max} C_{\min}}. \tag{16}$$

The quantization error of CAP-DAC is

$$E_{\text{q}} = \frac{C_0/2^{n-1}}{C_{\text{center}}}, \tag{17}$$

where n is the number of digital control bits.

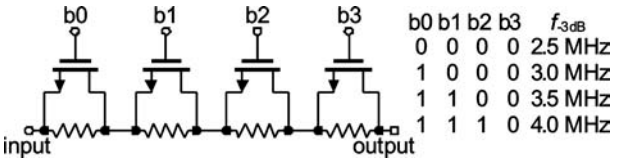

Fig. 10. Switched-resistor array.

To cover the ±20% variation of resistors and capacitors over different process corners and to satisfy ±5% tuning precision, $C_{\max}/C_{\min}$ = 2.25/1 and n = 6 are chosen, and the quantization error is 1.4%. Furthermore, in the same chip, the resistor and capacitor mismatch can be controlled within 0.5% and 0.2% separately with suitable size and excellent layout. Besides *RC* mismatch, current mismatch is another important contribution, which can be designed to be below 0.5%. All the other contributions such as charge injection and charge sharing should be controlled within 0.4%, thus the total tuning error can be controlled under ±3% in 4-MHz cut-off frequency mode, which is the calibration reference. Consider that the cut-off frequency will vary within ±2% when other cut-off frequency modes are selected, which will be shown below. Finally, the worst tuning error can be restricted below ±5%.

3.5. Adjustable cut-off frequencies in low-IF and zero-IF modes

In our DVB tuner, system design specifies that the cut-off frequency can be changed between 5, 6, 7 and 8 MHz to cover all the DVB-T/H protocols, and then the cut-off frequency also should be changed between 2.5, 3, 3.5 and 4 MHz for zero-IF architecture and between 5, 6, 7 and 8 MHz for low-IF architecture.

The precise cut-off frequency can be obtained by the tuning circuit above. When the tuning circuit finishes, the cut-off frequency of the filter can be changed between 2.5, 3, 3.5 and 4 MHz using a switched-resistor array in Fig. 10. All these cut-off frequencies maintain relative precision with each other so that only one cut-off frequency reference should be chosen to be tuned. Here, the cut-off frequency of 4 MHz is chosen to be tuned as the reference. The shunt impedance introduced by switch transistors should be considered to obtain precise matching between different cut-off frequencies. When the

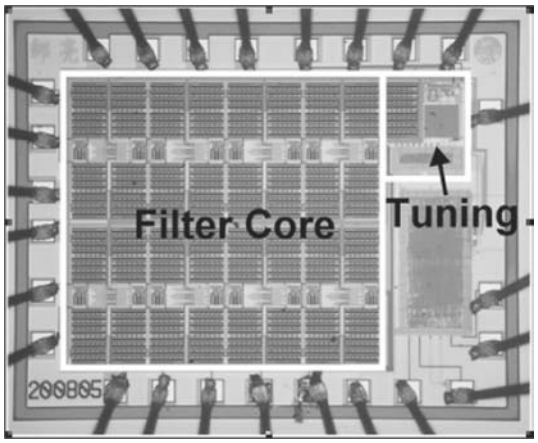

Fig. 11. Chip microphotograph.

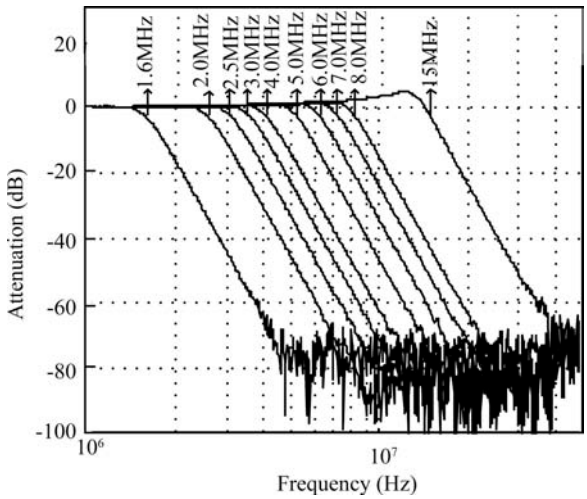

Fig. 12. Frequency response.

cutoff frequencies 2.5, 3, 3.5 and 4 MHz are achieved, we can obtain the other corresponding cut-off frequencies 5, 6, 7 and 8 MHz respectively by halving the switched-capacitor value automatically.

4. Experimental results

The proposed filter circuit was fabricated in SMIC 0.18 μm technology. A chip microphotograph is shown in Fig. 11, and die area of the filter including both I and Q channels is 1.03×0.93 mm^2 including 0.3×0.25 mm^2 for the AFT tuning circuit. An off-chip buffer is used to convert the differential signal into a single-end signal, providing a 50 Ω driver for the test purpose. 6 dB gain is introduced by this off-chip buffer. In Fig. 12, 60 dB ACR is achieved at 20 MHz in the 8-MHz cut-off frequency mode and frequency attenuation at the stop-band below –80 dB. The minimum –3 dB frequencies 1.6 MHz and maximal –3 dB frequencies 15 MHz can be achieved. Perfect stop-band attenuation will help to alleviate the out-band linearity requirement of the following VGA (variable gain amplifier) and provide good anti-aliasing performance for the following ADC.

Lots of measurement results show that the precision of the cut-off frequency 4 MHz, which is chosen as the calibration reference, can be tuned to less than ±3%, and all the other

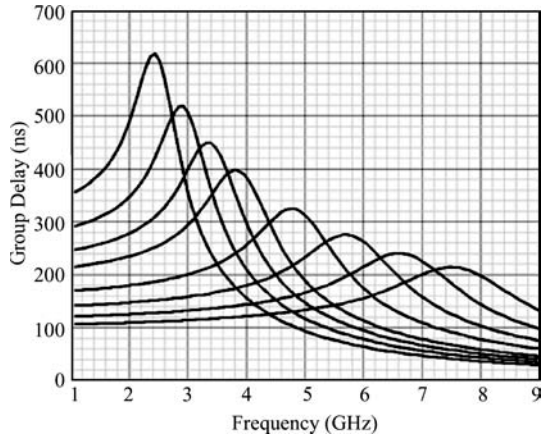

Fig. 13. Simulated group delay.

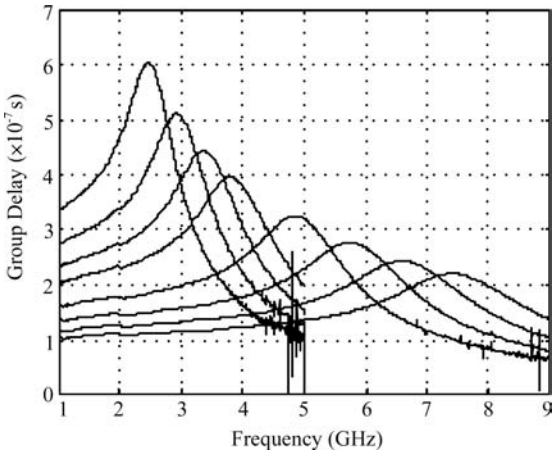

Fig. 14. Measured group delay.

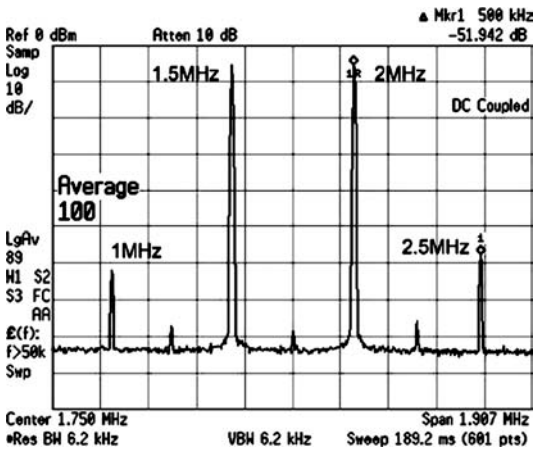

Fig. 15. Measured in-band IM_3.

cut-off frequencies ranging from 2.5 to 8 MHz can be tuned to less than ±5%. This is enough to satisfy both the requirement of ACR and EVM loss. In Figs. 13 and 14, precise in-band group delay is achieved compared with the simulation results.

In Figs. 15 and 16, two-tone tests with input power –11 dBm are shown, which indicate that the in-band IM_3 achieves –52 dB with –11 dBm input power at 2 MHz & 1.5 MHz, and the out-band IM_3 achieves –55 dB with –11 dBm input power at 16 MHz & 28 MHz. So, the out-band IIP_3 can be calculated as +16.5 dBm, which satisfies the system requirements, and an in-band IIP_3 of +15 dBm can be obtained. Finally, the

Table 3. Summary of the measurement results.

Parameter	Value
Technology	0.18 μm CMOS process
Supply voltage	1.8 V
Power consumption	4 mA × 1.8 V = 7.2 mW
Area (for both I & Q channels)	1.03 × 0.93 mm^2 (Filter core) 0.3 × 0.25 mm^2 (Tuning circuit)
–3 dB frequency	2.5, 3, 3.5, 4 MHz, 5, 6, 7, 8 MHz
Pass-band ripple @ 2.5, 3, 3.5, 4 MHz @ 5, 6, 7, 8 MHz	< 1 dB < 2 dB
Attenuation @ 20 MHz @ Stop-band	> 60 dB > 80 dB
In-band group delay variation with different cut-off frequencies	120–300 ns
In-band IM$_3$ @ Input power –11 dBm (f_{-3dB} = 8 MHz, f_{signal} = 2 MHz & 1.5 MHz)	–52 dB (In-band IIP$_3$ +15 dBm)
Out-band IM$_3$ @ Input power –11 dBm (f_{-3dB} = 8 MHz, f_{signal} =16 MHz & 28 MHz)	–55 dB (Out-band IIP$_3$ +16.5 dBm)
Noise figure	41 dB
Tuning error @ f_{-3dB} 4 MHz @ The other f_{-3dB}	±3% ±5%
Tuning time	7.68 μs

Table 4. Performance comparison.

Reference	Ref. [6]	Ref. [7]	Ref. [8]	This work
Technology	0.18 μm CMOS	0.35 μm SiGe BiCMOS	0.18 μm BiCMOS	0.18 μm CMOS
Application	DAB/T-DMB tuner	DBS-tuner	—	DVB-T/H tuner
Supply (V)	1.8	5	2.7	1.8
Power consumption (mA)	4.5	13	4.3	4
Area (mm^2)	1.395	0.5	2.86	1.03
Filter orders	8	7	5	8
Cut-off frequency (MHz)	1.58	4–40	1.92	1.6–15
Stop-band attenuation (dB)	65	43	64	80
In-band IIP$_3$ (dBm)	+4.6	+10	+11	+15

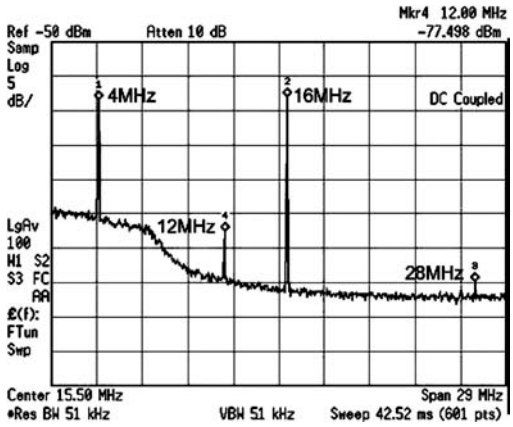

Fig. 16. Measured out-band IM$_3$.

performance of the proposed filter is summarized in Table 3, and a performance comparison is given in Table 4.

5. Conclusion

An eighth order active-RC filter with automatic frequency tuning for DVB tuner applications is proposed in this paper. The programmable cut-off frequency is tuned using switched-resistor arrays and switched-capacitor arrays, thus it can cover all the DVB-T/H protocols and is suitable for both low-IF and zero-IF architectures. Frequency response measurements show ±5% tuning precision and 60 dB frequency attenuation at 20 MHz. This will be useful to alleviate the requirements of the following VGA and ADC and reduce the effect of out-band blockers. The results of two-tone testing show –52 dB in-band IM$_3$ and –55 dB out-band IM$_3$ with –11 dBm input power. The proposed filter circuit, fabricated in a SMIC 0.18 μm CMOS process, consumes only 4 mA current with 1.8 V power supply.

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