A wideband CMOS VGLNA based on single-to-differential stage and resistive attenuator for TV tuners*

Han Kefeng(韩科锋), Tan Xi(谈熙)†, Tang Zhangwen(唐长文), and Min Hao(闵昊)

State Key Laboratory of ASIC & System, Fudan University, Shanghai 201203, China

Abstract: A wideband CMOS variable gain low noise amplifier (VGLNA) based on a single-to-differential (S2D) stage and resistive attenuator is presented for TV tuner applications. Detailed analysis of input matching, noise figure (NF) and linearity for S2D is given. A highly linear passive resistive attenuator is proposed to provide 6 dB attenuation and input matching for each gain stage. The chip was fabricated by a 0.18 μm 1P6M CMOS process, and the measurements show that the VGLNA covers a gain range over 36.4 dB and achieves a maximum gain of 21.3 dB, a minimum NF of 3.0 dB, an IIP3 of 0.9 dBm and an IIP2 of 26.3 dBm at high gain mode with a power consumption less than 10 mA from a 1.8 V supply.

Key words: S2D; VGLNA; TV tuner; attenuator; wideband; noise canceling

DOI: 10.1088/1674-4926/32/7/075003 **EEACC:** 1220

1. Introduction

The frequency plan of a DVB-T poses a great challenge towards the design of a LNA over such a wideband of frequency (50–860 MHz) because a traditional narrow band LNA cannot cover the full band and the frequency of 50 MHz is also a nightmare in realizing an on-chip LC tank. A tunable LNA suffers from the same problem. As a result, a wideband LNA shows its superiority over other solutions. With the technique of noise canceling proposed in 2003[1], the NF can be lowered to 2 dB, thus it is more practical to implement a wideband low noise receiver, such as a TV tuner[2] or SDR receiver[3].

Designing a LNA for a TV tuner pose three problems. The first one is the wideband requirement, which is no more a problem with the scaling property of CMOS technology — the measured 3 dB bandwidth of LNA can be up to several giga hertz[7]. However, flicker noise is a problem at 50 MHz for CMOS technology. The second is a linearity problem because the input signal without filtering contains more than 100 channels allocated to the received band, so the 2nd and 3rd inter-modulation distortions are much more serious than for narrow band receivers (e.g. GSM)[5, 12]. The last one is that the input signal level can be up to 0 dBm when receiving all of the channels each with a strong power, so an attenuation strategy is generally considered[2, 6, 14].

This paper presents a highly linear, low-noise wideband VGLNA based on a S2D and resistive attenuator for TV tuner applications[9]. A new insight into noise in S2D is given. An attenuator employing an RF switch with fewer parasitics and better linearity is presented.

2. Single-to-differential stage

The S2D stage with a history of over 20 years[10] has drawn a lot of attention recently. With the proposal of a noise canceling technique in wideband LNAs, S2D is predicted to be a wideband low noise amplifier owing to noise cancellation[4]. S2D is also very linear because of distortion cancellation[4, 7]. As a result, this topology is well studied and adopted in some wideband receivers[8]. The well-known S2D (also called balun-LNA or active balun) is composed of a common gate (CG) stage with a common source (CS) stage, as shown in Fig. 1.

2.1. Input impedance

The impedance of the S2D seen from the input can be calculated as

$$Z_{\rm in}=\left[\frac{C_{\rm G}}{C_{\rm gs1}+C_{\rm G}}\left(g_{\rm m1}+sC_{\rm gs1}\right)+\frac{C_1}{C_{\rm gs2}+C_1}sC_{\rm gs2}\right]^{-1}. \tag{1}$$

Here, $C_{\rm G}$ is the capacitor (not shown here) connected to M1 for AC grounding and $g_{\rm m1}$ is the transconductance of CG. Assuming $C_{\rm G}\gg C_{\rm gs1}$ and $C_1\gg C_{\rm gs2}$, then $Z_{\rm in}$ is given as

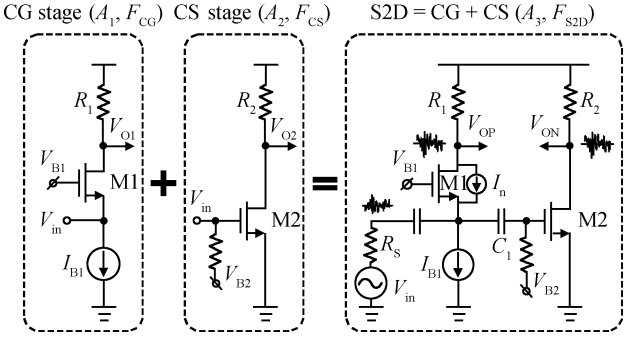

Fig. 1. CG and CS stages form a noise canceling S2D stage.

* Project supported by the National Science Funding of China (No. 60876019), the National S&T Major Project of China (No. 2009ZX0131-002-003-02), the Shanghai Rising-Star Program, China (No. 09QA1400300), the National Scientists and Engineers Service for Enterprise Program, China (No. 2009GJC00046), and the ASIC State-Key Laboratory Funding, China (No. 09MS007).

† Corresponding author. Email: tanxi@fudan.edu.cn

Received 19 December 2010, revised manuscript received 2 March 2011

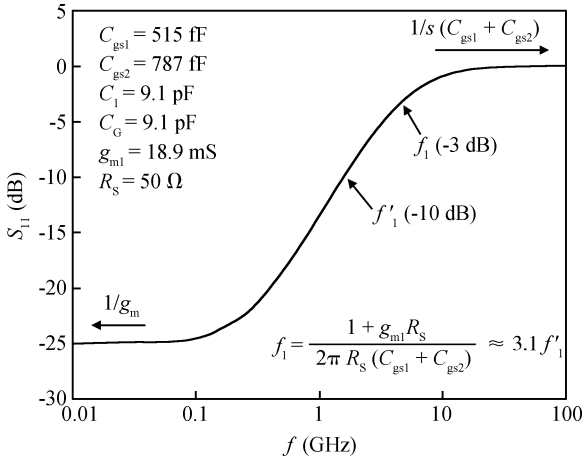

Fig. 2. Impact of parasitic capacitance on S_{11}.

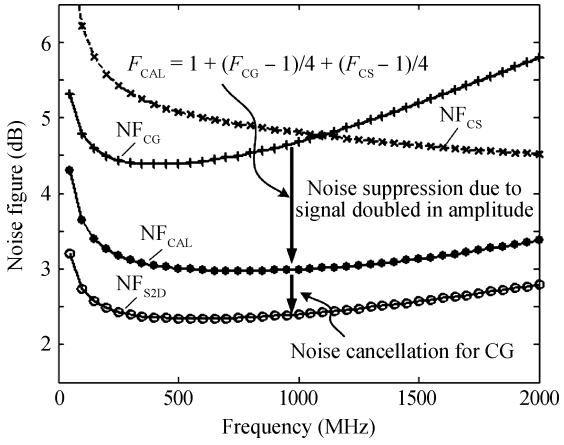

Fig. 3. Simulated NF for CG, CS and S2D respectively.

$$Z_{in} \approx \left[g_{m1} + s\left(C_{gs1} + C_{gs2}\right)\right]^{-1}. \quad (2)$$

As shown in Fig. 2, S_{11} depends on g_{m1} at low frequency, and parasitic capacitors C_{gs1} and C_{gs2} will deteriorate S_{11} when the frequency increases. With Eq. (2), the bandwidth for the acceptable limit (e.g. –10 dB) of S_{11} is determined by

$$f_{BW,-10dB} \approx \frac{1}{3.1}\frac{1+g_{m1}R_S}{2\pi R_S\left(C_{gs1}+C_{gs2}\right)}. \quad (3)$$

So the parasitic capacitance of C_{gs1} and C_{gs2} should be kept small for wideband input matching, and scaled L_{min} for MOS transistors will be very helpful towards the matching bandwidth $f_{BW,-10dB}$[7].

2.2. Voltage gain

The voltage gain (A_{CG}) of CG is $g_{m1}R_1$ and for a CS stage (A_{CS}) is $g_{m2}R_2$ regardless of the source impedance R_S. The small-signal voltage gain for a S2D stage is given by

$$A_{S2D} = \frac{g_{m1}R_1 + g_{m2}R_2}{1+g_{m1}R_S} = \frac{A_{CG}+A_{CS}}{1+g_{m1}R_S}. \quad (4)$$

2.3. Noise figure

With the condition of input matching, the noise factor for the CG stage is

$$F_{CG} = 1 + \gamma_1 + \frac{4}{g_{m1}R_1} = 1 + \gamma_1 + \frac{4}{A_{CG}}, \quad (5)$$

and the noise factor of CS stage is

$$F_{CS} = 1 + \frac{4\gamma_2}{g_{m2}R_S} + \frac{4}{g_{m2}R_S A_2}. \quad (6)$$

With a small-signal model for each noise source, the noise factor for the S2D stage is expressed as

$$F_{S2D} = 1 + \frac{\left(R_S A_{CS} - R_1\right)^2 \gamma_1 g_{m1} + 4R_2^2\gamma_2 g_{m2} + 4R_1 + 4R_2}{\left(A_{CG}+A_{CS}\right)^2 R_S}. \quad (7)$$

The first term in the polynomial means noise cancellation for CG. The condition for noise canceling is solved to be

$$A_{CS} = g_{m2}R_2 = g_{m1}R_1 = A_{CG}. \quad (8)$$

It can be learnt form Eq. (8) that all of the thermal noise generated from the CG transistor is eliminated when the outputs of S2D are balanced. So Equation (7) can be modified to

$$F_{S2D} = 1 + \frac{1}{g_{m1}R_1} + \frac{\gamma_2}{g_{m2}R_S} + \frac{1}{g_{m2}R_1}. \quad (9)$$

According to the noise analysis proposed in our previous work[9], the noise factor of S2D can be expressed as

$$\begin{aligned} F_{CAL} &= 1 + \frac{F_{CG}-1}{4} + \frac{F_{CS}-1}{4} \\ &= 1 + \frac{\gamma_1}{4} + \frac{1}{g_{m1}R_1} + \frac{\gamma_2}{g_{m2}R_S} + \frac{1}{g_{m2}R_1}. \end{aligned} \quad (10)$$

The cancelled part is $\gamma_1/4$ according to Eqs. (9) and (10). Actually, this part is a small portion of the overall noise, and a low noise factor is achieved for S2D mostly lies in the principle that useful signal doubles in amplitude at the differential outputs while the unrelated noises should be added in power[11], as shown in Fig. 3.

Moreover, if the ratio of R_1/R_2 is defined as k in the condition of Eq. (8), there is

$$k = R_1/R_2 = g_{m2}/g_{m1}. \quad (11)$$

Then the noise factor of S2D can be re-arranged as

$$F_{S2D} = 1 + \frac{1}{A} + \frac{\gamma_2}{k} + \frac{1}{Ak}. \quad (12)$$

Here, A is the voltage gain for CG and CS with Eq. (8). When varying A and k, NF contours can be plotted in Fig. 4.

Compared to our previous work[9], three points should be highlighted in noise optimization. Firstly, the noise generated from CG cannot be fully cancelled because the noises of CG to the differential outputs are not the same in amplitude, though a CR high pass path is added to the CG stage. Secondly, according to the figure plotted in Fig. 4, increasing power consumption of the CS stage and gain will lower the NF effectively,

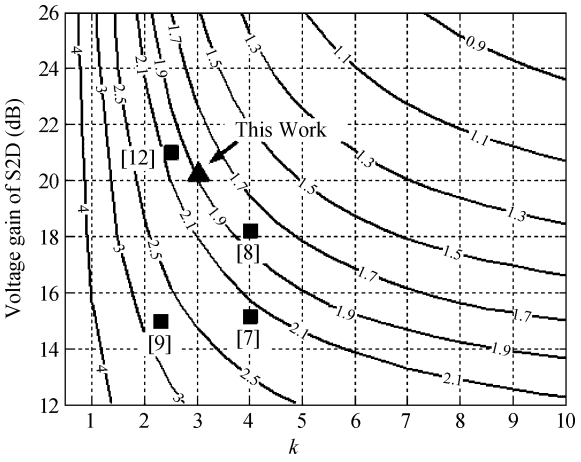

Fig. 4. Calculated NF (in dB) contours for S2D core.

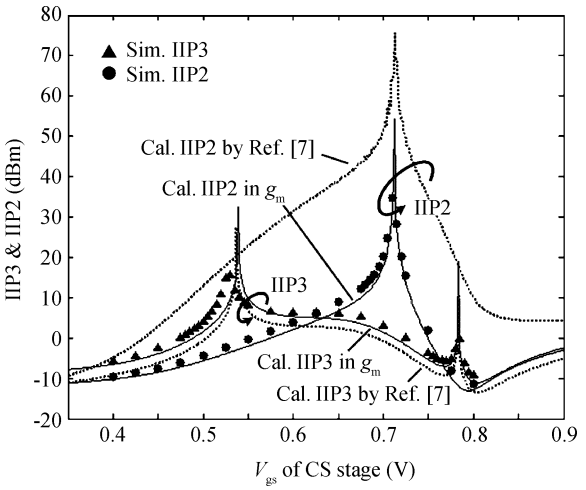

Fig. 5. IIP3 and IIP2 calculations from IV curves of the CS stage.

so a 0.9 dB NF improvement is achieved compared to Ref. [9] in Fig. 4. It is worth pointing out that the BW of S2D will be small because the loads are increased for the exchange of gain enhancement. Finally, if the noise from current bias is added, the contribution to the noise factor is $\gamma_1 g_{m3} R_S$ because it can be seen as an outside noise source to the S2D. The length L and over-drive voltage for this bias transistor should be kept large to lower the noise contribution. As a result, the overall expression for the noise factor is

$$F_{S2D} = 1 + \frac{1}{g_{m1} R_1} + \frac{\gamma_2}{g_{m2} R_S} + \frac{1}{g_{m2} R_1} + \gamma_3 g_{m3} R_S. \quad (13)$$

2.4. Linearity analysis

IIP3 and IIP2 can be optimized from the I–V curves of the CS stage[7], which dominates the non-linearity in S2D because the distortion in CG can be cancelled in the principle of noise cancellation. As stated in Ref. [13], the distortion mostly comes from g_m if the load resistance is small (such as 100 Ω). So the expressions for IIP3 and IIP2 of a single CS stage are

$$\mathrm{IIP2}_{\mathrm{dBm}} = 20 \lg \left| \frac{g_{m1}}{g_{m2}} \right| + 10\,\mathrm{dB}, \quad (14)$$

$$\mathrm{IIP3}_{\mathrm{dBm}} = 20 \lg \left| \sqrt{\frac{4 g_{m1}}{3 g_{m3}}} \right| + 10\,\mathrm{dB}. \quad (15)$$

Here, g_{mn} represents the nth order derivation from I–V curve, that is

$$g_{mn} = \frac{1}{n!} \frac{\mathrm{d}^n I_{DS}}{\mathrm{d} V_{GS}^n}. \quad (16)$$

Figure 5 shows the calculated results versus simulations for IIP2 and IIP3. The method in Ref. [7] overestimates the values of IIP2 by the technology used in this work while the g_m-based method gives a relative accurate prediction versus simulation results.

A diode connected load will improve the linearity performance because of the post-correction effect[9, 11]. However, the limitation is that the overdrive voltage should be kept large enough for a higher gain and a lower NF. As a result, the large overdrive voltage will drive the CG transistor into the triode region. In Ref. [9], IIP2 performance (8.6 dBm) is not good enough without any optimization; actually, the specification should be 20 dBm or more[7], so if a higher IIP2 is wanted, the bias voltage of CS should be chosen carefully, such as 0.71 V according to Fig. 5, though IIP3 degrades a little but the value is still above 0 dBm.

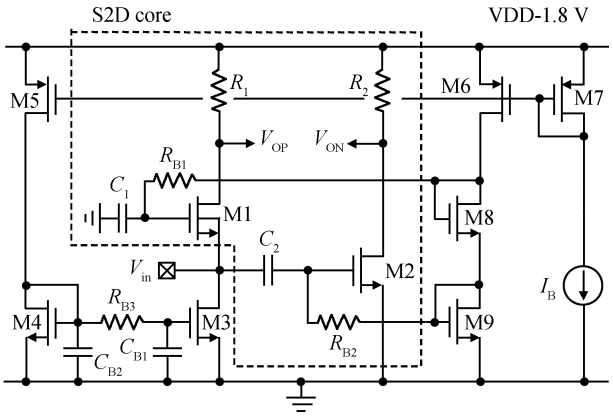

Fig. 6. Schematic for the S2D stage with bias branch.

2.5. Phase and magnitude imbalance

It is impractical to realize a perfect matching between CS and CG stages, so gain and phase errors do exist for the differential outputs. As stated in Section 2.3, the transconductance of CS should be k times as the CG stage, so is the ratio of load resistance for CG over CS. Accordingly, a 3 dB bandwidth for CG is much smaller than the CS stage, and thus the phase and gain error increase with frequency, and the parasitic capacitance should be kept as small as possible for the layout.

2.6. S2D circuit design

The schematic of S2D is given in Fig. 6. M1 with R_1 forms a CG stage for in-phase amplification and M2 with R_2 is configured as the CS stage for anti-phase path. In order to reduce the impact of flicker noise at low frequency, a 0.3 μm length transistor is chosen. M1 is of the DNW transistor to eliminate the body effect. M3 is a current bias for M1 and the channel

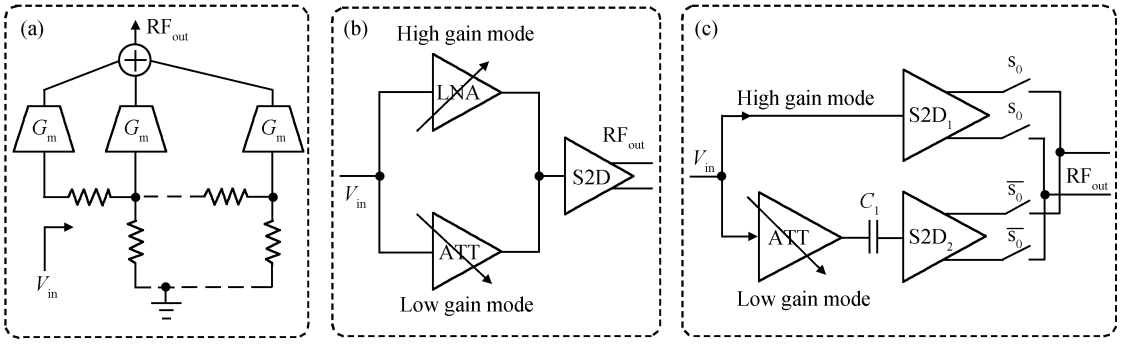

Fig. 7. (a) Tapped attenuator. (b) Two gain modes front-end. (c) Two gain modes with S2D.

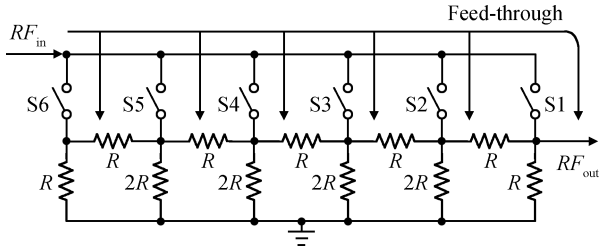

Fig. 8. Schematic of the 6-step resistive attenuator.

length is set to 1 μm. C_1 is AC grounding for CG, and C_2 is for DC blocking of M2. The bias voltages of CG and CS come from diode-connected transistors. The CG draws 1.6 mA and CS stage consumes 7.5 mA, and the total current of S2D including the bias is less than 10 mA from the supply.

3. Attenuator design

A passive attenuator can be either capacitive or resistive. A capacitive network is sensitive to parasitics so the gain step cannot be easily controlled. In addition, it needs an extra input matching part[14]. A resistive network can match the source impedance easily with an accurate gain step. Figure 7(a) shows a tapped resistive attenuator with one G_m-stage for each step, and the matching is done by attenuator, so the NF is not good enough[15]. Figure 7(b) is composed of two gain modes; this topology can achieve a low NF but with poor IIP2 performance for the single-ended LNA[16]. The scheme of this work is shown in Fig. 7(c); this is similar to Fig. 7(b) but in replace of two S2Ds, so this choice has good performance in both noise and linearity[9].

The presented attenuator is based on a R–$2R$ ladder, as shown in Fig. 8. In this way, the attenuator shows an input impedance of $(2/3)R$ for each step, so R is 75 Ω for a 50 Ω system. The switches are of a single NMOS transistor in the triode region, so the turn-on resistance is

$$R_{\rm on} = \frac{L}{\mu C_{\rm ox} W \left(V_{\rm gs} - V_{\rm T}\right)}. \tag{17}$$

In a traditional way, a simple NMOS is applied with relatively good linearity when the signal is weak. However, as the input level increases, the distortion increases dramatically because $V_{\rm gs}$ is no more a constant and hence the switch behaves non-linearly. A modified scheme[17] is with a resistor at the gate, which forms a high pass path, and the voltage at gate follows the input signal, so $V_{\rm gs}$ is a constant and the linearity improves. To gain a better linearity performance, a new RF switch is adopted, as shown in Fig. 9. $R_{\rm b}$ is placed at the terminal of the body because $C_{\rm sb}$ also introduces distortion and the threshold voltage related to $V_{\rm sb}$ too. The simulation results are shown in Fig. 10 for the NMOS switch with dimensions of 100 μm/0.18 μm. When a two-tone signal with frequencies of 495 MHz and 505 MHz is applied to the different types of switch, a 19 dB improvement of IM3 is achieved for the adopted switch to a traditional one at an input level of 0 dBm.

An additional benefit of this topology is that the input parasitic capacitance is greatly reduced due to resistors of $R_{\rm g}$ and $R_{\rm b}$. According to the simulations, the equivalent input capacitance is 392 fF for a switch of 100 μm/0.18 μm, when a resistor $R_{\rm g}$ is applied to the gate, the value is reduced to 212 fF, and the adopted topology shows a capacitance of less than 10 fF.

As shown in Fig. 8, a great limitation for the gain range of the attenuator is the feed-through effect, which also degrades the linearity performance simultaneously. The feed-through relates to switch dimensions; a larger switch will bring in poor isolation performance but with improvement of linearity. So the switches of S1–S7 are of different dimensions and a trade-off must be made between linearity, gain steps and input matching. The dimension of S1 should be much less than S7 because the feed-through is most serious at this branch. The layout also plays an important role in the proposed attenuator, especially for the source and drain connections in the switches, because the parasitic capacitance can also introduce serious feed-through to the output. As a result, the gain range of this design is larger than our previous work[9] with a similar topology.

4. Chip fabrication and measurements

This chip was fabricated by a SMIC 0.18 μm 1P6M CMOS process. It accounts for an area of 0.54 mm^2 with ESD protected PADs and the core area of S2D is 0.06 mm^2, as shown in Fig. 11.

The measured S_{11} for all gain steps are plotted in Fig. 12. Even in the worst case, S_{11} is still below –10 dB from 50 MHz to 1.2 GHz.

The gains of each step are firstly measured from 10 MHz to 1 GHz in Fig. 13. Because a source follow buffer and an off-chip balun with a ratio of 2 : 1 are applied for testing, so an extra 9 dB should be added to S_{21} to calculate voltage gains.

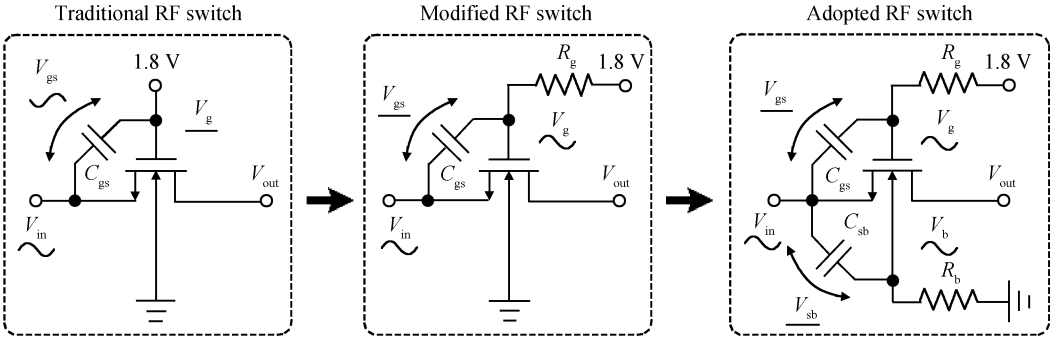

Fig. 9. Analysis of different types of RF switches.

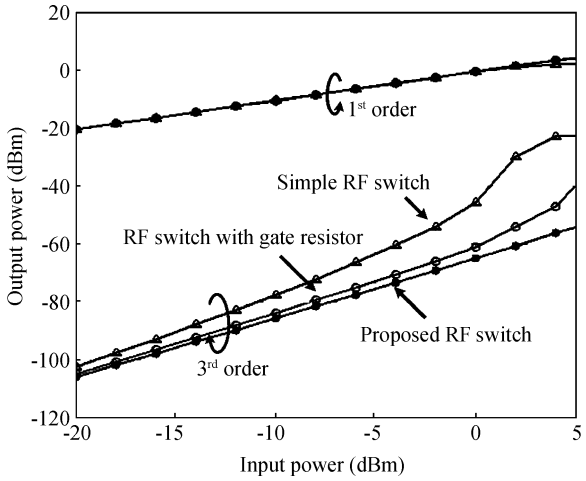

Fig. 10. Simulated IM3 for different types of RF switches.

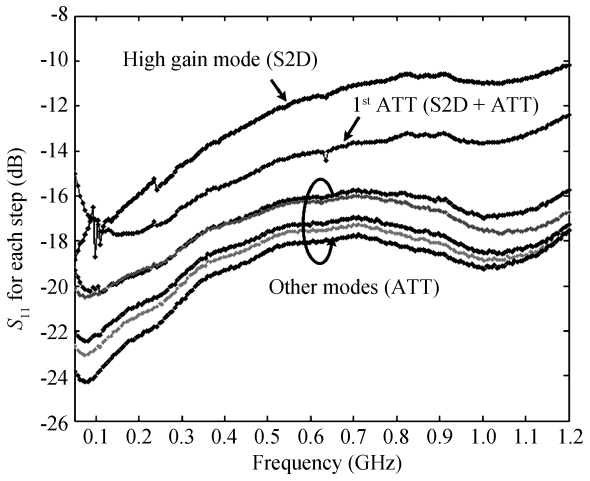

Fig. 12. The measured S_{11} for each gain step.

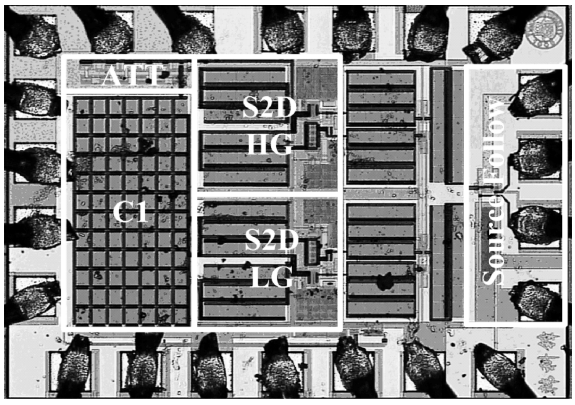

Fig. 11. Die photo of VGLNA for a TV tuner.

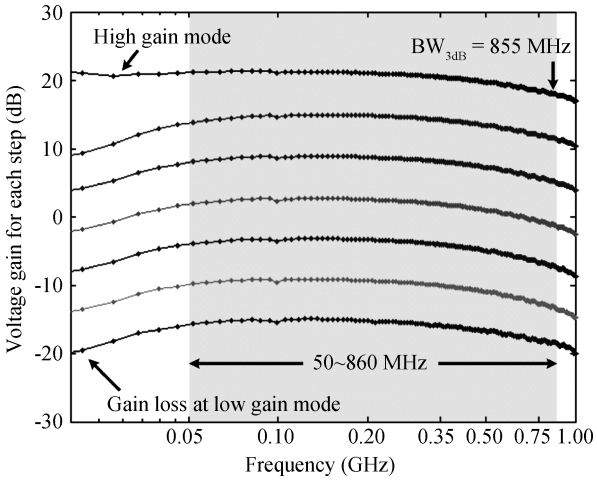

Fig. 13. The measured gain of VGLNA for each gain step.

The measured voltage gain at high gain mode is 21.3 dB with a 3 dB bandwidth of 855 MHz. The gains at attenuation mode drop to low frequency due to a high pass pole by C_1 and Z_{in} in Fig. 7(c), thus C_1 should be chosen as large as possible.

IIP3 and IIP2 are measured by two-tone methods. IIP3 is measured to be 0.9 dBm and IIP2 is 26.3 dBm at high gain mode, and the frequencies for the tones are given in Fig. 14.

NF at high gain mode is also measured, as shown in Fig. 15. The NF is in accordance with the post-layout simulation, especially for the low frequency band, and the measured NF increases with frequency because of gain drops.

Figure 16 shows the measured performance versus gain steps. The maximum gain error is less than 0.4 dB at 450 MHz and NF increases from 3.0 to 39.0 dB for attenuation. IIP3 is 0.9 dBm at high gain mode and it achieves a value of 23.5 dBm for maximum attenuation. It is also limited by the input switches in front of the R–$2R$ ladder. The reason is also applicable for IIP2 with the peak value of 50.0 dBm for maximum attenuation.

Table 1 summarized the measurements of this proposed VGLNA and comparisons are also made between similar

Table 1. Performance summary and comparisons.

	JSSC'08[7]	ASSCC'08[9]	JSSC'07[14]	ISSCC'09[16]	CICC'05[18]	This work
CMOS process	65 nm	0.18 μm	0.18 μm	0.13 μm	130 nm	0.18 μm
Power supply (V)	1.2 V	1.8	1.8	1.2	1.8	1.8
Bandwidth (GHz)	0.2–5.2	0.05–0.86	0.47–0.87	0.2–1	0.8–6	0.01–0.855
NF (dB) @ Max gain	< 3.5	4.2	4.3	2.5	2.9–4.2	3.0–4.5
Voltage gain (dB)	15.6	15	16	> 20	18–20	–15.1 to 21.3
Gain range (dB)	—	31	33	—	—	36.4
IIP3 (dBm)	> 0	2.6	–1.5	2.5	1	0.9–23.5
IIP2 (dBm)	> 20	8.6	—	> 28	4	26.3–50.0
S_{11} (dB)	< –10	< –10	–11	< –10	< –10	< –10.4
Power (mA)	11.67	5.56	12.2	6.5	6.5	< 10
Size (mm^2)	0.009*	0.29	0.32	—	—	0.06*

* Core area.

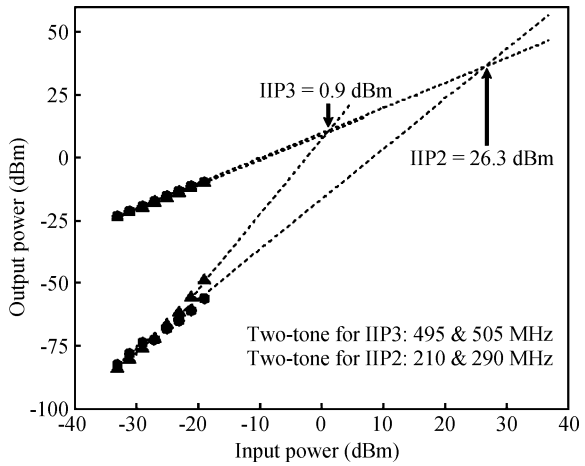

Fig. 14. The measured IIP3 and IIP2 performance at high gain mode.

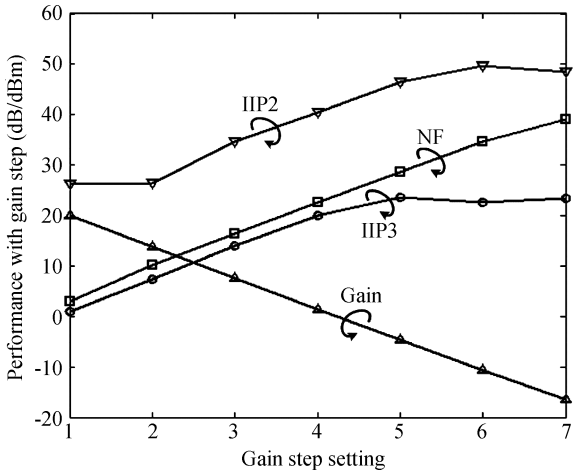

Fig. 16. Performance of this VGLNA with gain steps.

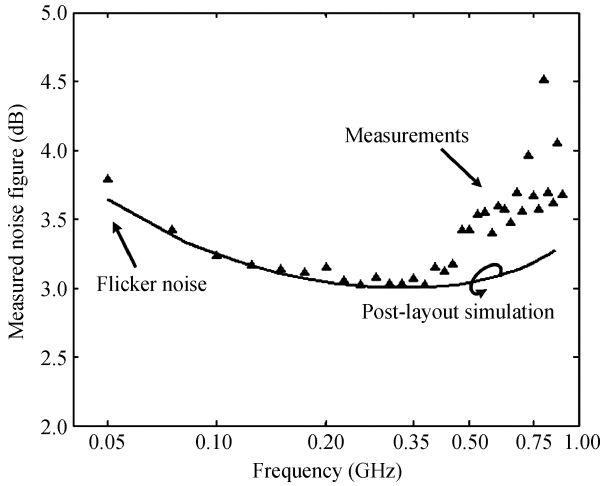

Fig. 15. The measured NF for VGLNA at high gain mode.

works.

5. Conclusion

In this paper, a wideband RF VGLNA has been presented. This VGLNA employs a S2D stage for single-to-differential conversion with low noise and high linearity. The paper gives a detailed noise analysis for S2D. Comparison has also been made for accurate linearity calculations and it can be learnt that the transconductance still dominates the non-linearity in S2D. For the adaptation of high signal level, a resistive attenuator is presented with a 6 dB gain step and constant input matching. A RF switch has also been proposed to improve the linearity and reduce the parasitic capacitance. Measurements show that this VGLNA achieves a minimum NF of 3.0 dB with a voltage gain of 21.3 dB, the IIP3 is 0.9 dBm and IIP2 is 26.3 dBm at high gain mode. With the attenuation, the value IIP3 reaches 23.5 dBm and IIP2 is close to 50 dBm. The total area for this VGLNA is 0.54 mm^2 (0.06 mm^2 for S2D) and the power consumption is less than 10 mA from a 1.8 V supply.

References

[1] Bruccoleri F, Klumperink E A M, Nauta B. Wide-band CMOS low-noise amplifier exploiting thermal noise canceling. IEEE J Solid-State Circuits, 2004, 39(2): 275

[2] Lerstaveesin S, Gupta M, Kang D, et al. A 48–860 MHz CMOS low-IF direct-conversion DTV tuner. IEEE J Solid-State Circuits, 2008, 43(9): 2013

[3] Giannini V, Nuzzo1 P, Soens C, et al. A 2 mm^2 0.1–5 GHz software-defined radio receiver in 45 nm digital CMOS. IEEE ISSCC, 2009: 408

[4] Bruccoleri F. Wideband low noise amplifiers exploiting thermal noise cancellation. PhD Thesis, 2005

[5] Im D, Nam I, Kim H T, et al. A wideband CMOS low noise amplifier employing noise and IM2 distortion cancellation for a digital TV tuner. IEEE J Solid-State Circuits, 2009, 44(3): 686
[6] Gatta F, Gomez R, Shin Y J, et al. An embedded 65 nm CMOS baseband IQ 48 MHz–1 GHz dual tuner for DOCSIS 3.0. IEEE J Solid-State Circuits, 2009, 44(12): 3511
[7] Blaakmeer S C, Klumperink E A M, Leenaert D M W, et al. Wideband balun-LNA with simultaneous output balancing, noise canceling and distortion canceling. IEEE J Solid-State Circuits, 2008, 43(6): 1341
[8] Bagheri R, Mirzaei A, Chehrazi S, et al. An 800-MHz–6-GHz software-defined wireless receiver in 90-nm CMOS. IEEE J Solid-State Circuits, 2006, 41(12): 2860
[9] Han K, Zou L, Liao Y, et al. A wideband CMOS variable gain low noise amplifier based on single-to-differential stage for TV tuner applications. IEEE Asia Solid-state Circuit Conference, 2008: 457
[10] Enrique F. Single input to differential output amplifier. US Patent, No. 4885550, 1988
[11] Razavi B. Design of analog CMOS integrated circuits, US: McGrawHill, 2001
[12] Mastantuono D, Manstretta D. A low-noise active balun with IM2 cancellation for multi-band portable DVB-H receivers. IEEE ISSCC, 2009: 216
[13] Kang S, Choi B, Kim B. Linearity analysis of CMOS for RF application. IEEE Trans Microw Theory Tech, 2003, 51(3): 972
[14] Xiao J, Mehr I, Silva-Martinez J, et al. A high dynamic range CMOS variable gain amplifier for mobile DTV tuner. IEEE J Solid-State Circuits, 2007, 42(2): 292
[15] Manstretta D, Dauphinee L. A highly linear broadband variable gain LNA for TV applications. IEEE CICC, 2007: 531
[16] Huang Y T, Yang C M, Huang S C, et al. A 1.2 V 67 mW 4 mm^2 mobile ISDB-T tuner in 0.13 μm CMOS. IEEE ISSCC, 2009: 124
[17] Dogan H, Meyer R G, Niknejad A M. Analysis and design of RF CMOS attenuators. IEEE J Solid-State Circuits, 2008, 43(10): 2269
[18] Chehrazi S, Mirzaei A, Bagheri R, et al. A 6.5 GHz wideband CMOS low noise amplifier for multi-band use. IEEE CICC, 2005: 801