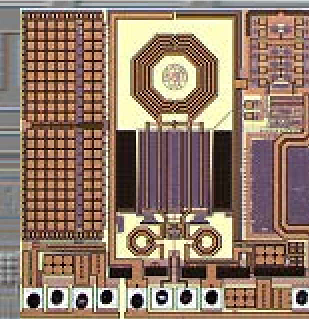


模拟集成电路设计原理

(Principle of Analog Integrated Circuit Design, INF0130025.02)

2014年11月13日

唐长文 教授

zwtang@fudan.edu.cn

http://rfic.fudan.edu.cn/Courses.htm

复旦大学/微电子学院/射频集成电路设计研究小组

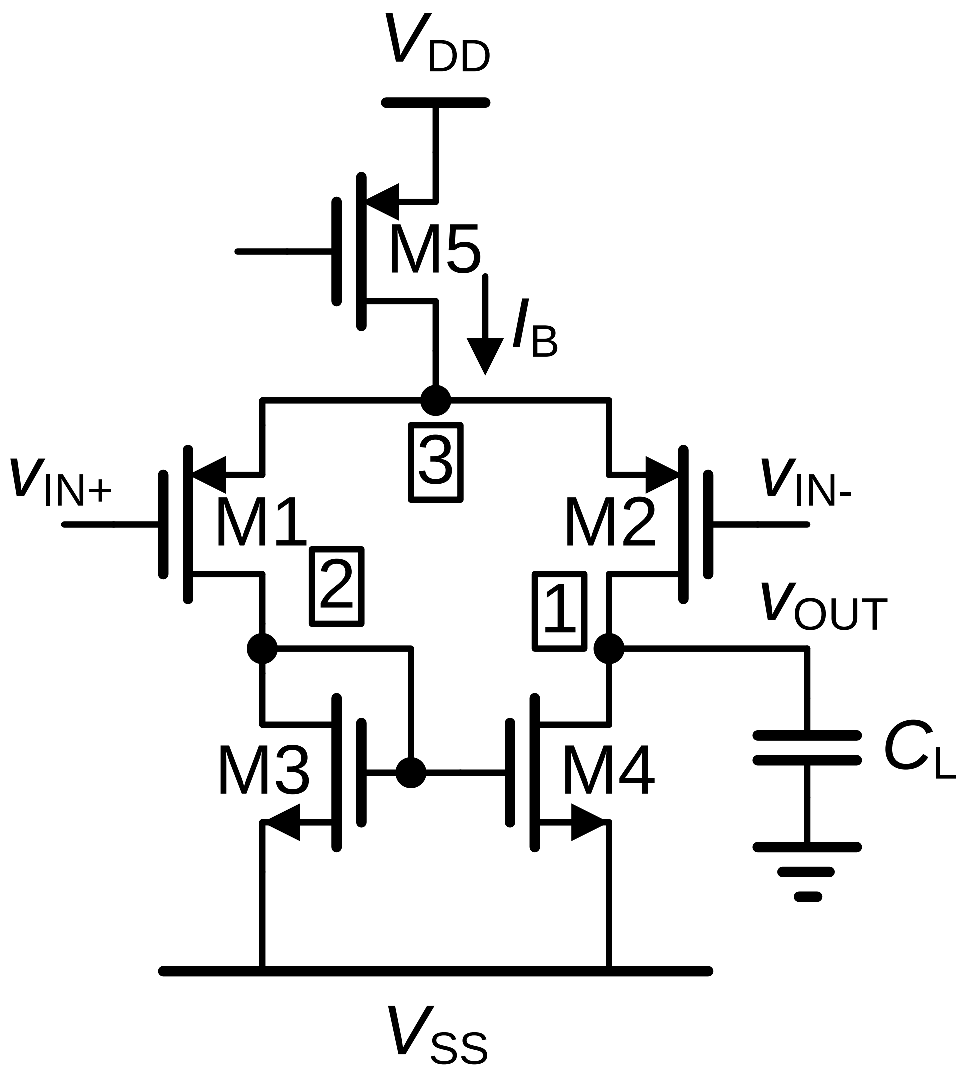
运算放大器的系统设计

目录

- 单级OTA的设计
- CMOS密勒OTA的设计
- *GBW*和相位裕度的设计
- 其他指标：输入范围、输出范围、*SR*…

Ref.: W. Sansen : Analog Design Essentials, Springer 2006

CMOS单级OTA：GBW



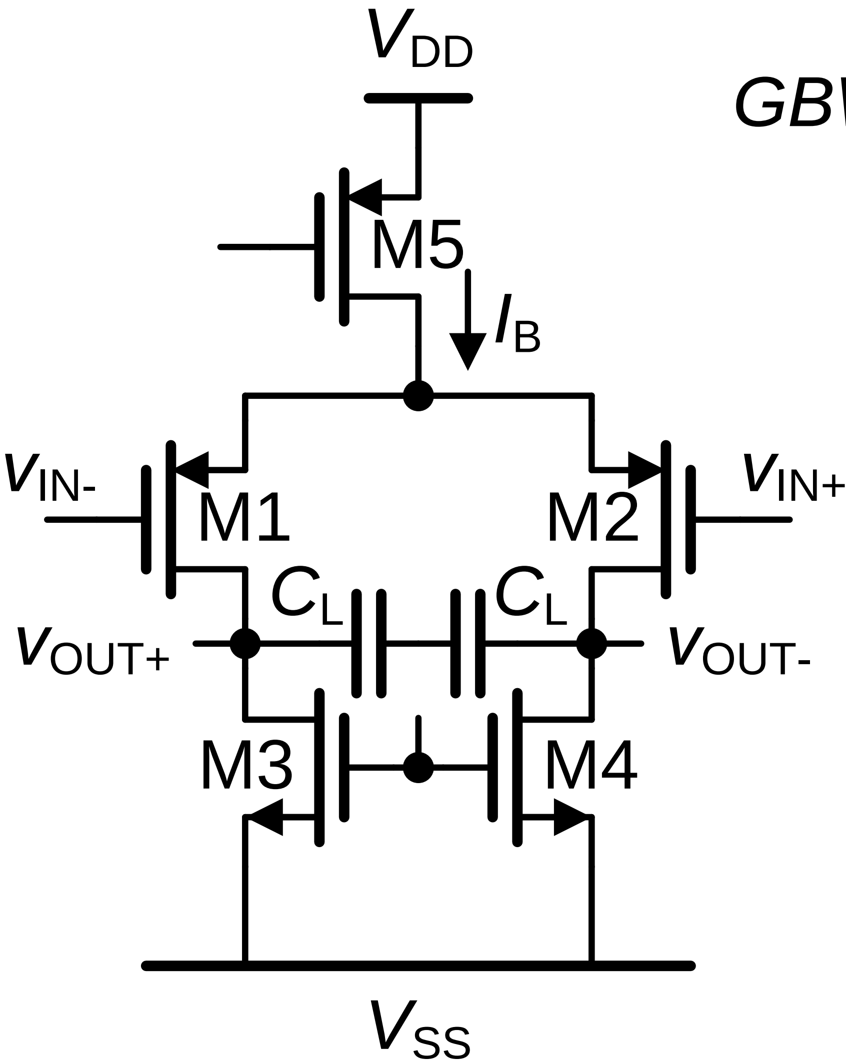
$$A_V = g_{m1}\frac{r_{DS}}{2}$$

如果：$r_{DS2} = r_{DS4} = r_{DS}$

$$BW = \frac{1}{2\pi\frac{r_{DS}}{2}(C_L + C_{n1})}$$

$$GBW = \frac{g_{m1}}{2\pi(C_L + C_{n1})}$$

CMOS OTA：最大GBW



$$GBW = \frac{g_{m1}}{2\pi C_L} \qquad g_{m1} = \frac{I_B}{V_{GS1} - V_T}$$

$$GBW_{max} = \frac{I_B}{V_{GS1} - V_T}\frac{1}{2\pi C_L}$$

$C_L = 1\ \text{pF}$

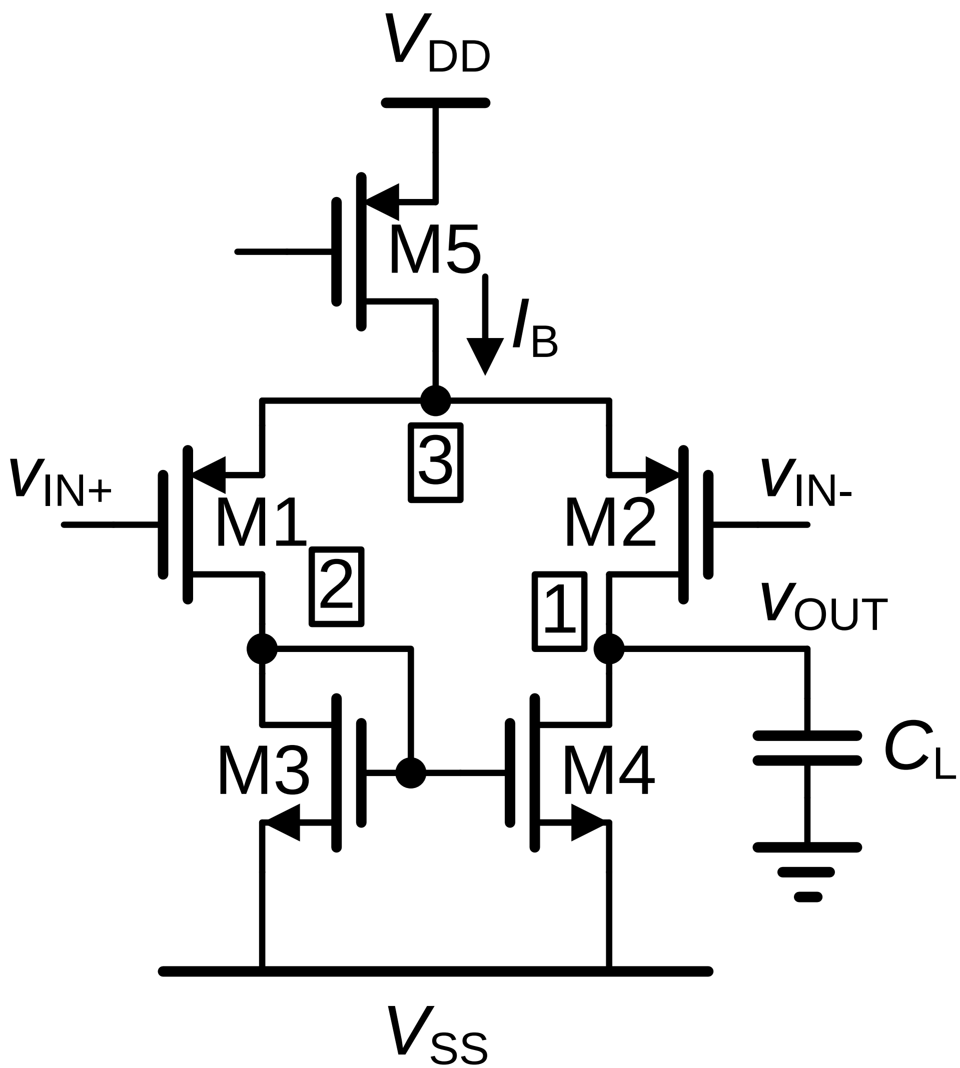
$I_B = 10\ \mu\text{A}$

$\Rightarrow GBW_{max} \approx 10\ \text{MHz}$ [8]

$$FOM = \frac{GBW \bullet C_L}{I_B}$$

$= 1000\ \text{MHzpF/mA}$ [800]

CMOS单级OTA：f_{nd}



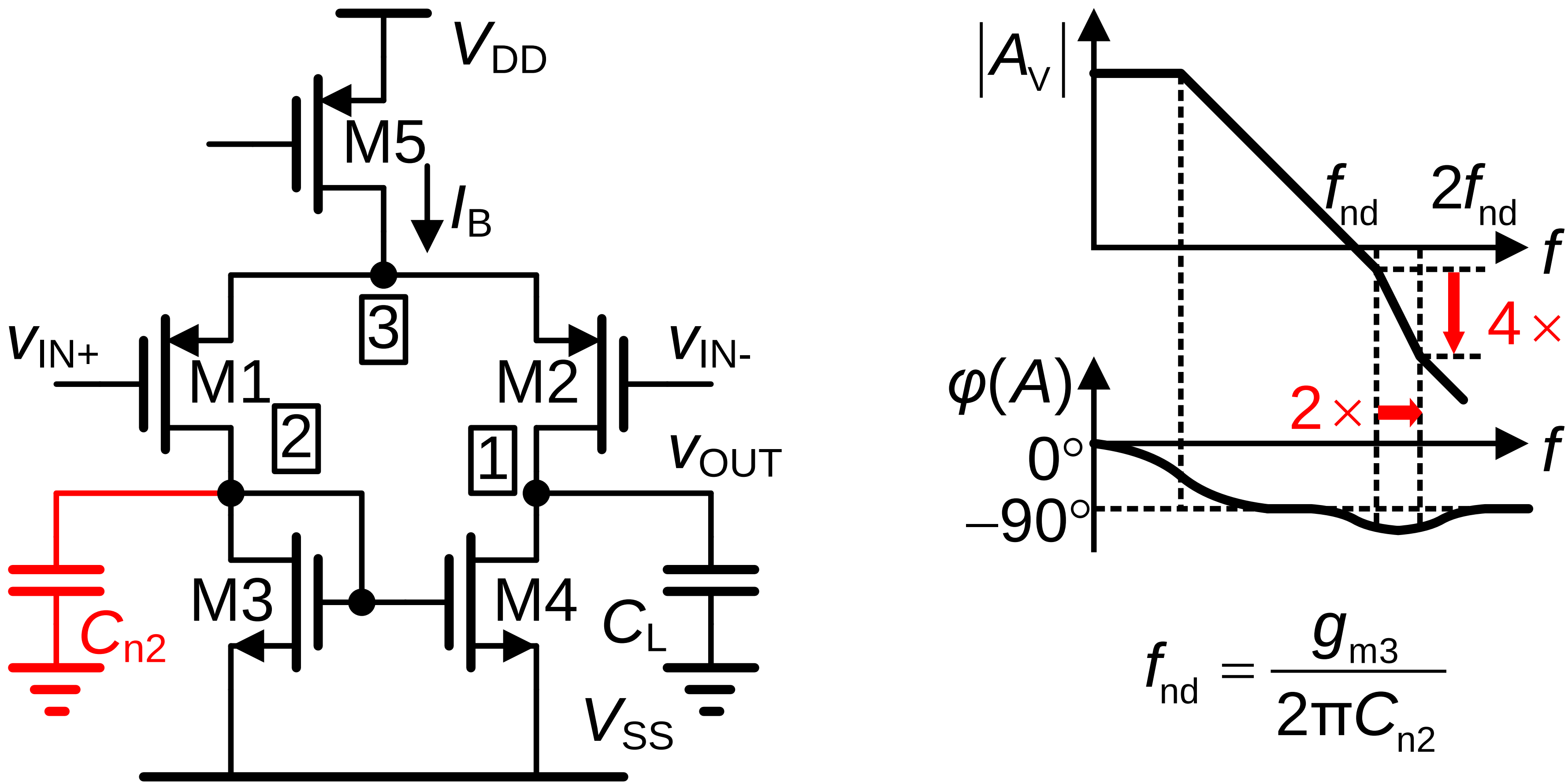
$$GBW = \frac{g_{m1}}{2\pi(C_L + C_{n1})}$$

$$f_{nd} = \frac{g_{m3}}{2\pi C_{n2}}$$

$$C_{n2} \approx 2C_{GS3} + C_{DB3} + C_{DB1}$$
$$\approx 4C_{GS3}$$

$$f_{nd} \approx \frac{f_{T3}}{4}$$

CMOS OTA: f_{nd}



$$f_{nd} = \frac{g_{m3}}{2\pi C_{n2}}$$

$$PM = 90° - \arctan\left(\frac{GBW}{f_{nd}}\right) + \arctan\left(\frac{GBW}{2f_{nd}}\right) \approx 85°$$

CMOS单级OTA：设计 1

已知: $GBW = 100\ \text{MHz}$ 和 $C_L = 2\ \text{pF}$

工艺: $L_{min} = 0.35\ \mu\text{m}$、$K_n' = 60\ \mu\text{A/V}^2$ 和 $K_p' = 30\ \mu\text{A/V}^2$

求: I_{DS}、W、L

$$g_m = 2\pi C_L GBW = 1.2\ \text{mS} \qquad V_{GS} - V_T = 0.2\ \text{V}$$

$$I_{DS} = g_m \frac{V_{GS} - V_T}{2} = \frac{g_m}{10} = 0.12\ \text{mA}$$

$$\frac{W}{L} = \frac{I_{DS}}{K'(V_{GS} - V_T)^2} = 100 \qquad L_p = L_n = 1\ \mu\text{m}\ \text{考虑增益！}$$

$$W_n = 50\ \mu\text{m}、W_p = 100\ \mu\text{m}$$

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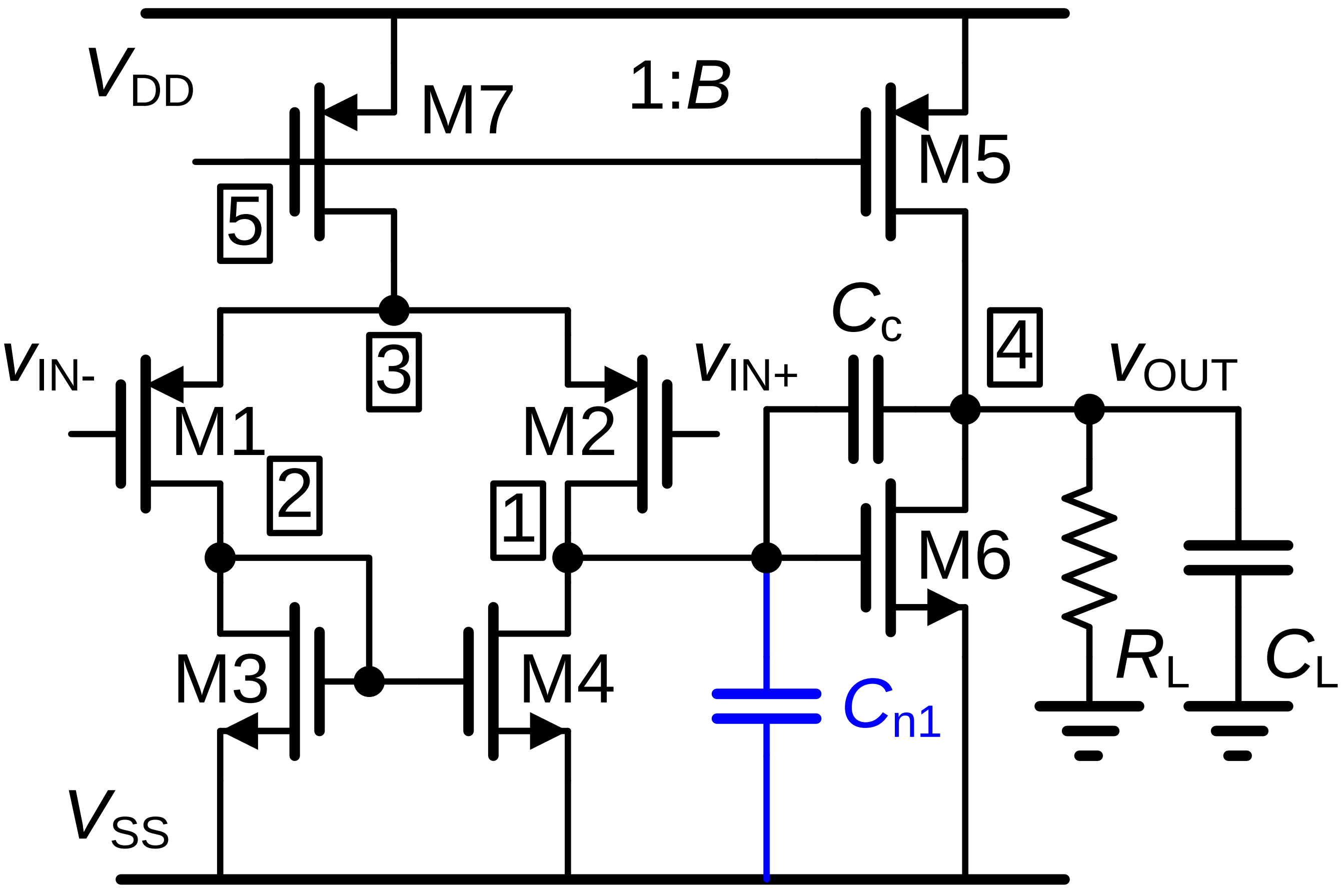
CMOS密勒OTA



两个节点

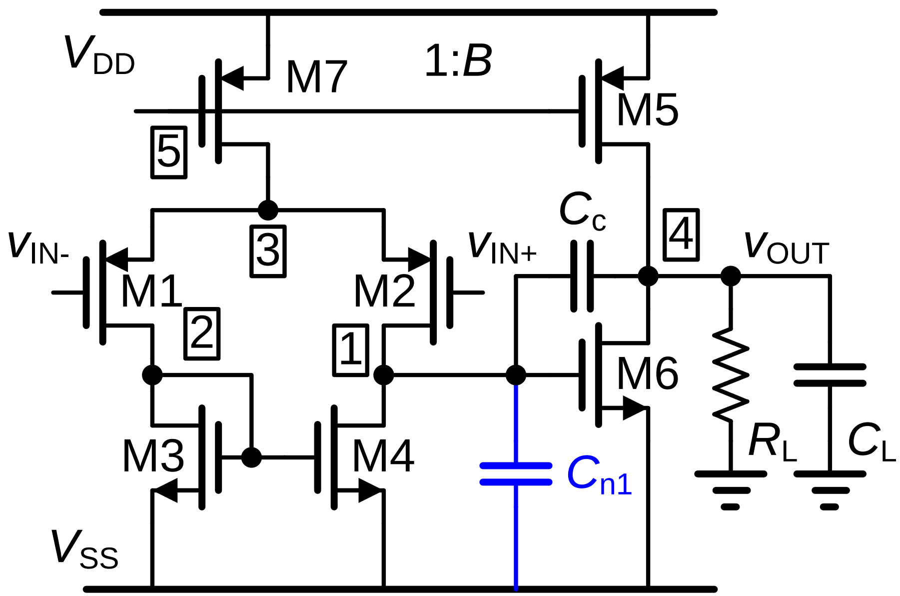
1 4

具有高阻抗

产生两个极点

用C_c进行分离

CMOS密勒OTA：小信号



$GBW = 1\ \text{MHz}$

$C_L = 10\ \text{pF}$

$R_L = 10\ \text{k}\Omega$

$g_{m1} = 7.5\ \mu\text{S}$

$g_{o24} = 0.03\ \mu\text{S}$

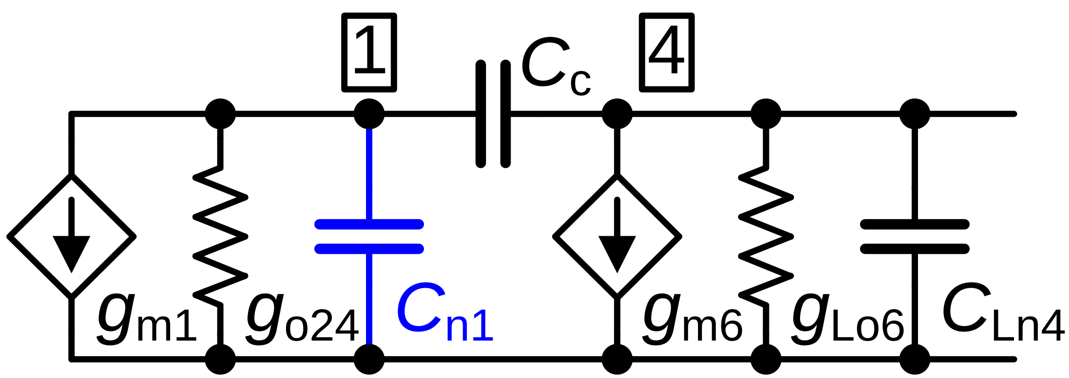
$C_{n1} = 0.37\ \text{pF}$

$C_c = 1\ \text{pF}$

$g_{m6} = 246\ \mu\text{S}$

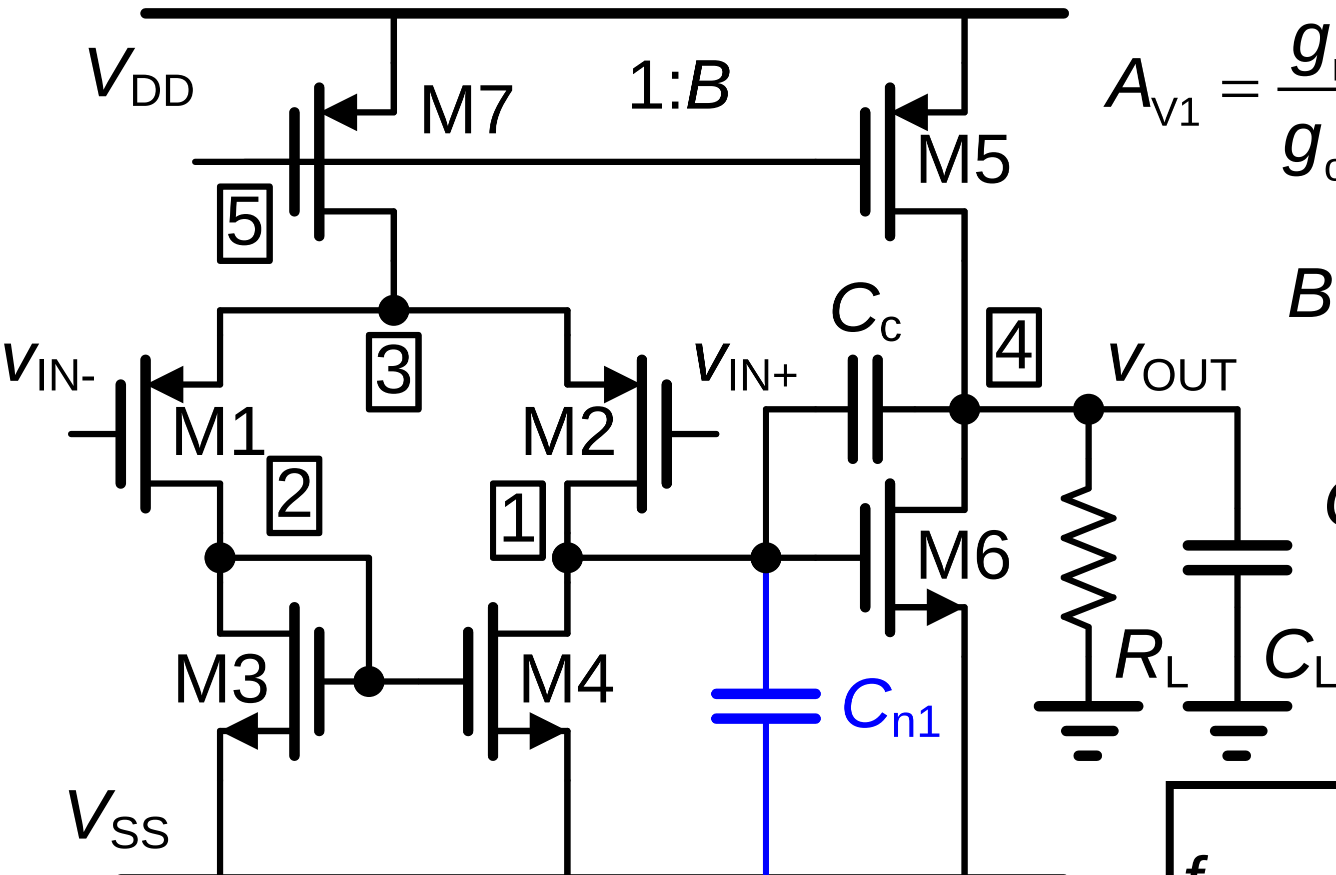
$g_{Lo6} = 20\ \mu\text{S}$

$C_{Ln4} = 10.2\ \text{pF}$



$I_{DS1} = 1.1\ \mu\text{A}$ $I_{DS6} = 25\ \mu\text{A}$

CMOS密勒OTA：GBW



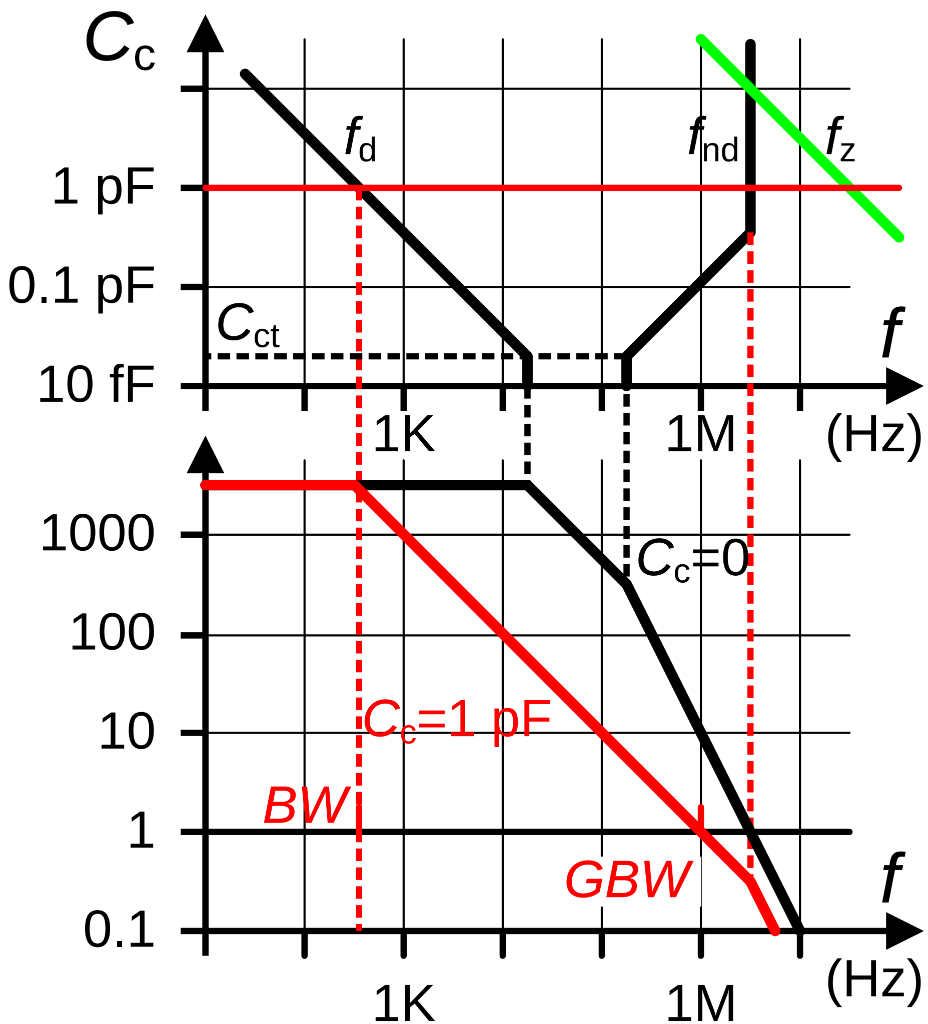
$$A_{V1} = \frac{g_{m1}}{g_{o24}} \quad A_{V2} = \frac{g_{m6}}{g_{Lo6}}$$

$$BW = \frac{g_{o24}}{2\pi A_{V2} C_c}$$

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} \approx \frac{g_{m6}}{2\pi C_{Ln4}} \frac{1}{1+\dfrac{C_{n1}}{C_c}}$$

CMOS密勒OTA：极点和零点



极点分离

从 $C_c \approx \frac{C_{n1}}{A_{V2}} \approx 20\ \text{fF}$ 开始

$C_c = 1\,\text{pF}$足够

$$f_z = \frac{g_{m6}}{2\pi C_c}$$

目录

CMOS密勒OTA：设计规划

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} \approx \frac{g_{m6}}{2\pi C_{Ln4}} \frac{1}{1+\frac{C_{n1}}{C_c}}$$

$GBW = 100\ \text{MHz}$ $C_L = 2\ \text{pF}$

两个方程，

三个变量g_{m1}、g_{m6}、C_c？

求解：选择g_{m1}或g_{m6}或C_c？

选择 C_c=1 pF 有问题吗?

CMOS密勒OTA设计：参变量C_c 1

选择$C_c \approx 3C_{n1}$得$GBW = \dfrac{g_{m1}}{2\pi C_c}$和$3GBW \approx \dfrac{g_{m6}}{2\pi C_{Ln4}} \dfrac{1}{1.3}$

$$\frac{g_{m6}}{g_{m1}} \approx 4\frac{C_L}{C_c}$$

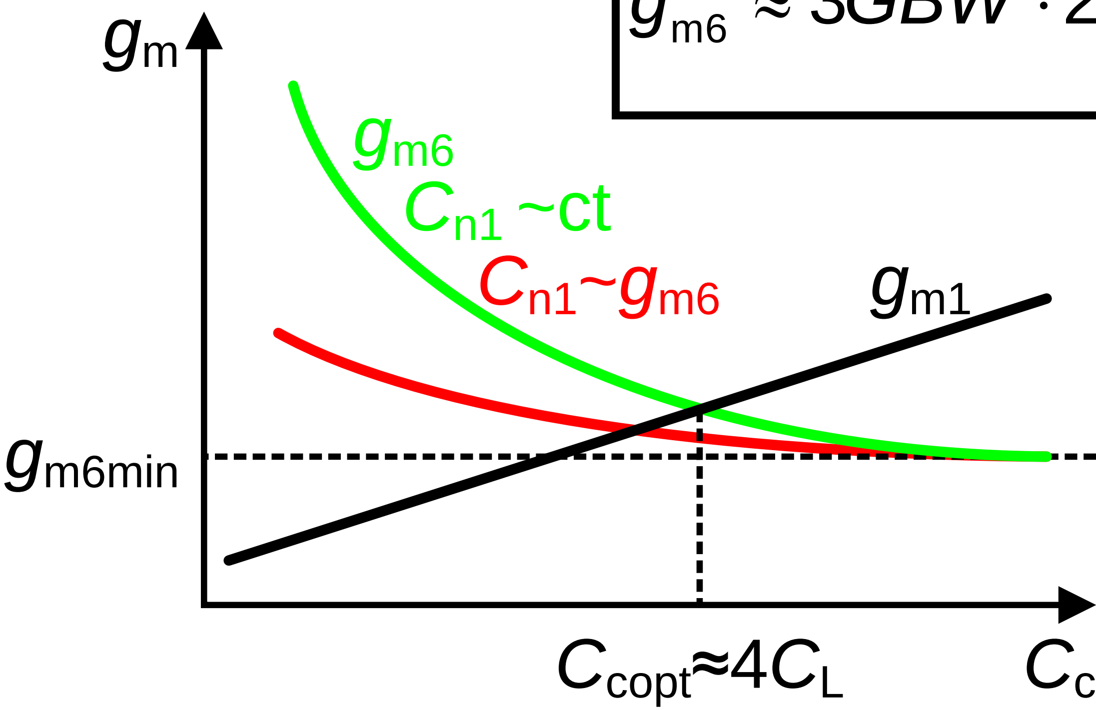
$GBW = 100\ \text{MHz} \quad C_L = 2\ \text{pF}$

选择 $C_{n1} < C_c < C_L$

选择 $C_c = 1\,\text{pF}$ 得 $g_{m1} = 0.63\ \text{mS}$ 和 $g_{m6} = 5.0\ \text{mS}$

CMOS密勒OTA设计：参变量C_c 2

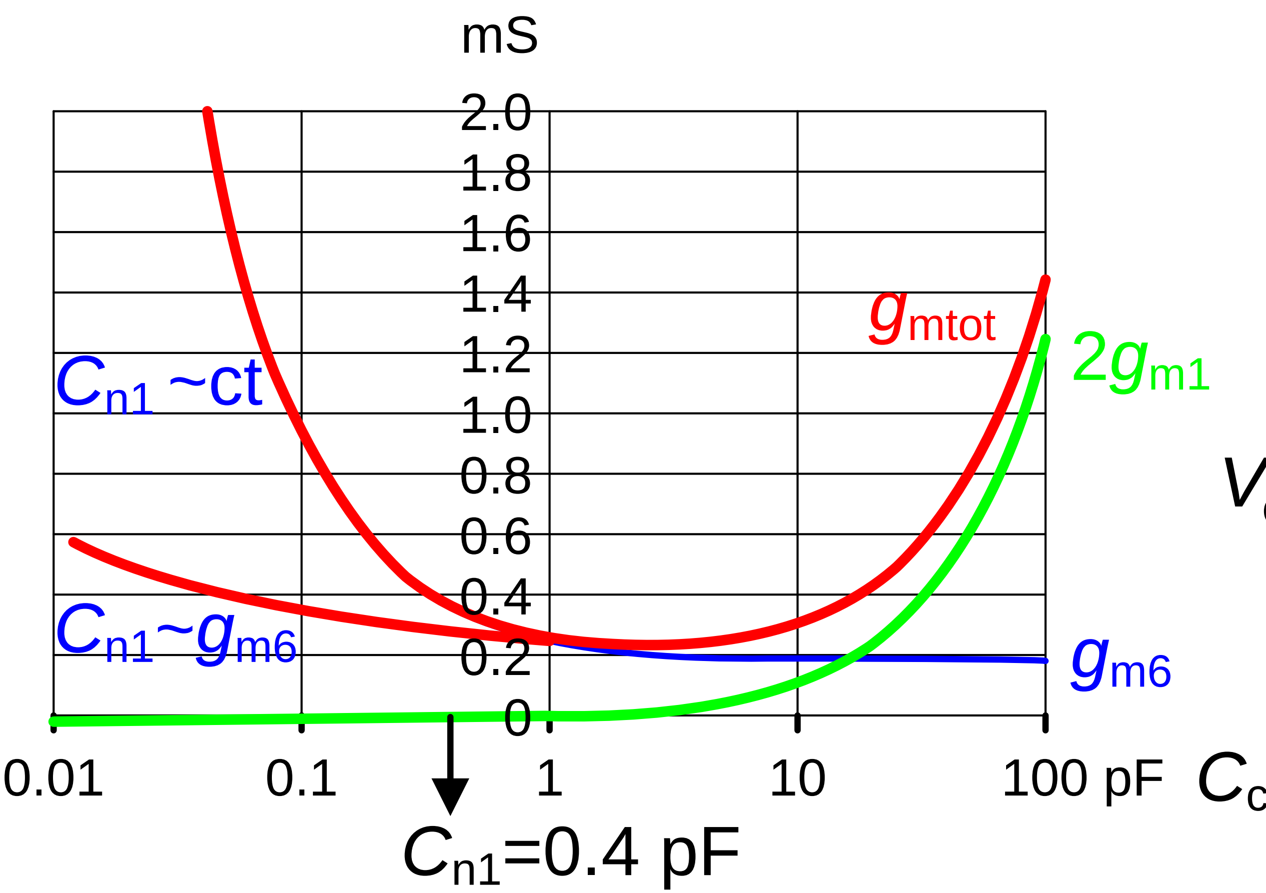
$$g_{m6} \approx 3GBW \cdot 2\pi C_{Ln4} \cdot (1 + \frac{C_{n1}}{C_c})$$



$$g_{m1} = 2\pi \cdot GBW \cdot C_C$$

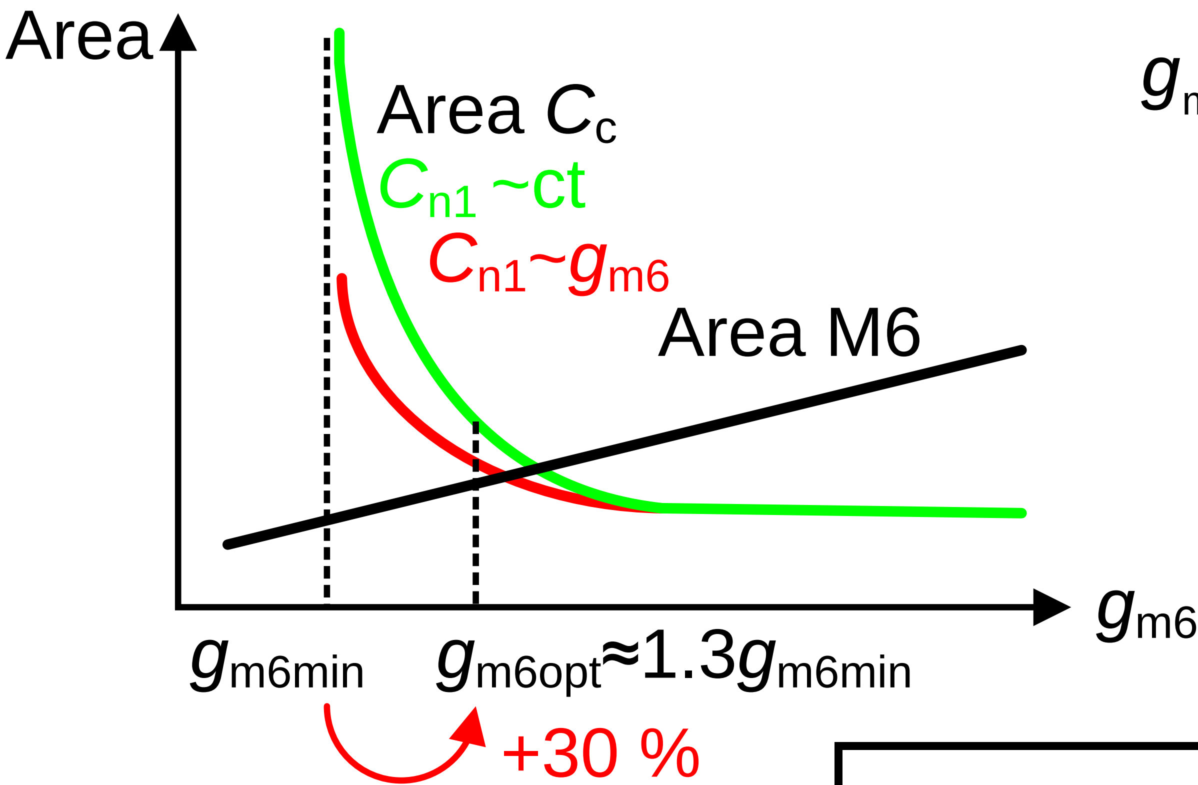
$$g_{m6min} = 3GBW(2\pi C_L)$$

1 MHz CMOS密勒OTA：参变量C_c



$$GBW = 1\ \text{MHz}$$
$$C_L = 10\ \text{pF}$$
$$C_{n1} = 0.4\ \text{pF}$$
$$K' = 20\ \mu\text{A/V}^2$$
$$V_{GS} - V_T = 0.2\ \text{V}$$
$$L = 10\ \mu\text{m}$$

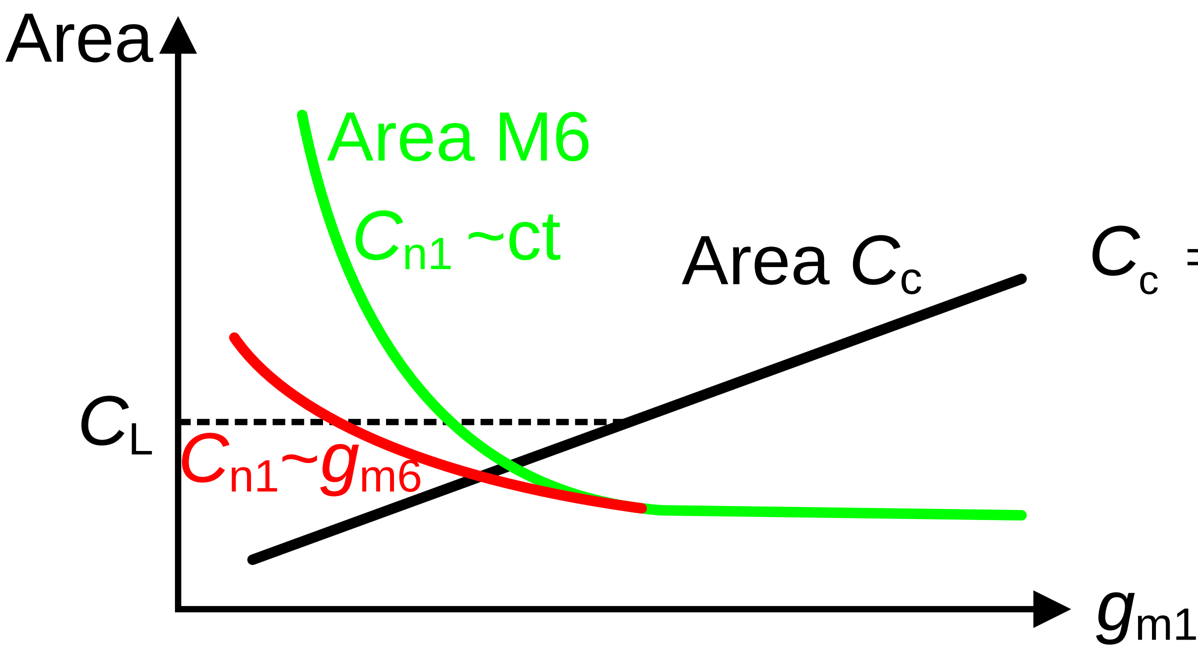
CMOS密勒OTA设计：参变量g_{m6}



$$g_{m6min} = 3GBW(2\pi C_L)$$

$$g_{m6} \approx 3GBW \cdot 2\pi C_{Ln4} \cdot \left(1+\frac{C_{n1}}{C_c}\right)$$

CMOS密勒OTA设计：参变量g_{m1}



$$C_c = \frac{g_{m1}}{2\pi GBW}$$

$$g_{m6} \approx 3GBW \cdot 2\pi C_{Ln4} \cdot (1 + \frac{C_{n1}}{g_{m1}} 2\pi GBW)$$

高速密勒OTA的优化设计 1

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$f_{nd} = \frac{g_{m6}}{2\pi C_L} \frac{1}{1 + C_{n1}/C_c}$$

$$C_L = \alpha C_c \qquad \alpha \approx 2$$

$$C_c = \beta C_{n1} = \beta C_{GS6} \qquad \beta \approx 3$$

$$f_{nd} = \gamma GBW \qquad \gamma \approx 2$$

$$C_{GS} = kW \qquad k = 2\ \text{fF}/\mu\text{m}$$

$$GBW = \frac{f_{nd}}{\gamma} = \frac{g_{m6}}{2\pi C_L} \frac{1}{\gamma(1 + 1/\beta)} = \frac{f_{T6}}{\alpha\beta\gamma(1 + 1/\beta)}$$

$$C_L = \alpha C_c = \alpha\beta C_{n1} = \alpha\beta C_{GS6} = \alpha\beta k W_6$$

如果C_L↑ 则W_6↑

高速密勒OTA的优化设计 2

代入f_{T6}得

$$f_{T6}=\frac{g_{m6}}{2\pi C_{GS6}}$$

$$f_{T6}=\frac{1}{L_{6\min}}\frac{13.5}{1+2.8L_{6\min}/V_{GST6}}$$

L的单位为μm
f_T的单位为GHz

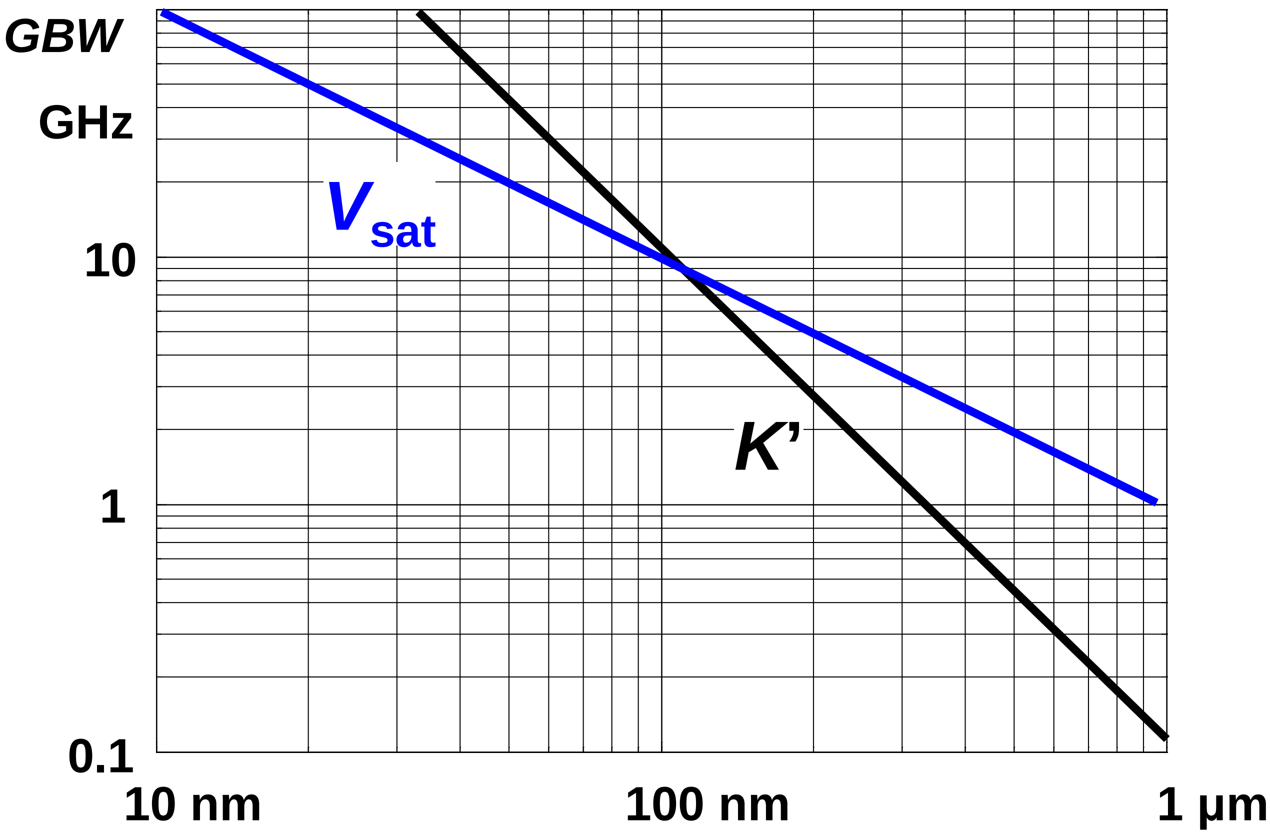
$$GBW=\frac{f_{T6}}{\alpha\beta\gamma(1+1/\beta)}$$

GBW不是由C_L决定，只由f_T决定！
f_T由L(和V_{GST})决定!!!

当V_{GST}=0.2 V，L_{min}<65 nm;

或V_{GST}=0.5 V，L_{min}<0.18 μm 时，晶体管进入速度饱和区

最大GBW与沟道长度L_{min}



$$V_{GS} - V_T = 0.2\ \text{V}$$

$$\alpha \approx 2$$

$$\beta \approx 3$$

$$\gamma \approx 2$$

$$16x$$

$$GBW \approx \frac{f_{T6}}{16}$$

高速密勒OTA的设计优化

- 选择$\alpha\ \beta\ \gamma$
- 由给定的GBW得到最小的f_{T6}
- 由选定的$(V_{GS6}-V_T)$

  选择最大沟道长度L_6(最大化增益)
- 由C_L计算W_6，

  确定I_{DS6}
- 由α以及C_L计算C_c
- 由C_c计算g_{m1}和I_{DS1}
- 由g_{m1}或C_c确定噪声

设计练习：*GBW* = 0.4 GHz & C_L = 5 pF

• 选择$\alpha\ \beta\ \gamma$	2 3 2
• 由给定的*GBW*得到最小的f_{T6}	$f_{T6} = 6.4$ GHz
• 由选定的$(V_{GS6}-V_T)$， 选择最大沟道长度L_6(最大化增益)	 $L_6 = 0.5$ μm
• L_6取最小沟道长度L_{min}	
• 由C_L计算W_6， 确定I_{DS6} ($K_n' = 70$ μA/V^2) 确定C_{n1} ($k = 2$ fF/μm)	$W_6 = 417$ μm $I_{DS6} = 2.3$ mA $C_{n1} = 0.83$ pF
• 由α以及C_L计算C_c	$C_c = 2.5$ pF
• 由C_c计算g_{m1}和I_{DS1}	$I_{DS1} = 0.63$ mA

低速密勒OTA的优化设计 1

$$GBW = \frac{f_{T6}}{\alpha\beta\gamma(1+1/\beta)}$$

$$\frac{f_T}{f_{TH}} = \sqrt{i}(1-e^{-\sqrt{i}}) \approx \sqrt{i}(1-1+\sqrt{i}) \approx i \quad \text{当}\, i\, \text{较小时}$$

$$f_{TH} = \frac{3}{2}\frac{2\mu kT/q}{2\pi L^2}$$

*GBW*不是由C_L决定，只由f_T决定！

f_T由*L*和*i* 决定!!!

低速密勒OTA的优化设计 2

- 选择$\alpha\beta\gamma$
- 由给定的GBW得到最小的f_{T6}
- 由给定的f_{TH6}
  选择最大沟道长度L_6(最大增益)
- 计算i_6
- 由C_L计算W_6，
  确定I_{DST6}和I_{DS6}
- 由α以及C_L计算C_c
- 由C_c计算g_{m1}和I_{DS1}
- 由g_{m1}或C_c确定噪声

设计练习：*GBW* = 1 MHz & C_L= 5 pF

- 选择$\alpha\ \beta\ \gamma$ ——— 2 3 2
- 由*GBW*=1 MHz得到最小的f_{T6} ——— $f_{T6} = 16\ \text{MHz}$
- 由给定的f_{TH6} ——— $f_{TH6} = 2\ \text{GHz}$

  选择最大沟道长度L_6(最大增益) ——— $L_6 = 0.5\ \mu\text{m}$
- 反型系数i ——— $i = 0.008$
- 由C_L计算W_6， ——— $W_6 = 417\ \mu\text{m}$

  确定I_{DST6}($K_n' = 70\ \mu\text{A/V}^2$) ——— $I_{DST6} = 0.33\ \text{mA}$

  确定I_{DS6} ——— $I_{DS6} = 2.7\ \mu\text{A}$

  确定C_{n1}($k = 2\ \text{fF}/\mu\text{m}$) ——— $C_{n1} = 0.83\ \text{pF}$
- 由α以及C_L计算C_c ——— $C_c = 2.5\ \text{pF}$
- 由C_c计算g_{m1}和I_{DS1} ——— $I_{DS1} = 1.6\ \mu\text{A}$

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CMOS密勒OTA：规范 1

1. Introductory analysis

1.1 DC currents and voltages on all nodes

1.2 Small-signal parameters of all transistors

2. DC analysis

2.1 Common-mode input voltage range vs supply Voltage

2.2 Output voltage range vs supply Voltage

2.3 Maximum output current (sink and source)

CMOS密勒OTA：规范 2

3. AC and transient analysis

3.1 AC resistance and capacitance on all nodes

3.2 Gain versus frequency : *GBW*, …

3.3 Gainbandwidth versus biasing current

3.4 Slew rate versus load capacitance

3.5 Output voltage range versus frequency

3.6 Settling time

3.7 Input impedance vs frequency (open & closed loop)

3.8 Output impedance vs frequency (open & closed loop)

CMOS密勒OTA：规范 3

4. Specifications related to offset and noise

4.1 Offset voltage versus common-mode input Voltage

4.2 *CMRR* versus frequency

4.3 Input bias current and offset

4.4 Equivalent input noise voltage versus frequency

4.5 Equivalent input noise current versus frequency

4.6 Noise optimization for capacitive/inductive sources

4.7 *PSRR* versus frequency

4.8 Distortion

CMOS密勒OTA：规范 4

5. Other second-order effects

5.1 Stability for inductive loads

5.2 Switching the biasing transistors

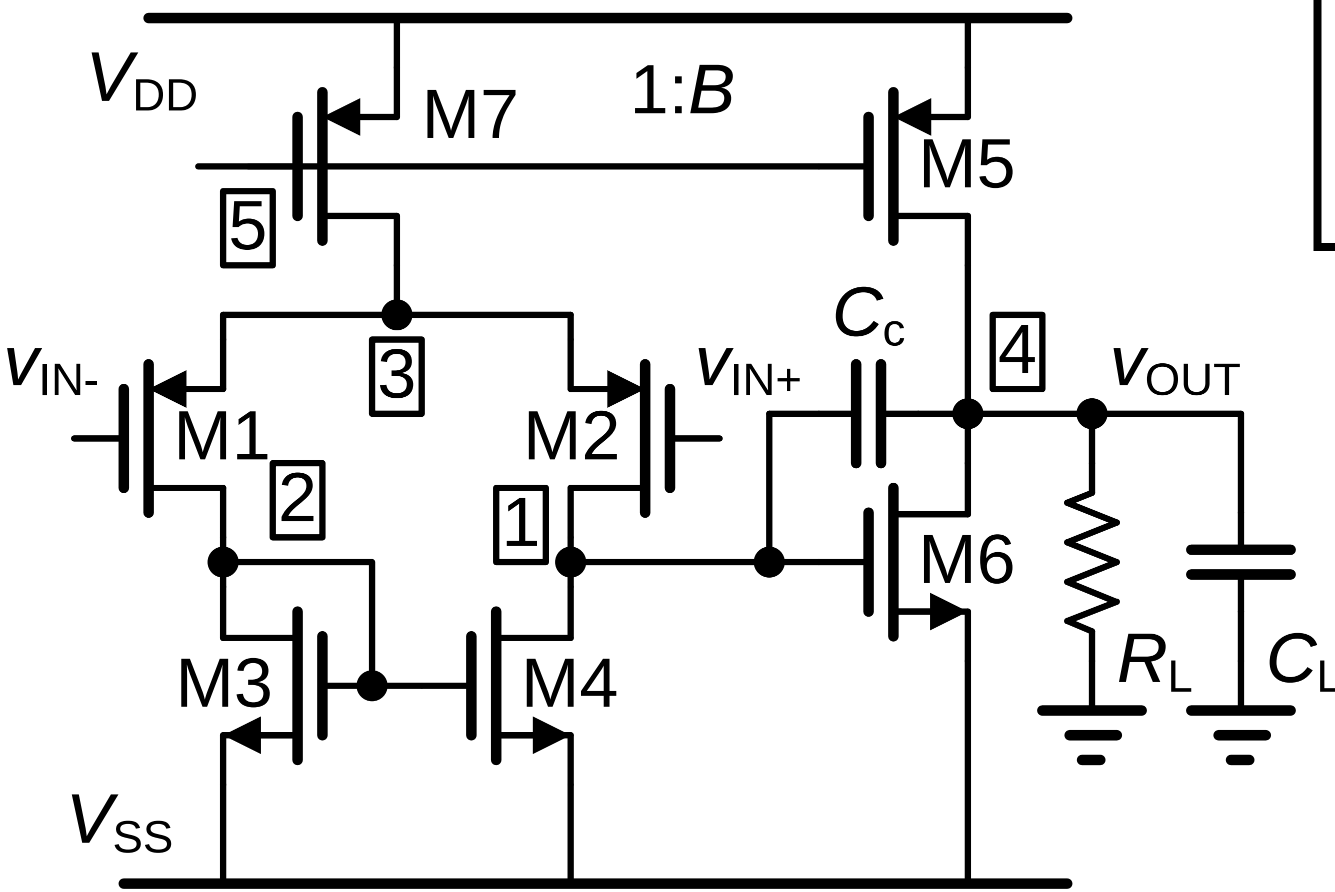
5.3 Switching or ramping the supply voltages

5.4 Different supply voltages, temperatures, ...

MCO：其他规范

- Common-mode input voltage range
- Output voltage range
- Slew Rate
- Output impedance
- Noise

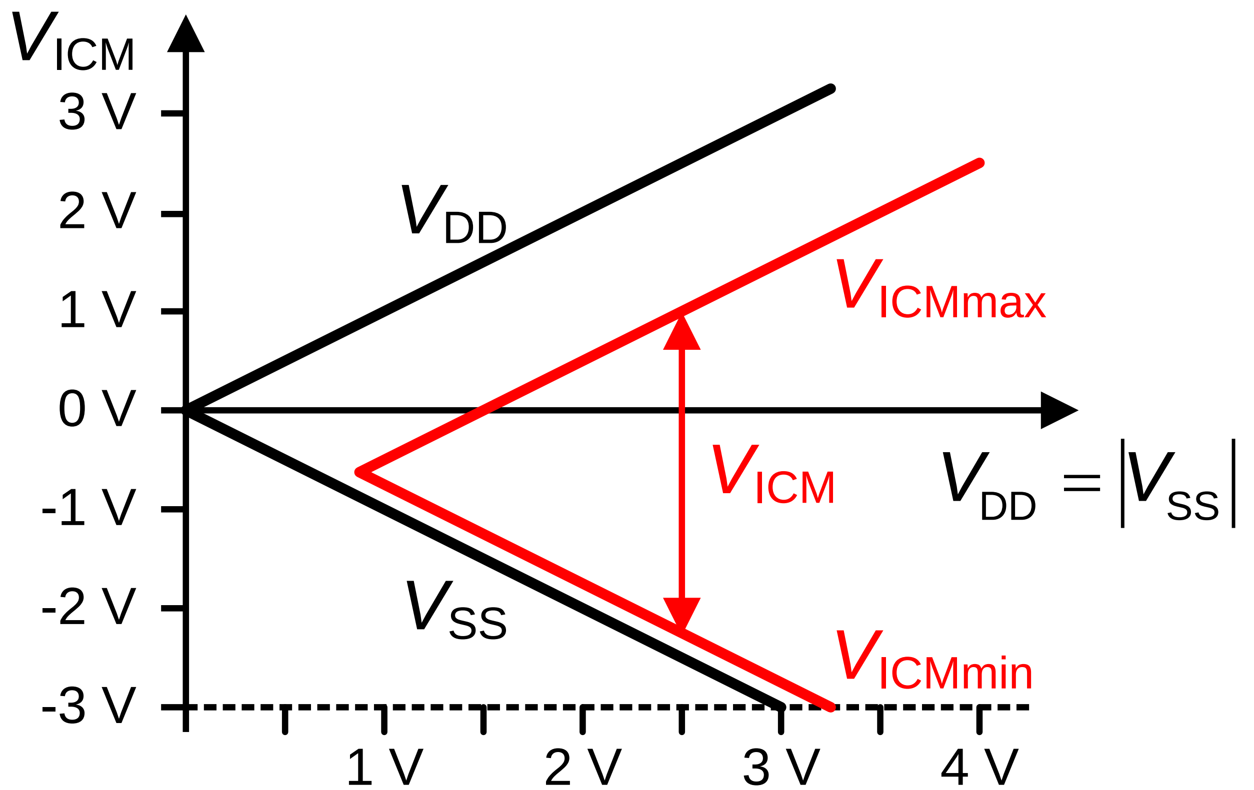
CMOS密勒OTA



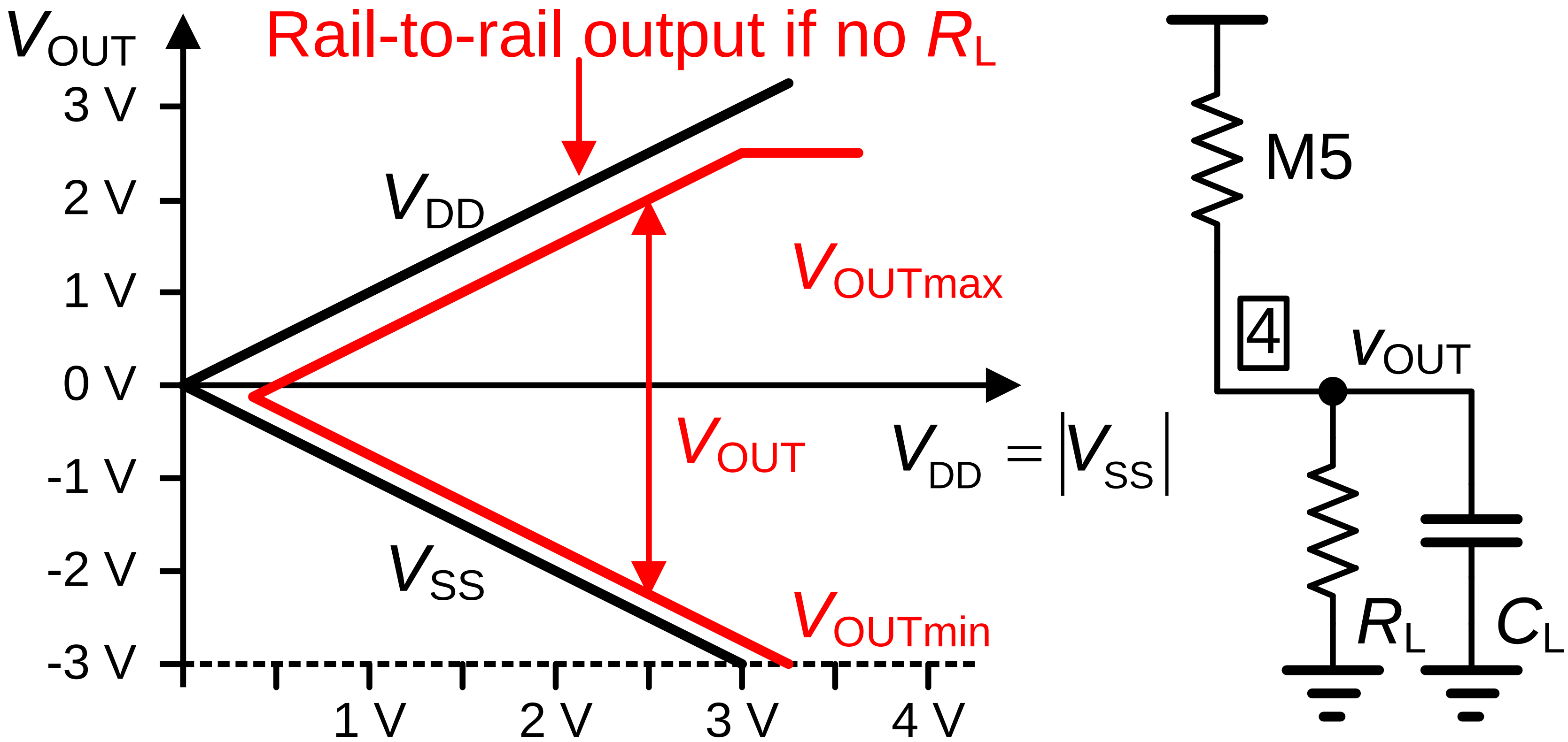
$$GBW = 1\ \text{MHz}$$
$$C_L = 10\ \text{pF}$$
$$R_L = 10\ \text{k}\Omega$$

$$g_{m1} = 7.5\ \mu\text{S}$$
$$I_{DS1} = 1.1\ \mu\text{A}$$
$$g_{o24} = 0.03\ \mu\text{S}$$
$$g_{m6} = 246\ \mu\text{S}$$
$$I_{DS6} = 25\ \mu\text{A}$$
$$C_c = 1\ \text{pF}$$
$$g_{Lo6} = 20\ \mu\text{S}$$

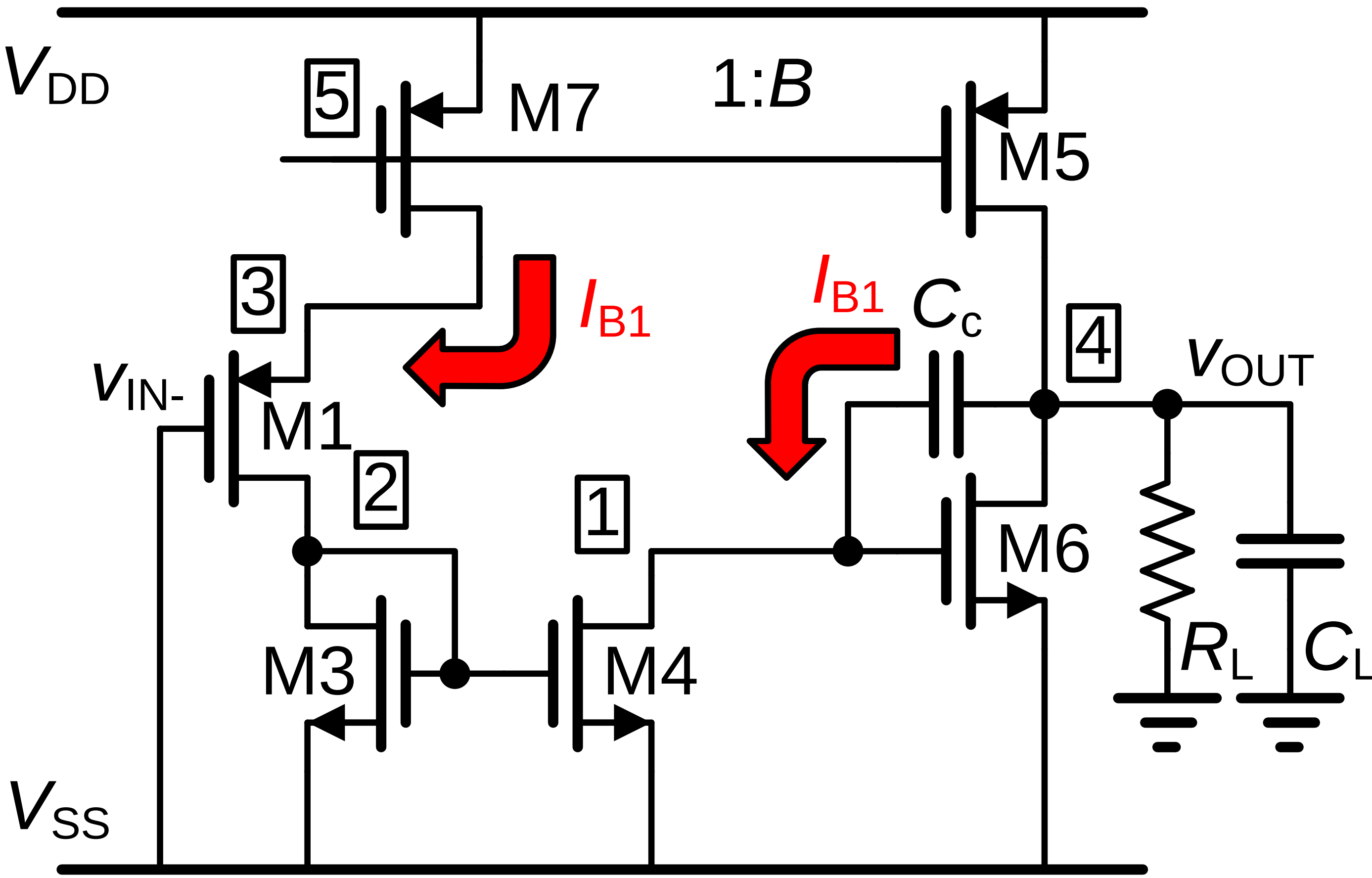
CMOS密勒OTA：共模输入电压范围



CMOS密勒OTA：输出电压范围



CMOS密勒OTA：压摆率 1



开关输入：

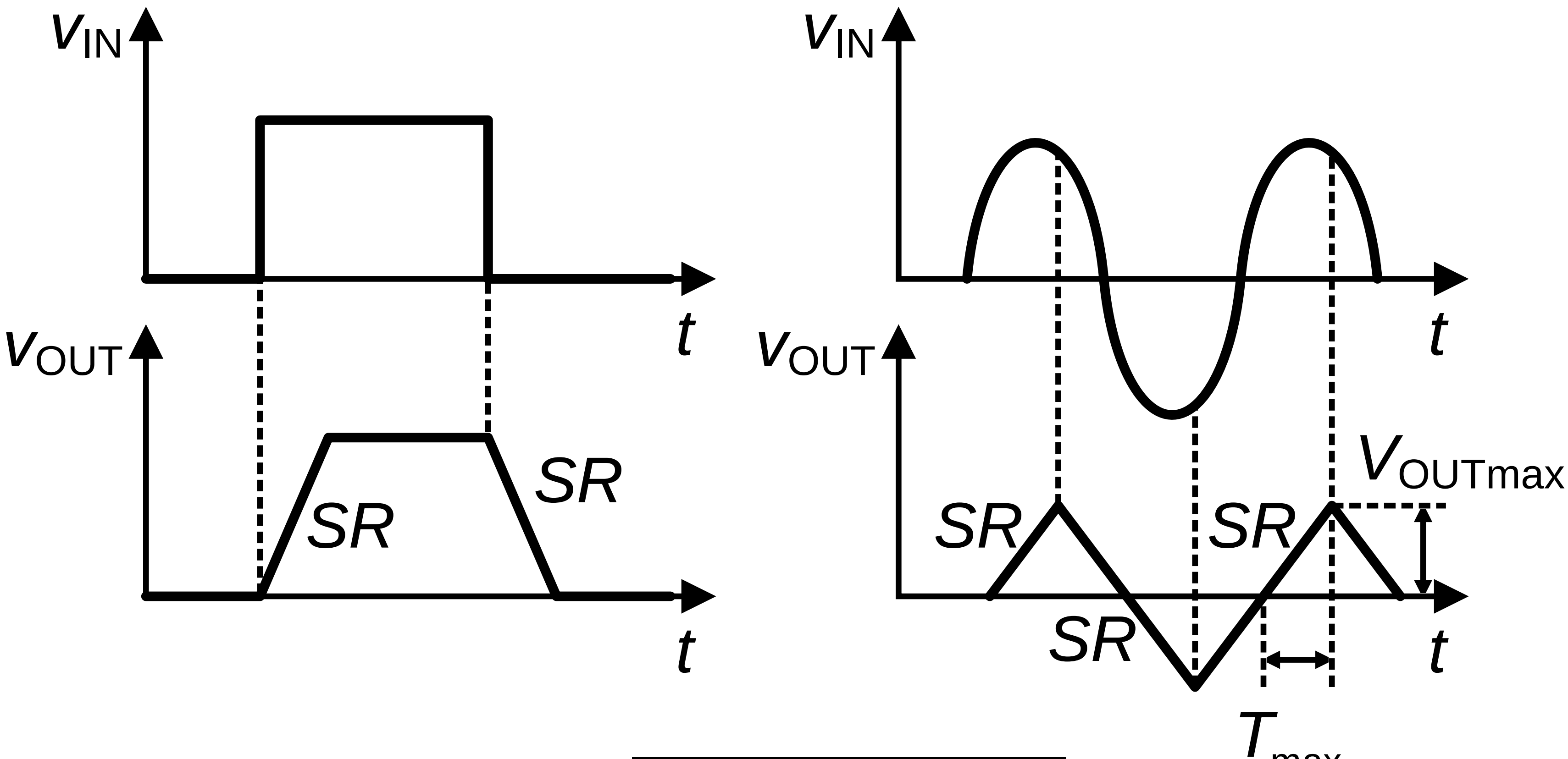
$v_{IN+} > 1$

$v_{IN\_} > 0$

$$SR = \frac{\Delta V_{OUT}}{\Delta t}$$

$$SR = \frac{I_{B1}}{C_C}$$

CMOS密勒OTA：压摆率 2

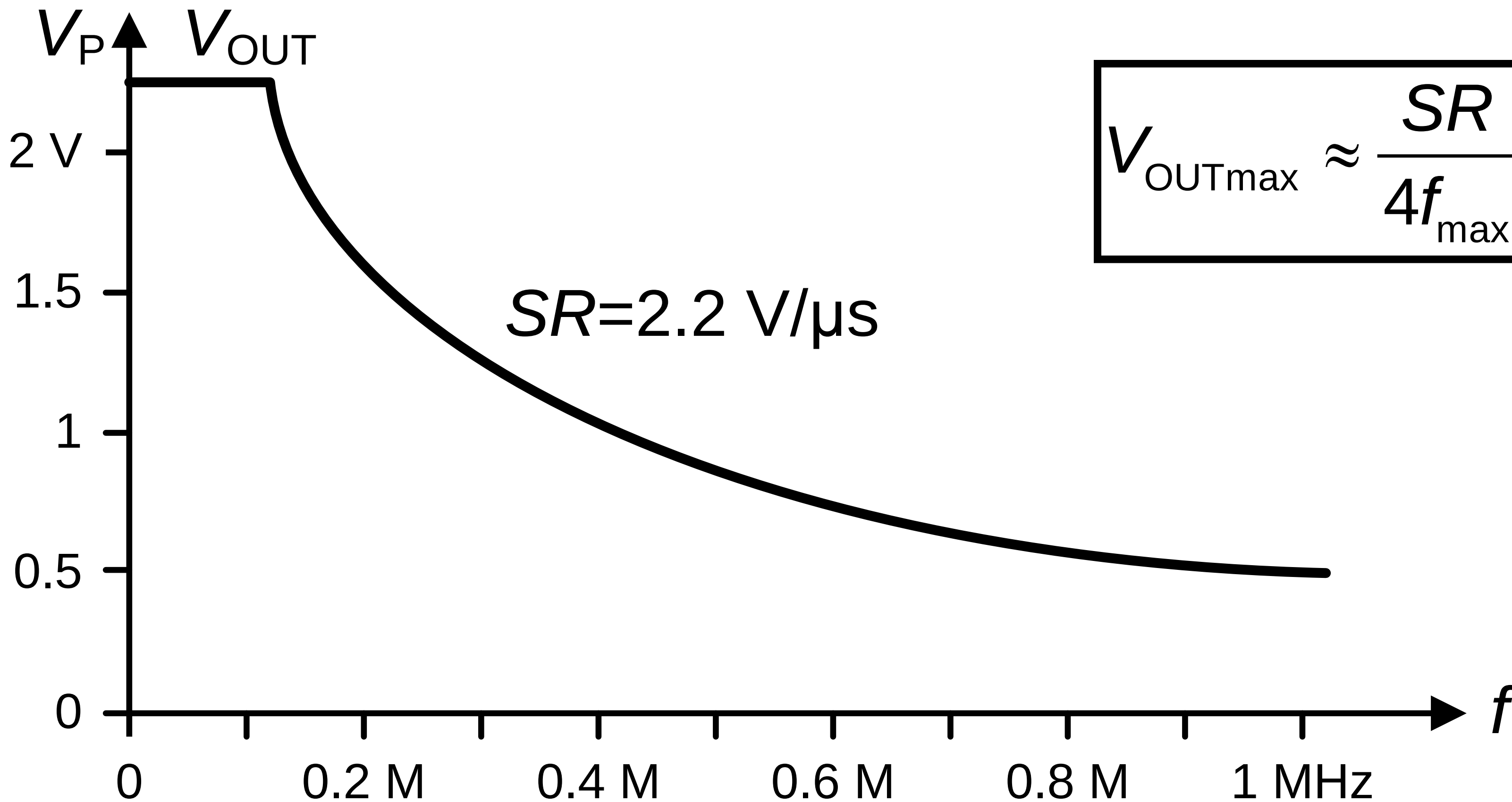


$$\frac{T_{max}}{4}$$

$$\frac{SR}{V_{OUTmax} f_{max}} \approx 4$$

$$\boxed{V_{OUTmax} \approx \frac{SR}{4 f_{max}}}$$

CMOS密勒OTA：压摆率 3



$$V_{OUTmax} \approx \frac{SR}{4 f_{max}}$$

GBW与SR的关系

$$\frac{SR}{GBW} = 4\pi \frac{I_{DS1}}{g_{m1}}$$

x 10

$$\frac{I_{DS1}}{g_{m1}} = \frac{V_{GS1} - V_T}{2} \approx 0.1 \ldots 0.3\ \text{V} \quad \text{MOST(si)}$$

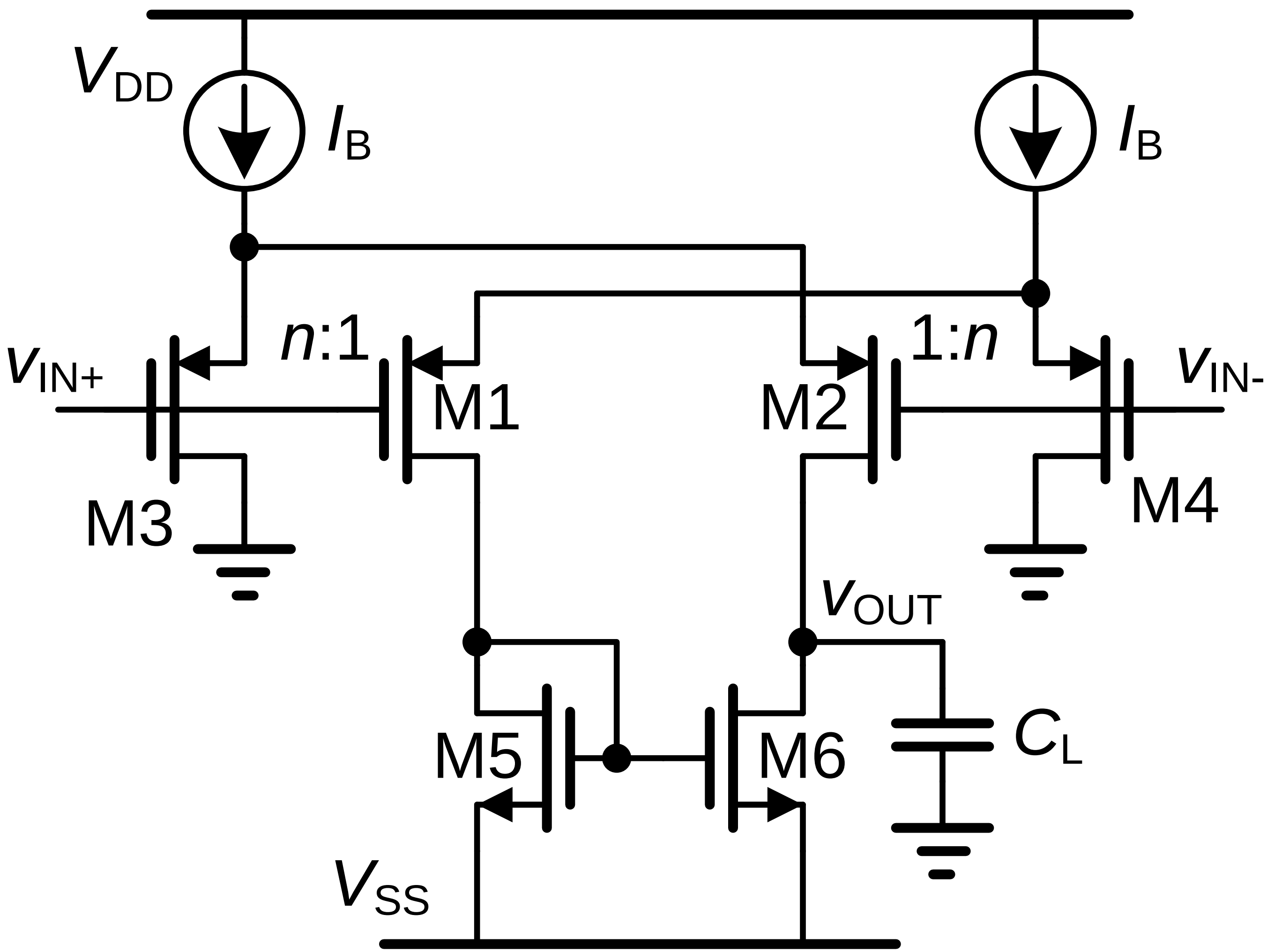
$$\frac{I_{DS1}}{g_{m1}} = \frac{nkT}{q} \approx 30 \ldots 50\ \text{mV} \quad \text{MOST(wi)}$$

$$\frac{I_{CE1}}{g_{m1}} = \frac{kT}{q} \approx 26\ \text{mV} \quad \text{Bipolar trans.}$$

$$\frac{I_{CE1}}{g_{m1}} = (1 + g_{m1}R_E)\frac{kT}{q} \approx 0.5\ \text{V} \quad 接R_E$$

Ref.: Solomon, JSSC Dec 74, 314-332

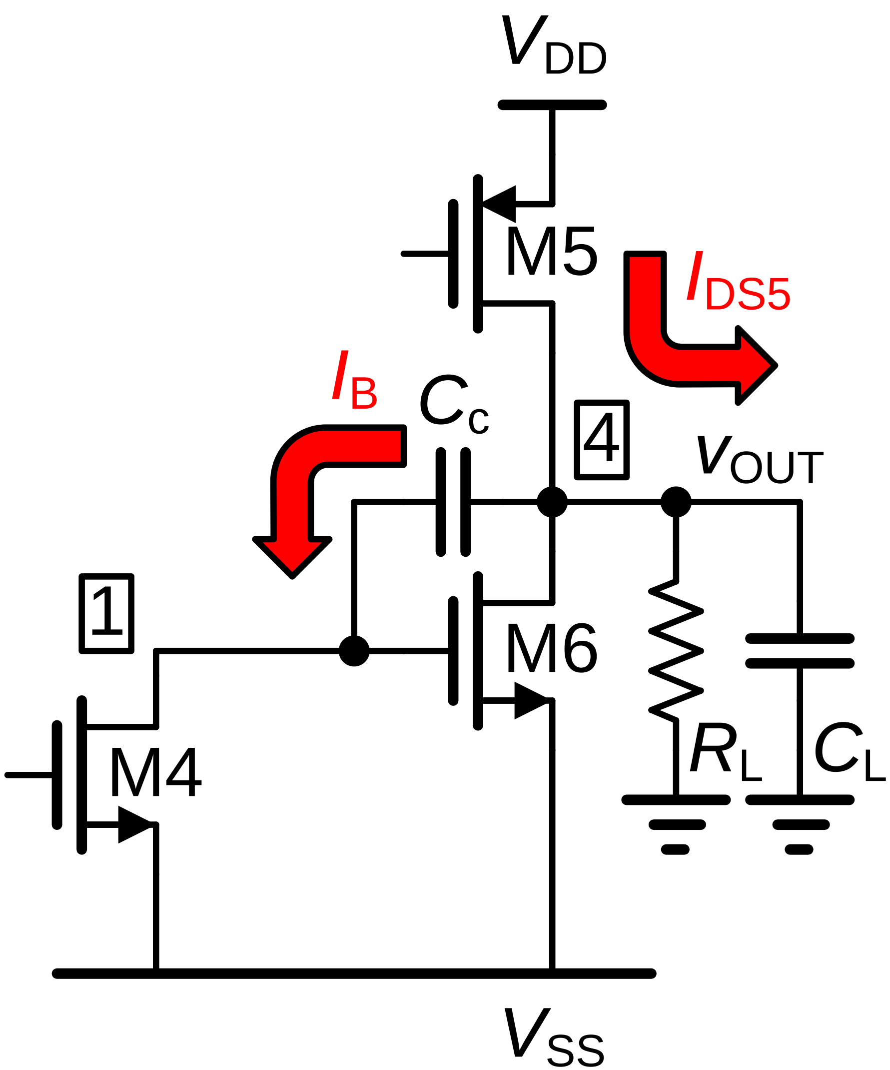
提高压摆率的方法



$$\frac{SR}{2\pi GBW} = x(n+1)$$

Ref.: Schmoock, JSSC Dec.75, 407-411

内部和外部压摆率



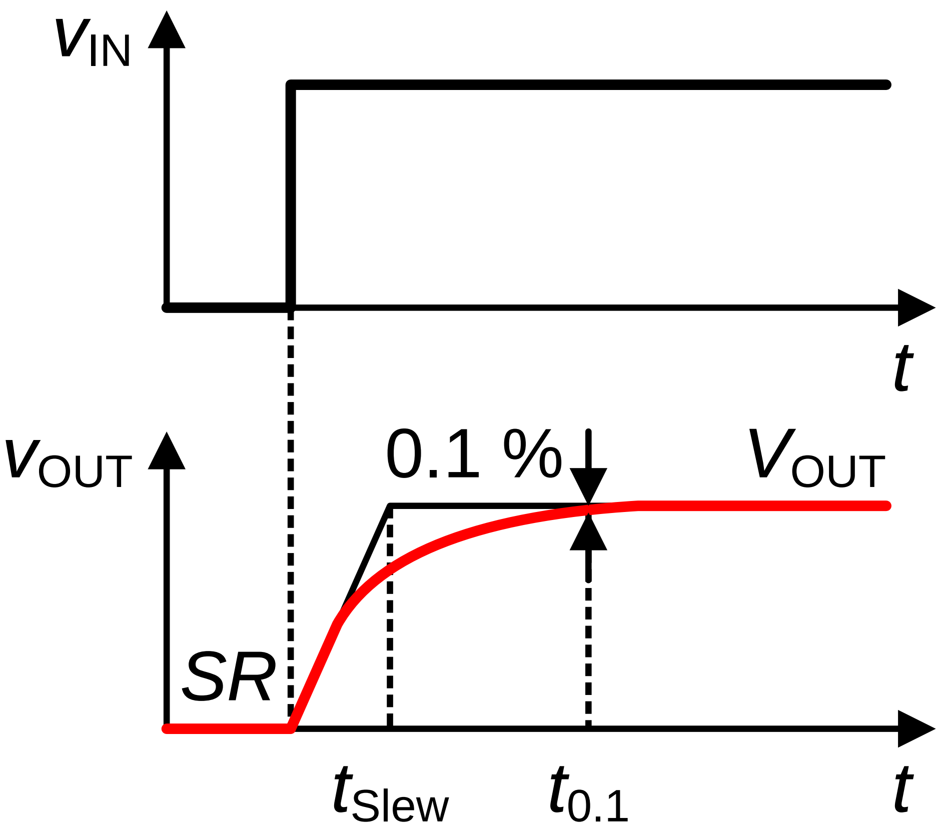
$$SR_{int} = \frac{I_B}{C_c}$$

$$SR_{ext} = \frac{I_{DS5}}{C_L}$$ 比较大！

$$\frac{g_{m6}}{g_{m1}} = 4\frac{C_L}{C_c} = \frac{I_{DS5}}{I_{DS1}}$$

$$\frac{I_{DS5}}{C_L} \approx 2\frac{2I_{DS1}}{C_c}$$

压摆率和建立时间



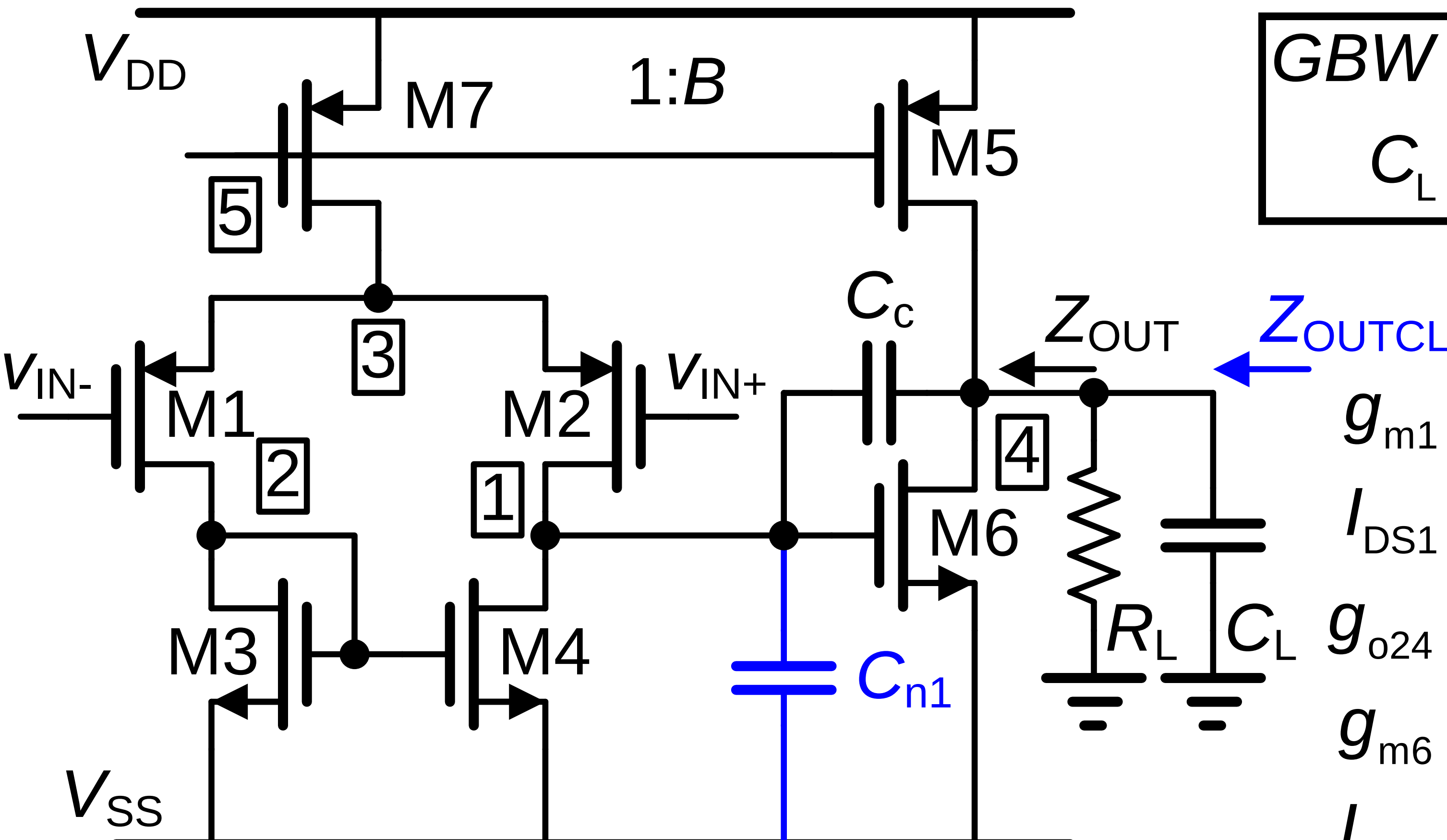
$$t_{TOT} = t_{Slew} + t_{0.1}$$

$$t_{Slew} = \frac{V_{OUT}}{SR}$$

$$t_{0.1} = \frac{7}{2\pi BW}$$

$$\ln(1000) \approx 7$$

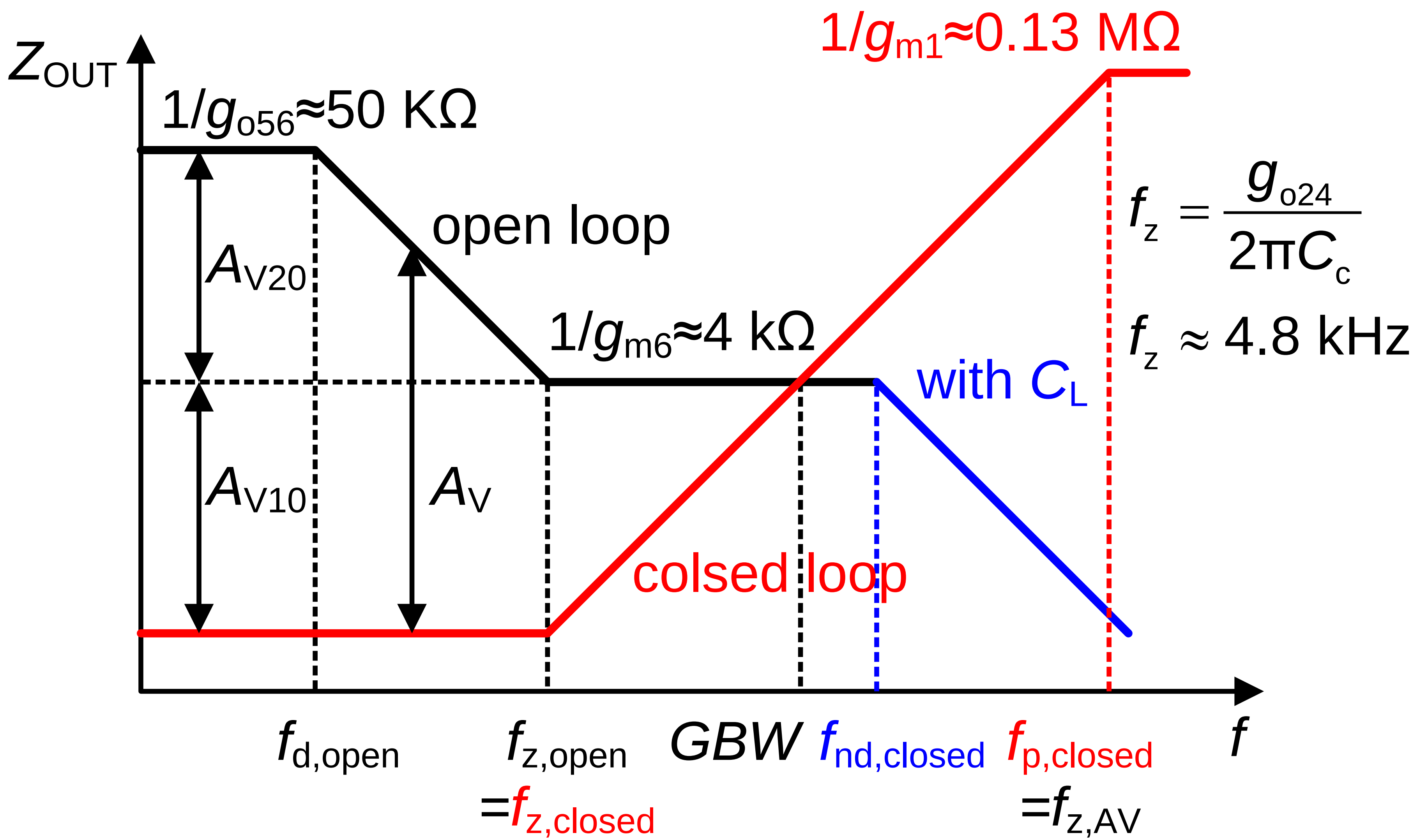
CMOS密勒OTA输出阻抗



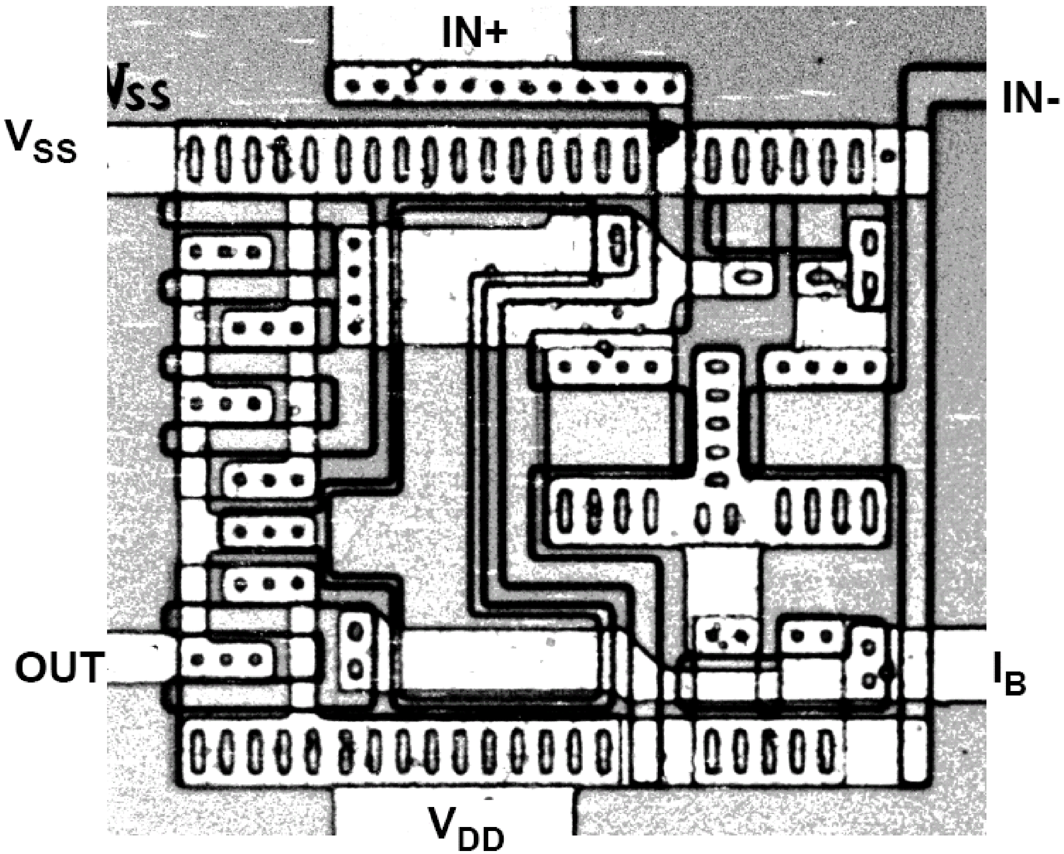
$$GBW = 1\ \text{MHz}$$
$$C_L = 10\ \text{pF}$$

$$g_{m1} = 7.5\ \mu S$$
$$I_{DS1} = 1.1\ \mu A$$
$$g_{o24} = 0.03\ \mu S$$
$$g_{m6} = 246\ \mu S$$
$$I_{DS6} = 25\ \mu A$$
$$C_c = 1\ \text{pF}$$
$$g_{Lo6} = 20\ \mu S$$

CMOS密勒OTA：输出阻抗Z_{OUT}



CMOS密勒OTA版图照片



$$GBW = 1\ \text{MHz}$$

$$C_L = 10\ \text{pF}$$

$$SR = 2.2\ \text{V/µs}$$

$$V_{DD} = 5\ \text{V}$$

$$I_{TOT} = 27\ \text{µA}$$

370 MHzpF/mA

密勒CMOS OTA：练习

已知GBW=50 MHz和C_L=2 pF：选用最小是I_{DS6}！

工艺参数

$C_L = 2\ \text{pF}$、$L_{min} = 0.5\ \mu\text{m}$、$K_n^{'} = 50\ \mu\text{A/V}^2$、$K_p^{'} = 25\ \mu\text{A/V}^2$

$C_{GS} = kW(= C_{ox}WL_{min})$ 和$k = 2\ \text{fF}/\mu\text{m}$

$V_{GS} - V_T = 0.2\ \text{V}$

求

g_{m6}、I_{DS6}、W_6、$C_{n1} = C_{GS6}$、C_c、g_{m1}、I_{DS1}、$\overline{dv_{ineq}^2}$ 和 v_{inRMS}